Effect of Multiple Flip-Chip Assembly on Joint Strength of AuSn solder in Hybrid Compact Optoelectronic Module

K.-M. Chu, *Student Member*, *IEEE*, J.-S. Lee, H. Oppermann, G. Engelmann, J. Wolf, H. Reichl, and D. Y. Jeon

***Abstract*--The hybrid integration of several electrical and optical chips on a common substrate is an important technology for merging highly functional optoelectronic modules. To fabricate such a hybrid compact optoelectronic module, it is essential to develop a multiple flip-chip assembly technique on a common substrate. In this study, four Si chips were flip-chip bonded successively on a common substrate using electroplated AuSn solder bumps. However the high thermal conductivity of the substrate and a multiple reflow process could make solder bumps formed on the substrate tend to be damaged by neighboring ones significantly during several repeated bonding steps. As a result, it is difficult to perform an interconnection that shows high bonding strength. This paper will discuss the correlation between the successive multiple flip-chip assembly and after-bonding characteristics such as die shear strength, microstructures of remelted joints between AuSn solder bumps and chip pads. In addition, we try to suggest a new bonding condition through a thermal simulation (ANSYS^{TM}).**

***Index Terms*--AuSn solder, flip-chip, ANSYS^{TM}, repeated bonding, multiple reflow**

I. Introduction

IN communications and computer-related fields, the fusion of electrical and optical technologies has been progressed rapidly. Pushing performance levels even higher will soon require hybrid circuit boards that integrate optical chips alongside electrical chips **[1]**. With this approach, the hybrid integration of semiconductor optical amplifiers (SOAs) on a silica-based planar lightwave circuit (PLC) platform is an important technology for merging the highly functional optical signal processing. To fabricate such a highly functional optical module, it is essential to develop a multi-chip assembly technique for the PLC platform **[2,3]**. In addition, since module size is one of the important factors for cost reduction, the integration density should be high to make the module compact. The eutectic Au80Sn20 solder is generally used for flip-chip assembly of optoelectronic packaging because no flux is necessary during soldering **[4]**. The AuSn solder has been proven to provide interconnections with a high reliability due to its unique mechanical properties. The AuSn solder shows an excellent wetting performance and almost void-free interconnections are achieved. Because of its good mechanical properties and the slow growth rate of intermetallic phases the reliability of the interconnection is very high **[5]**.

In this study, we have successively flip-chip bonded four Si chips on a common substrate using electroplated AuSn solder bumps. However, the high thermal conductivity of the substrate and a multiple reflow process make it difficult to form a joint that shows a high bonding strength. Because solder bump formed on the substrate tend to be thermally damaged during the repeated bonding steps. When the solder joints are reflowed several times during IC packaging processes, extensive metallurgical reaction takes place between solder bumps and their thin film pads **[6,7]**. In addition, if several chips were flip-chip bonded on a common substrate successively, the intermetallic compound (IMC) of solder bump and bonding strength would be changed during the repeated bonding steps. Also, surface oxides and other contaminants on the solder can cause non-wetting of the metallized substrates and leading to a poor metallurgical, mechanical, or conductive joint between the chip and the substrate. Due to the strong oxidation tendency of Sn, Sn oxides are easily formed on the plated sample after being exposed to ambient air **[8]**. These problems become more serious in optoelectronic multi-chip module that requires both the precise bonding alignment and the successive multiple flip-chip bonding. However, many researches are mostly focused on module performance and system demonstration after multiple flip-chip assembly **[3,9,10]**. Therefore, it is desirable to study the microstructure of the joint and the characteristics of the AuSn solder bumps during the multiple flip-chip assembly. This paper investigates the correlation between the successive multiple flip-chip assembly and after bonding characteristics such as die shear strength, microstructures of remelted joints between AuSn solder bumps and chip pads.

II. EXPERIMENT

A. *Structure and Fabrication*

This **Figure 1** shows the schematic of multiple flip-chip

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assembly for this study. For the solder reflow and flip-chip assembly experiments, test samples consisting of Si chips and compatible Si substrates were used. There are four flip-chip bonding positions on the substrate.

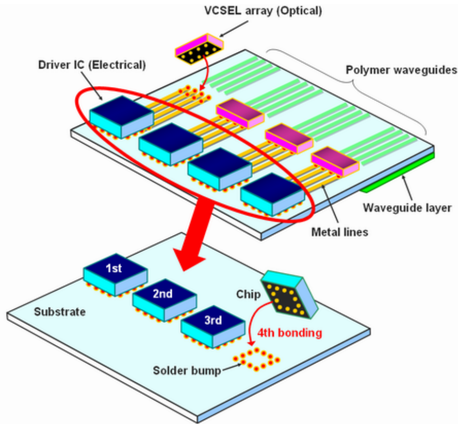
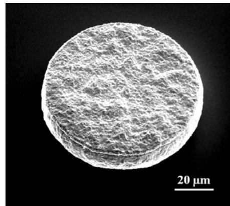
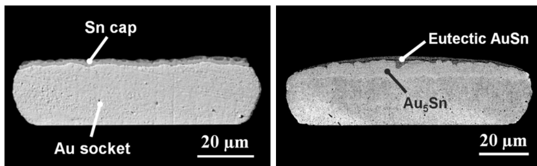


Fig. 1. The schematics of multiple flip-chip assembly on common substrate.

The process steps involved in the fabrication of AuSn bumps by electroplating were described in detail elsewhere **[11,12]**. First the plating base consisting of a Ti:W(N) and an Au layer was sputtered. The sputtering was followed by lithography of thick photo resist as plating mask. After electroplating of Au socket and the Sn cap, the resist was stripped. In the last process steps, the Au and the Ti:W(N) layers were etched. **Figure 2(b)** shows a cross sectional SEM image of an as-plated AuSn solder bump (height: 23μm, diameter: 80μm) on the surface of the substrate. After reflow process, the bump consists of an Au socket with eutectic AuSn on top and Au_5Sn (ζ-phase) layer as shown in **Fig. 2(c)**.



(a)

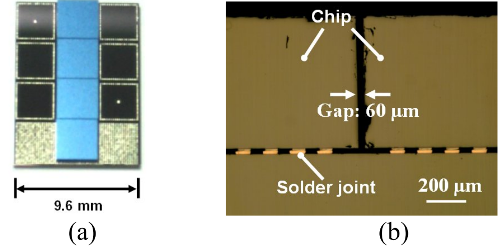


(b) (c)

Fig. 2. SEM images of AuSn solder bump after (a),(b) electroplating and (c) reflow process. (*(b),(c):cross-section view)

B. Flip-chip bonding

In this study, the chip is aligned to the alignment mark of the substrate using a flip-chip bonder (TORAY, model: FC 1500). **Figure 3** shows the image of multiple flip-chip assembled chips on the substrate. The gap between edges of chips was about 60μm. The size of the bonding stage of flip-chip bonder was 20×20 mm. The chips were flip-chip bonded successively on a common substrate at various bonding temperatures. The bonding temperatures were 280°C, 300°C, and 320°C, and the bonding pressure was 500gf.



(a) (b)

Fig. 3. Images of multiple flip-chip bonded chips on common substrate. ((a) Top view and (b) cross-section view).

III. RESULT AND DISCUSSION

A. Cross-sectional analysis of AuSn solder bump under different reflow conditions

In the first experiment, the as-electroplated AuSn solder bumps were reflowed at the bonding stage of flip-chip bonder. When the bumps are heated up to above 280°C after electroplating, the solder cap forms small volume of eutectic Au80Sn20 solder on top of the bump. **Figure 4** shows cross-sectional SEM images of reflowed AuSn solder bumps at each reflow temperatures and times.

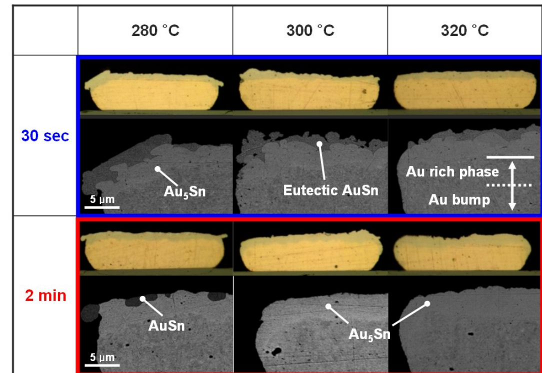


Fig. 4. Cross-sectional SEM images of reflowed AuSn solder bump at various temperatures and times.

As shown in **Fig. 4**, after 30 seconds of reflow process, two phases (eutectic AuSn and Au_5Sn) were found on top of the bump. The thickness of the Au_5Sn was about 5μm thick. The bumps which were reflowed for 2 minutes no longer show eutectic solder on top of the bumps because eutectic solder almost transformed to IMCs such as AuSn and Au_5Sn. Only a very small portion of the eutectic volume remained on top of the bump which is obviously not enough to obtain a high bonding strength. Thus, it is recommended that total bonding time including four bonding steps should not exceed 2 minutes. It is obvious that bumps with no eutectic on top are not

suitable for flip-chip assembly as the ζ-phase (Au_5Sn) stays solid beyond 500ºC. Elger et al **[5]** reported that the ζ-phase can prevent the bump from interacting with the chip pad because it has a high melting temperature.

B. Die shear test after multiple flip-chip bonding

A die shear test was conducted to investigate the change in the bonding strength for various bonding temperatures. After multiple flip-chip bonding, the assembled substrate was clamped and shear force was applied at the edge of the chip. The traveling speed of the stylus positioned 30μm above the substrate was 50μm/s. **Figure 5** shows the measured die shear strength at each bonding positions. As the number of bonding position was increased ($1^{st} \rightarrow 2^{nd} \rightarrow 3^{rd} \rightarrow 4^{th}$), the die shear strength decreased. When the bonding temperature was 300°C, the die shear strength was higher than the others except 1st bonding position. When the bonding temperature was 320°C, the die shear strength decreased to almost half of the initial value between 1st and 2nd bonding positions. In addition, at the 3rd and 4th bonding positions, there is practically no difference in die shear strength regardless of the bonding temperature. This phenomenon might have corresponded to the result of reflow test (see **Fig. 4**). Since if two chips had been flip-chip bonded on the substrate, there was only a small amount of eutectic AuSn on top of the non-bonded bumps located at 3rd and 4th bonding positions. Thus it is inferred that the number of bonding step could strongly affect the reduction in die shear strength of joint.

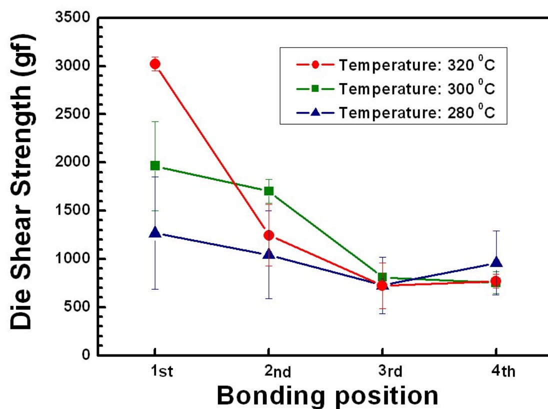


Fig. 5. Die shear strength at each bonding position after multiple flip-chip bonding. (Bonding pressure: 500g).

C. Cross-sectional analysis of joints after successive multiple flip-chip bonding

Figure 6 shows the cross sectional SEM images of joints and non-bonded solder bumps at each bonding positions during the successive multiple process. SEM and EDX results indicate that the solder bump consists of eutectic AuSn, Au_5Sn (IMC, ζ-phase) and Au socket. There were two Au_5Sn IMCs (lower: A, upper: B) at the joints.

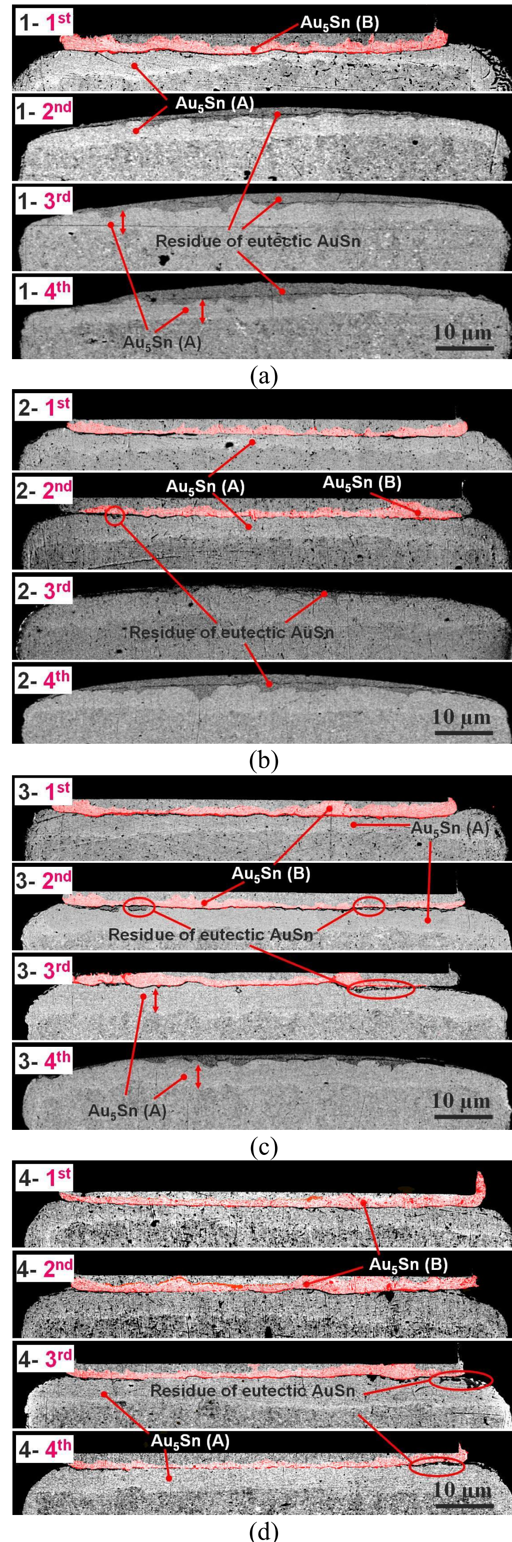


Fig. 6. Cross-sectional SEM images of joints and non-bonded bumps during flip-chip assembly. (After (a) 1st bonding step, (b) 2nd bonding step, (c) 3rd bonding step, and (d) 4th bonding step).

It was found that Au_5Sn (A) layer grew on the expense of the eutectic AuSn during the reflow process. As a result, the thickness of the eutectic AuSn decreases while that of the

Au_5Sn (A) increases during the multiple processes. While Au_5Sn (B) layer was formed by reaction between eutectic AuSn and Au chip pad during the bonding process. For example, as shown in **Fig. 6(b)**, there were two Au_5Sn IMCs (lower: A, upper: B) at 2-1st and 2-2nd joints. And the amount of remained eutectic AuSn at 2-3rd and 2-4th bonding positions is smaller than that at 1-3rd and 1-4th bonding positions (see **Fig. 6(a)**). As the solder bump approached nearly to its bonding position, the center of bonding stage, the eutectic AuSn gradually transformed to the Au_5Sn (A) phase. As a result, only a small portion of the eutectic AuSn that is solderable to the chip pad remained in the solder bump during the successive multiple flip-chip assembly.

D. Surface analysis of solder bump during the successive multiple flip-chip bonding

In this study, two specimens (I, II) were prepared to investigate the surface oxidation of bump. The 'I' solder bump (see **Fig. 2(a)**) was an as-electroplated bump and would experience one reflow step before flip-chip bonding. While 'II' solder bump located at the 4th bonding position (3-4th, see **Fig. 6(c)**) had already experienced three reflow steps before flip-chip bonding and would undergo an additional one reflow step. **Figure 7** shows the AES depth profiles of two specimens. The rich oxygen concentration near the surface means that thin Sn oxide is likely formed on the surface layers of the bumps. This Sn oxide layer might have caused the reduction in die shear strength seen in **Fig. 5**. In the case of 'I' solder bump, the oxygen concentration (-o-, **Fig. 7**) on the surface is significantly decreased at a sputter time from 0.1 to 0.2 min. While the oxygen concentration of 'I' solder bump became less than 10 at.% within 0.2 min of sputtering time but 1 min in the case of 'II' solder bump. From this depth profile, it was inferred that thin Sn oxide exists onto the top surface of the bump and bumps were easily oxidized after 1st flip-chip bonding. Also, Sn oxide was slightly grown due to the repeated bonding steps.

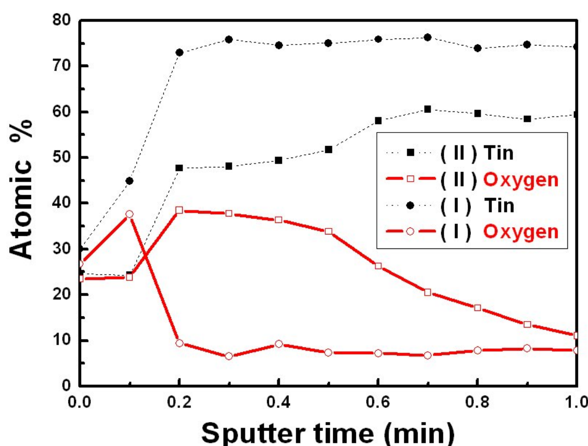


Fig. 7. Auger electron spectroscopy (AES) in-depth profile of AuSn bumps.

To find out the kinds of oxide at the top surface, XPS was used to investigate the outermost surface region of the solder bumps. Sn has three different chemical states, pure metal and two oxidation states (SnO, SnO_2), and in principle the chemical shift should differ for each state **[13,14]**. The peak was broad showing at least two different peaks that indicate Sn (① peak) and SnO (② peak). As the solder bump experienced repeated reflow steps ('I'→'II'), a high binding-energy peak (② peak, see **Fig. 8**) developed on the $Sn3d_{5/2}$ peak around at 486eV. In the case of 'I' solder bump (see **Fig. 8(a)**), the second peak (② peak, SnO) was observed at 485.6eV, and the area ratio of Sn/SnO was 1.13. While in the case of 'II' solder bump (see **Fig. 8(b)**), a second peak (② peak, SnO) was also observed at 485.6eV and the area ratio of Sn/SnO was 0.183. If we compared the XPS peaks of 'I' and 'II' solder bumps, the Sn peak (①, **Fig. 8(a)**) decreased after multiple flip-chip process while the SnO peak (②, **Fig. 8(a)**) increased relatively. This means that almost Sn phase at the surface of bump changed to SnO phase gradually as the process progressed (1st →4th). From the AES and XPS analyses, it was found that the oxide of bump consisted of mostly SnO and once the multiple flip-chip process started, SnO could be found at bump surface mainly. It is clear that SnO existed at the top surface of bump during the multiple flip-chip process and it could cause reduction in die shear strength.

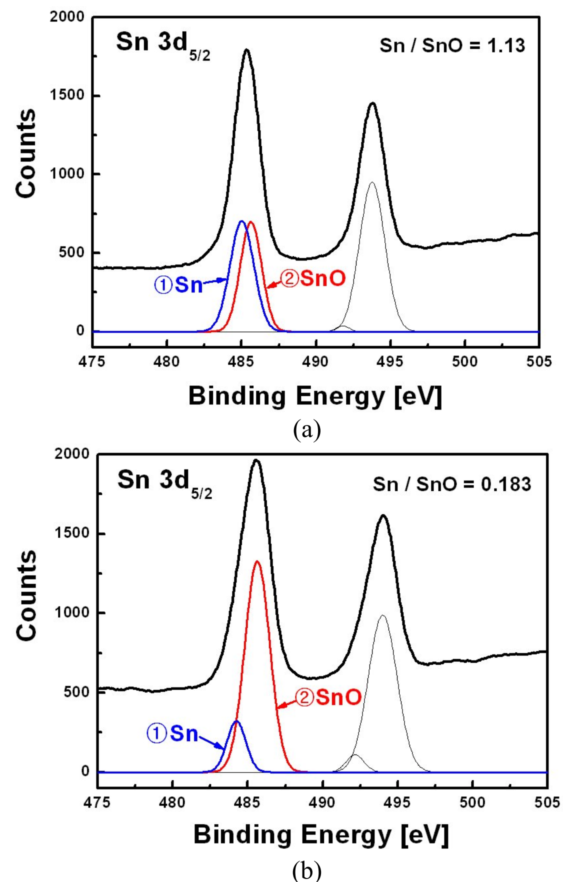


Fig. 8. $Sn3d_{5/2}$ lines for the AuSn bump ((a) 'I' and (b) 'II') during the multiple flip-chip bonding process.

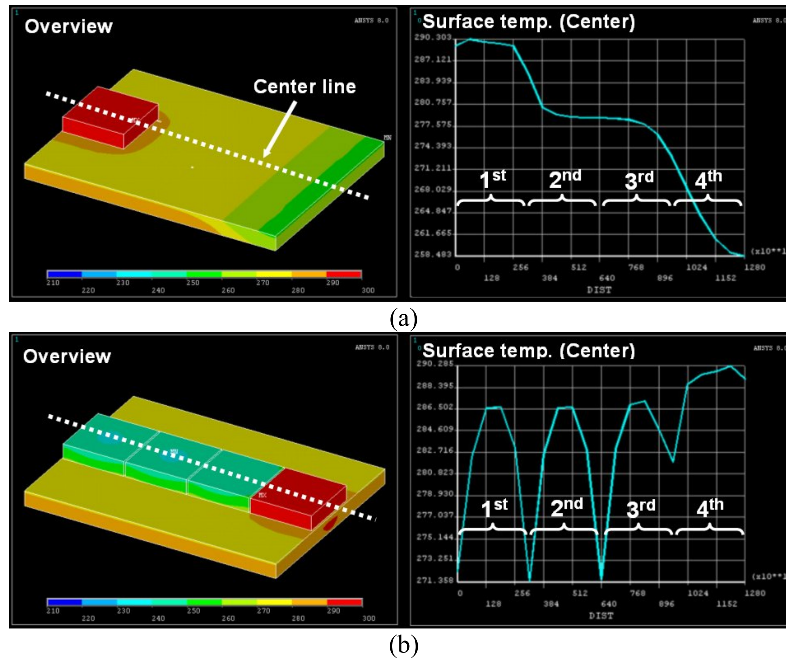
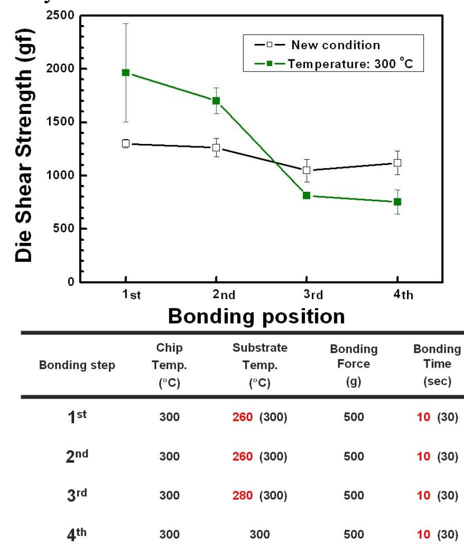


Fig. 9. Temperature distribution of multiple flip-chip bonded package with temperature profile of surface at center position after (a) 1st bonding step and (b) 4th bonding step.

E. Appropriated bonding condition for multiple flip-chip assembly

When several chips were flip-chip bonded on a common substrate, both the solder joints and non-bonded solder bumps were remelted during the multiple process. As a result, it is difficult to obtain a mechanically reliable solder joint. Thus we tried to suggest an appropriated flip-chip bonding condition through a thermal simulation (ANSYS^{TM}). **Figure 9** presents the temperature distribution of multiple flip-chip bonded package at the center of the substrate surface. While there are some temperature fluctuations at the profile. Since the chip is peripherally connected to the solder bumps, the heat generated from the substrate transferred to the chip side. Thus, local temperature of the peripherally bonded position is lower during the process. When the 1st chip was flip-chip bonded on the substrate, the calculated maximum temperature of 290.4°C exists at the center of 1st bonding position. Since the bonding temperature was applied through the chip tool, the chip generates heat and has the highest temperature. While the temperature of 4th bonding position is about 262.1°C as shown in **Fig. 9(a)**. In the case of 4th bonding step (**Fig. 9(b)**), although the amount of heat being dissipated from the lateral sides of the 4th chip to the neighbor chip (3rd) is small, it can cause about 2.4°C difference in temperature. As a result, the temperature of 3rd solder joint would reach around 281.8°C and then the joint could be remelted during the 4th bonding step. Consequently, it is advisable to adjust both the bonding temperature and time to prevent thermal damages of solder joints and bumps during the process. The results obtained from the simulation are of great value in suggesting bonding condition of multiple flip-chip package.

New bonding condition is suggested on the basis of the thermal simulation. **Figure 10** shows the die shear strength at each bonding position after multiple flip-chip bonding using a new bonding condition. Although the maximum value of die shear strength is lower than that of previous condition (**-■-**, see **Fig. 10**), we could get a uniform value successfully regardless of bonding position. In addition, total process time can be shortened by 66.7%.



Bonding step	Chip Temp. (°C)	Substrate Temp. (°C)	Bonding Force (g)	Bonding Time (sec)
1st	300	260 (300)	500	10 (30)
2nd	300	260 (300)	500	10 (30)
3rd	300	280 (300)	500	10 (30)
4th	300	300	500	10 (30)

※ ( ): previous bonding condition

Fig. 10. Comparison of die shear strength at each bonding position using previous and new bonding conditions (Bonding pressure: 500g).

IV. CONCLUSIONS

In this study, four Si chips were flip-chip bonded successively on a common substrate using electroplated AuSn solder bumps. We reported the correlation between the

successive multiple flip-chip assembly of chips and after-bonding characteristics such as die shear strength, microstructures of remelted joints between AuSn solder bumps and chip pads. There was a serious reduction of the die shear strength as the bonding position number increased ($1^{st} \rightarrow 2^{nd} \rightarrow 3^{rd} \rightarrow 4^{th}$). It was inferred that bumps which were reflowed several times show little eutectic AuSn at the joint because it almost transformed to the intermetallic phase, Au_5Sn (ζ-phase), during the multiple process. In addition, thin Sn oxide (SnO) that was formed on the surface of bump during the repeated bonding steps can cause non-wetting of the metallized chip pads and leading to a poor mechanical joint between the chip pad and the solder bump. It is necessary to optimize the bonding conditions for obtaining uniform die shear strength regardless of the bonding position during the successive multiple processes. By using a thermal simulation (ANSYS™), we successfully improved the previous bonding conditions. The results obtained from this study will offer a useful guidelines to the optoelectronic packaging industries in which a multiple flip-chip assembly is needed.

V. Acknowledgment

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VII. Biographies

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