VLSI Symposium on Circuits 2017 Reports Program (2017/6/15)

Session Chair	Time		Title	Speaker(Affiliation)
	13:00 13:15		Opening / Review of VLSI Symposium 2017	Makoto Ikeda (University of Tokyo)
Dr. Ryuichi Fujimoto (Toshiba Memory)	13:15 13:30	C19-1	A 4.1Mpix 280fps Stacked CMOS Image Sensor with Array-Parallel ADC Architecture for Region Control	Tomohiro Takahashi (Sony Corporation)
	13:30 13:45	C19-4	224-ke Saturation Signal Global Shutter CMOS Image Sensor with In-pixel Pinned Storage and Lateral Overflow Integration Capacitor	Yorito Sakano (Sony Corporation)
	13:45 14:00	C12-3	A 140 MHz 1 Mbit 2T1C Gain-Cell Memory with 60-nm Indium-Gallium-Zinc Oxide Transistor Embedded into 65-nm CMOS Logic Process Technology	Takahiko Ishizu (Semiconductor Energy Laboratory)
	14:00 14:15	JFS3-4	A 65 nm 1.0 V 1.84 ns Silicon-on-Thin-Box(SOTB) Embedded SRAM with 13.72 nW/Mbit Standby Power for Smart IoT	Makoto Yabuuchi (Renesas Electronics)
	14:15 14:30	C17-1	System Architecture with Single Chip 8K HEVC Decoder for 8K Advanced BS Receiver System	Masaitsu Nakajima (Socionext)
	14:30 15:00		Break	
Dr. Toshiya Mitomo (Toshiba)	15:00 15:15	JFS1-1	An Adaptive Clocking Control Circuit with 7.5% Frequency Gain for SPARC Processors	Tetsutaro Hashimoto (Fujitsu Laboratories)
	15:15 15:30	C23-4	43%-Efficiency 20dBm Sub-GHz Transmitter Employing Rise-Edge-Synchronized Harmonic Calibration with 33.3% Duty Cycle	Masakazu Mizokami (Renesas Electronics)
	15:30 15:45	C25-3	A 2.25-mW/Gb/s 80-Gb/s-PAM4 Linear Driver with a Single Supply using Stacked Current-Mode Architecture	Shinsuke Nakano (Nippon Telegraph and Telephone Corporation)
	15:45 16:00	C23-1	A 100mW 3.0 Gb/s Spectrum Efficient 60 GHz Bi-Phase OOK CMOS Transceiver	Yun Wang (Tokyo Institute of Technology)
	16:00 16:15	C10-1	A Pulse-Tail-Feedback VCO Achieving FoM of 195dBc/Hz with Flicker Noise Corner of 700Hz	Aravind Tharayil Narayanan (Tokyo Institute of Technology)
	16:15 16:30	C10-2	A 3.2ppm/C Second-Order Temperature Compensated CMOS On-Chip Oscillator Using Voltage Ratio Adjusting Technique	Guoqiang Zhang (Renesas Electronics)
	16:30 16:45	C22-2	車載LIDAR向け2D-SPADチップの研究 (An Imager Using 2-D Single-Photon Avalanche Diode Array in 0.18-μm CMOS for Automotive LIDAR Application)	Hironobu AKITA (Denso)
	16:45 17:00		Break	
Prof. Makoto Nagata (Kobe University)	17:00 18:00		**IEEE SSCS Kansai Chapter, Distinguished Lecture**	Hirotaka Tamura (Fujitsu Laboratories)

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