IEEE SSCS Japan Chapter Technical Seminar

—NTU-MTK Wireless Lab Visiting IEEE SSCS Japan Chapter—

The University of Tokyo
June 18, 2007

Agenda

Welcome and opening remarks **2:00-2:05 PM**
Dr. T. Furuyama, Chairman of IEEE SSCS Japan chapter

I. SSCS Region 10 and NTU-MTK Wireless Lab

Initiatives/Status/Cooperation for IEEE SSCS, 2008 ISSCC and 2007 A-SSCC **2:05-2:20 PM**
Prof. C-k Wang
The topic presents the promotions, activities and overall plans cooperated among SSCS, ISSCC in Feb. 2008 and A-SSCC in Nov. 2007.

Introduction -- the Academic Advancement in NTU/Taiwan **2:20-2:30 PM**
Prof. C-k Wang
This topic introduces the development of academic research in semiconductor IC design in National Taiwan University. In order to explain the advancement of academic IC design in NTU, this presentation focuses on the introduction of overall operation of NTU-MTK Lab, which is the most representative collaboration model between academic and semiconductor IC industry in Taiwan, and also covers the government policies for cultivating semiconductor IC human resource in Taiwan.

NTU-MTK Wireless Faculty Members **2:30-3:30 PM**
Faculty of NTU-MTK Wireless Lab
Introducing to individual research interests/plans and current research achievements by NTU-MTK Wireless Lab faculty.

II. Research Presentations

RF Building Blocks

Ultra-Low-Power and Ultra-Low-Voltage Techniques for RFICs **3:30-3:55 PM**
Hsieh -Hung Hsieh
In this talk, ultra-low-voltage and ultra-low-power techniques for RF front-ends are demonstrated. By using various design strategies, the circuits including LNA, T/R switch and VCO are introduced for 0.6-V 5-GHz operations. A 0.5-V 1.9-GHz phase-locked loop will also be included in this speak to illustrate the approach to low-voltage and low-power system integration in CMOS process.

PLL/CDR/Frequency Synthesizer

A 75GHz PLL in 90nm CMOS *(2007 ISSCC Beatrice Winner Award)* **3:55-4:20 PM**
Prof. Jri Lee
The design and experimental verification of a 75GHz PLL implemented in a 90nm CMOS process are presented. The circuit incorporates a three-quarter wavelength oscillator and a PFD based on SSB mixers and achieves an operation range of 320MHz and reference sidebands of less than -72dBc while consuming 88mW from a 1.45V supply.

Break **4:20-4:30 PM**

A Jitter-Tolerance-Enhanced CDR Using a GDCO-Based Phase **4:30-4:55 PM**
Che –Fu Liang
A jitter-tolerance-enhanced 10Gb/s clock and data recovery (CDR) circuit is presented. By using a gated-digital-controlled oscillator (GDCO), the proposed GDCO-based phase detector achieves a wide linear range and its jitter tolerance is enhanced by a factor of two without sacrificing the jitter transfer. The extra hardware and power consumption are less than the traditional jitter-enhancing techniques. The prototype chip has been fabricated in 0.13um CMOS technology and consumes 60mW from a 1.5V supply. It occupies a core area of 0.36mm^2. Measurements on the testing chip demonstrate an rms jitter of 0.96ps, and a peak-to-peak jitter of 7.11ps.

A Fully Integrated 36MHz to 230MHz Multiplying DLL with Adaptive Current Tuning
Keng-Jan Hsiao **4:55-5:20 PM**
A multiplying-DLL based frequency synthesizer with a fully-integrated loop capacitor employs an adaptive current adjusting loop to generate low-jitter clock for LCD panel applications. The measured rms jitter is 3.5ps for 229.5-MHz output clock. The frequency synthesizer occupies 0.09mm2 active area in a 0.18-mm CMOS technology and consumes 9 mW from a 1.8-V supply.

Baseband Signal Processing

A 19-mode 8.29mm² 52-mW LDPC Decoder Chip for IEEE 802.16e System **5:20-5:45 PM**

Xin-Yu Shih

This talk presents a LDPC decoder chip supporting all 19 modes in IEEE 802.16e system. An efficient design strategy is proposed to reduce 31.25% decoding latency, and enhance hardware utilization ratio from 50% to 75%. Besides, we propose an early termination scheme that can dynamically adjust the number of iterations. The multi-mode chip can be maximally measured at 83.3MHz with only 52mW power consumption. The core area is 4.45mm² and the die area is 8.29mm².

Conclusion **5:45- PM**