＜ISSCC’2009 報告会＞

日時: 2009年3月2日(月) 9:30～17:00
会場: 東京大学本郷キャンパス武田先端知ビル 5F 武田ホール
主催: Japan Chapter, IEEE Solid-State Circuits Society
協賛: ISSCC Far-East Regional Committee

********** ISSCC’2009 報告会 プログラム **********

<<午前の部>> 9:30-12:00

○挨拶 9:30-9:35 松澤 昭
IEEE SSCS Japan Chapter Chair

○レビュー講演1 9:35-10:00 (講演 20 分＋質疑 5 分)
「ISSCC2009 の Overview」 河原 尊之
ISSCC Far-East Regional Committee Chair

○論文発表
[午前の部] 発表 4 件 10:00 - 11:50(それぞれ講演＋質疑 REGULAR 30 分 SHORT 20 分)
座長 松澤 昭 (IEEE SSCS Japan Chapter Chair, 東工大)

<< Wireline >>
1. "An 18Gb/s Duobinary Receiver with a CDR-Assisted DFE" (16.1)
Kazuhisa Sunaga, NEC

<< Imager >>
2. "A Charge-Multiplication CMOS Image Sensor Suitable for Low-Light-Level Imaging" (2.7) [SHORT]
Ryu Shimizu, Sanyo Electric

<< Technology Direction >>
3. "Wireless DC Voltage Transmission Using Inductive-Coupling Channel for Highly-Parallel Wafer-Level Testing" (28.2)
Yoichi Yoshida, Keio University

4. "A Subjective-Contour Generation LSI System with Expandable Pixel-Parallel Architecture for Vision Systems" (28.6)
Takashi Morie, Kyushu Institute of Technology

○昼休み 11:50～13:00

[午後の部 I]　発表4件　13:00 - 14:30 （それぞれ講演＋質疑 REGULAR 30 分 SHORT 20 分）
座長　岡田　健一　（IEEE SSCS Japan Chapter Secretary, 東工大）

<< RF >>

5. "A 77GHz Transceiver in Standard 90nm CMOS" (18.3)
   Yoichi Kawano, Fujitsu Laboratories

6. "A 59GHz Push-Push VCO with 13.9GHz Tuning Range Using Loop-Ground Transmission Line for a Full-Band 60GHz Transceiver" (29.7) [SHORT]
   Takahiro Nakamura, Hitachi Ltd.

7. "A 0.6V 380μW -14dBm LO-Input 2.4GHz Double-Balanced Current-Reusing Single-Gate CMOS Mixer with Cyclic Passive Combiner" (12.5) [SHORT]
   Jun Deguchi, Toshiba

8. "A 2.88Gb/s Digital-Hopping UWB Transceiver" (18.7) [SHORT]
   Akio Tanaka, NEC

○休憩　14:30 - 15:00

<<午後の部 II>>　発表4件　15:00 - 17:00　（それぞれ講演＋質疑30 分）
座長　内山　邦男　（IEEE SSCS Japan Chapter Vice Chair, 日立）

<< Memory >>

9. "A Process-Variation-Tolerant Dual-Power-Supply SRAM with 0.179μm^2 Cell in 40nm" (27.2)
   Osamu Hirabayashi, Toshiba Semiconductor

10. "A 90nm 12ns 32Mb 2T1MTJ MRAM" (27.4)
    Ryusuke Nebashi, NEC

<< Low Power Digital >>

11. "A 342mW Mobile Application Processor with Full-HD Multi-Standard Video Codec" (8.7)
    Kenichi Iwata, Renesas Technology

12. "A 45nm Single-Chip Application-and-Baseband Processor Using an Intermittent Operation Technique" (8.6)
    Motoyasu Shirasaki, Panasonic

○閉会　17:00

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[お問い合せ先]

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Homepage: http://www.ieee-jp.org/japancouncil/chapter/SSC-37/ssc.htm

会場：http://www.u-tokyo.ac.jp/campusmap/cam01_04_16_j.html