Reliability of scaled Metal Gate / High-K CMOS devices

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Abstract:
Aggressively scaled transistor technologies with metal gate/high-k stacks encounter additional reliability challenges beside bias temperature instability (BTI) in PMOS and NMOS devices, time dependent dielectric breakdown and hot carrier degradation. Time-zero variability and variability induced by device aging is a growing concern which needs to be modeled using stochastic processes. The physical nature of the stochastic process remains under debate and to support model development efforts large statistical data sets are essential. In addition, self-heating during reliability testing can be observed in novel device structures like bulk FinFET, SOI FinFETs, FDSOI and gate-all-around devices and needs proper attention. Furthermore, to increase the confidence in the discrete device reliability models, device-to-circuit correlations need to be established. In this presentation we discuss how to obtain stochastic BTI data for discrete SRAM and logic device beyond 3σ, address device-to-circuit correlations using ring-oscillators and explore self-heating effects in FinFET and SOI devices.

Andreas Kerber received his Diploma in physics from the University of Innsbruck, Austria, in 2001, and a PhD in electrical engineering from the TU-Darmstadt, Germany, with honors in 2014. From 1999 – 2000 he was an intern at Bell Laboratories, Lucent Technologies (Murray Hill, NJ, USA) working on the electrical characterization of ultra-thin gate oxides. From 2001 to 2003, he was the Infineon Technologies assignee to International SEMATECH at IMEC in Leuven, Belgium, where he was involved in the electrical characterization of alternative gate dielectrics for sub-100 nm CMOS technologies. From 2004 to 2006, he was with the Reliability Methodology Department at Infineon Technologies in Munich, Germany, responsible for the dielectric reliability qualification of process technology transfers of 110 and 90 nm memory products. During that time he developed a low-cost, fast wafer-level data acquisition setup for time-dependent dielectric breakdown (TDDB) testing with sub-ms time resolution. In 2006, he joined AMD in Yorktown Heights, NY, and now is with GLOBALFOUNDRIES in Malta, NY, working as a Principal Member of Technical Staff on front-end-of-line (FEOL) reliability research with focus on metal gate / high-k CMOS process technology, advanced transistor architecture and device-to-circuit reliability correlation. Dr. Kerber has contributed to more than 95 journal and conference publications and presented his work at international conferences, including the VLSI, IEDM and IRPS. In addition, he has presented tutorials on metal gate / high-k reliability characterization at the IIRW and IRPS. Dr. Kerber has served as a technical program committee member for the SISC, IRPS, IEDM, Infos, ESSDERC, is a Senior Member of the IEEE and a Distinguished Lecturer (DL) for the IEEE Electron Devices Society.