



## IEEE EDS Distinguished Lecturer Seminar

Time & date: December 22, 2016, 15:00-17:00

Venue: Conference room #1 (3F), Center for Innovative Integrated Electronic Systems (CIES),  
Tohoku University

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### Future Devices Enabled by 2D Nanomaterials

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**Abstract:** Discovered twelve years ago, graphene and its derivative material systems have received significant amount of research interests from both academia and industry. These emerging 2D nanostructures exhibit unique electrical, thermal, and electromechanical properties, attributed to their distinctive layered configuration, band structure, and quantum phenomena. The atomically-thin nanosheets could be potentially assembled by the existing commercial thin-film techniques. While graphene has been explored as both active and passive elements in the imaginary “all-carbon electronics”, its gap-less nature implies fundamental limitations that promote innovations in both new device principle and material engineering. This seminar will introduce the latest research of my lab in material preparation and demonstration of different device/technology prototypes, including logic switch, memory, on-chip interconnects, solar cells, and sensors, on emerging 2D material platforms. Challenges and near-future research opportunities in the respective areas will be also highlighted.

**Bio:** Dr. Bin Yu received Ph.D. degree in Electrical Engineering from University of California at Berkeley. He is currently Professor at SUNY College of Nanoscale Science & Engineering. His research is in the field of solid-state devices and nanoelectronics. Specific interests include post-CMOS devices, memories, carbon interconnects, nano-photovoltaics, and nano-sensors. He has authored/co-authored 8 book/contributed book chapters, more than 250 research publications, and was the speaker of 100+ invited talks to conferences, professional societies, universities, and industry. As one of the prolific inventors, he has more than 300 awarded U.S. patents. Dr. Yu served as Editor of IEEE Electron Devices Letters, Associated Editor of IEEE Transactions on Nanotechnology, Editor of Nano-Micro Letters, and Guest Editor of IEEE Transactions on Electron Devices and IEEE Transactions on Nanotechnology. He also served on the invited panels and advisory/technical program committees of many international conferences, and was the CMOS Subcommittee Chair of IEEE IEDM (2002-2003). He is IEEE Fellow, IEEE Distinguished Lecturer, recipient of IBM Faculty Award, and was appointed as a Consulting Professor at Stanford University, Guest Professor at Beijing University and Zhejiang University. Dr. Yu’s prior research includes the first 10-nm gate length “FinFET” (IEDM’ 2002), among others.

**Organizers:** IEEE EDS Japan Chapter

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