Nanocrystal embedded MOS non-volatile memory devices

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Introduction
Nanotechnology: A Revolutionary Concept

“*There’s plenty of room at the bottom*”
-Richard P. Feynman
(Caltech, 29.12.1959)

Today Nanotechnology is a vast Inter-disciplinary Field
The applications of Nanotechnology are numerous

Source: http://lib.bioinfo.pl/blid:1739

Nano-electronics holds a major share in this

Source: NATIONAL SCIENCE FOUNDATION, USA
MOS Memory Devices

- USB Flash drives
- Memory cards (SD, MMC, M2) used in mobile phones, digital cameras, MP3 players
- Computer DRAMs, Solid State Hard Drives (HDD)
- & many more

They are everywhere
Various MOS Memory Devices

Flash Card Market Growth

Card Units, M

2000
1500
1000
500
0

2006 2007 2008 2009 2010 2011

Digital Still Camera

Mobile Phone

Other

% Phones w/ Card Slots

DSC Card Density

Phone Card Density

68% >1B

Avg Card GB

*Source: SEC Marketing

Samsung
**Flash Memory Market Growth (NAND & NOR)**

*Data Source: WSTS & IC Insights*

<table>
<thead>
<tr>
<th>Year</th>
<th>Flash Memory Market (USD mn)</th>
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<tr>
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**Flash Memory Market Share (Q3 2010)**

- **SAMsUNG**: 28.5%
- **TOSHIBA**: 15.1%
- **MICRON**: 8.1%
- **HYNIX**: 3.7%
- **INTEL**: 2.1%
- **MACRONIX**: 2.5%
- **SPANSON**: 1.9%
- **WINBOND**: 1.5%
- **OTHERS**: 33.8%

*Data Source: http://www.isuppli.com/Abstract/P13698_20110331172924.pdf*
Transistors per die of MOS Memory Devices
MOSFET memory and MOS capacitors

MOSFET memory devices rely on charge stored in the Floating Gate to cause a shift in the threshold/ flatband voltage.

Campardo et. al. VLSI Design of Non-Volatile Memories, Springer Verlag, Berlin Heidelberg 2005, pp. 50
Conventional MOS NVMs: Floating gate & SONOS

- Charges are stored in the polysilicon Floating Gate.
- Most commonly used for Flash memory applications.

- Charges are stored in the Oxide-Nitride interface.
- Another variant MNOS useful for Aerospace/Military applications.
Fig. 2.3: Band diagrams of a Program /Erase operations of a floating gate cell

(Ref: Micheloni et. al. Inside NAND Flash memories, Springer pp.91)
Disadvantage of conventional MOS Memory Devices

- With scaling and thinner tunnel oxides, leakage provides a major challenge.
- Also for portability lesser write voltages are required.
- Advantages of Nanotechnology may be applied to MOS devices.
- Nanocrystal embedded MOS NVMs can help in this regard.
**Road-block:** Gate oxide tunneling current, the quantum nature of matter lets electrons penetrate the gate oxide.

- **Gate leakage:** ~100 A
- **Gate leakage:** ~0.1 A

**Figure:**
- **130 nm 2001**
- **60 nm**

**Graph:**
- **Nanotechnology**
- **Transistor cost**
- **Road-block:**
  - **Gate oxide tunneling current**
  - **Quantum nature of matter**
  - **Electrons penetrate the gate oxide**

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- **Courtesy: Prof. Jakub Kedzierski**
- **IIT-Bombay/MIT Lincoln Lab**
Nanoparticles Based Floating Gate MOS Memory Structure

- Nanoparticles (nc) diameter in 5-6nm range.
- Confined in a narrow layer within SiO₂ called embedded gate dielectric.
- Charging and discharging of nc carried out by electron tunneling.
- Electrons tunnel from Si substrate to gate electrode through gate dielectric.
- A thin tunneling barrier is formed at the interface of silicon substrate and composite gate dielectric.
- Comparison of nc-Si and nc-Ge embedded gate oxide MOS devices.

Nanoparticles embedded floating gate MOSFET and MOSCAP.
Write/Erase mechanism of such a device
Advantages of Nanocrystal embedded MOS NVM
Recent Developments
Metallic Nanocrystals

Use of Metallic nanocrystals like Ni, W, Ag, Au, Pt ncs.

Better charge storage, Lesser leakage, improved retention


Lee et. al. IEEE TED 52, 4, 507 (2005)
CNT/ C60 embedded MOS NVM


Stacked High-k gate dielectrics

- **High-k materials help in suppressing the leakage.**
- **They have better charge retention than SiO$_2$ gate dielectrics.**
- **Better Program / Erase cycles endurance.**
Compound semiconductor MOSFET

- Compound semiconductors like $\text{In}_x\text{Ga}_{1-x}\text{As}$, GaN, InP, GaAs have better MOSFET performance than conventional Si or strained Si MOS.
- Such compound semiconductor MOS can be used for memory applications as well.


Multigate MOS NVM structures

Yeom et. al. Nanotechnology 19 (2008) 395204


Modeling of MOS Non-Volatile Memories
Why Modeling?

• Many device structures, many materials in terms of the embedded NCs and the substrate materials.

• Fabrication and testing is costly, time-consuming and requires infrastructure and manpower.

• A good model can thus act as a pointer in the right direction well before the actual fab is carried out.
Need for New Simulations

- **Standard device simulators like Sentaurus, Silvaco TCAD do not incorporate nanocrystal embedded MOS NVMs.**
- **Existing models are either involving a large amount of numerical solutions and rather complex iterative orthogonalization and extraction methods for 3D Kohn-Sham / Poisson-Schrodinger equations.**
- **No analytical models for advanced multi-gate nc embedded gate dielectric MOSFET NVMs.**
Write Mechanism: Fowler – Nordheim Tunneling

- High Applied Gate voltage $\rightarrow$ Fowler-Nordheim tunneling
- The barrier becomes Triangular in shape
- Applied gate voltage $V > \left( \phi_{\text{eff}} - E_0 \right)/q$
- Electrons tunnel from the conduction band of Si to conduction band of oxide through part of potential barrier

Band diagram of Fowler-Nordheim tunneling
Band Structure of Tunneling under Different Conditions of Applied Electric Field

Band bending at applied electric fields under different conditions (a) \[ F_{\text{eff}} d < \phi_{\text{eff}} - E_n \] (b) \[ \phi_{\text{eff}} - E_n < F_{\text{eff}} d < \phi - E_n \] (c) \[ F_{\text{eff}} d > \phi - E_n \]
F-N Tunneling Probability

**Case I:** \( qF_{eff}d < (\phi_{eff} - E_o) \)

\[
D(E_0) = \exp \left( -\frac{4\sqrt{2}m_{eff}}{3q\hbar F_{eff}} \left( (\phi_{eff} - E_0)^{3/2} - (\phi_{eff} - E_0 - qF_{eff}d)^{3/2} \right) - \frac{4\sqrt{2}m}{3q\hbar F} (\phi - E_0 - qF_{eff}d)^{3/2} \right)
\]

**Case II:** \( (\phi_{eff} - E_o) < qF_{eff}d < (\phi - E_o) \)

\[
D(E_0) = \left\{ \sin^2 \theta_2 \cosh^2 (\theta_3 - \theta_1) + \cos^2 \theta_2 \cosh^2 \left[ \theta_3 + \theta_1 + \ln(4) \right] \right\}^{-1}
\]

\[
\hbar \theta_i = \int_{x_{i-1}}^{x_i} \left\{ 2m^* \left[ V(x) - E_0 \right] \right\}^{1/2} dx
\]

**Case III:** \( qF_{eff}d > (\phi - E_o) \)

\[
D(E_0) = \exp \left( -\frac{4\sqrt{2}m_{eff}}{3q\hbar F_{eff}} (\phi_{eff} - E_0)^{3/2} \right)
\]
Leakage: Direct Tunneling

- Low Applied Gate voltage $\rightarrow$ Direct tunneling
- Applied gate voltage condition
- The Barrier becomes Trapezoidal in shape
- Electrons tunnel directly from Si conduction band to metal instead of through oxide conduction band

Band diagram for direct tunneling

$$J_D = \frac{\left\{2m_{\text{eff}} \left(\phi_{\text{eff}} - E_0\right)\right\}^{1/2} \alpha q^2 V}{\hbar^2 d} \exp \left(\frac{2\alpha \sqrt{2m_{\text{eff}} \left(\phi_{\text{eff}} - E_0\right)}}{\hbar} d\right)$$
Parameters changed due to inclusion of Nanoparticles

- Dielectric constant of SiO₂ embedded with nc-Si determined by using Maxwell-Garnett Effective Medium Approximation (EMA)

\[
\varepsilon_{nc-ox} = \frac{\varepsilon_{ox} \left\{ 2\nu (\varepsilon_{nc} - \varepsilon_{ox}) + (\varepsilon_{nc} + 2\varepsilon_{ox}) \right\} \varepsilon_{nc} + 2\varepsilon_{ox} - \nu (\varepsilon_{nc} - \varepsilon_{ox})}{\varepsilon_{nc} + 2\varepsilon_{ox} - \nu (\varepsilon_{nc} - \varepsilon_{ox})}
\]

\[
\varepsilon_{eff} = \frac{t_{ox}}{\varepsilon_{ox} \cdot t} + \frac{t - t_{ox}}{\varepsilon_{nc-ox} \cdot t}
\]

- Band gap energy has been modified

\[
E_{gnc} = E_{bulk} + \frac{\hbar^2 \pi^2}{2R^2} \left( \frac{1}{m_h^*} + \frac{1}{m_e^*} \right)
\]

- Effective barrier height modified

\[
\phi_{eff} = \frac{1}{2} \left[ \frac{E_{gsio2}}{2} + \frac{1}{2} \left( E_{gsio2} \cdot (1 - \nu) + \nu \cdot E_{gnc} \right) - E_{gsi} \right]
\]

- Electron effective mass has been changed

\[
m_{eff} = \frac{m_{sio2} d_{sio2}}{d} + \frac{m_{nc} (d - d_{sio2})}{d}
\]
 FN plot compares the pure SiO$_2$ gate dielectric with the nc-Si and the nc-Ge embedded dielectric.

- Both The nanoparticles embedded composite gate dielectrics show higher F-N tunneling current density than the pure SiO$_2$ dielectric.
- The F-N tunneling current density is higher in nc-Ge embedded gate dielectric than the nc-Si embedded one.

Simulated Leakage Current

Here it is seen that the incorporation of nanocrystals in the gate oxide somewhat reduces the direct tunneling (leakage) current compared to pure SiO$_2$ gate. Also it is evident that for the nc-Ge the value of the direct Tunneling current is the least.

Simulated I-V Characteristics

- Nanocrystalline particles embedded gate oxide has an F-N tunneling current few decades greater compared to pure SiO$_2$ gate.
- Nanocrystal incorporation markedly reduces the onset voltage of F-N tunneling by ~5V-7V Volts.
- The composite gate dielectric with nc-Ge has a slightly lower value of onset voltage for F-N tunneling compared to the nc-Si embedded one.

Modified Floating Gate Approach

Charging of NCs

\[ \phi_1 = \phi_{10} - \alpha E_{ox}^{1/2} - \beta E_{ox}^{2/3} \]

Leakage from NC to Si

\[ \phi_2 = \phi_{20} - \alpha E_{ncox}^{1/2} \]

Ref:
A. Sengupta, P. Shah, C.K. Sarkar, F.G. Requejo
Adv. Sci. Lett. (Accepted Article)
• Metal Nanocrystals store higher amount of charge.

Simulated Leakage currents

- Metal Nanocrystals offer lesser leakage current compared to Semiconductor ncs.
- Use of High-k dielectrics can further reduce leakage current.
Flat-band Voltage Shift

Flat-band shift simulations show a fair degree of agreement with experimental results.

- Flat-band shift simulations show a fair degree of agreement with experimental results.
nc embedded stacked gate devices show better performance than non-stacked structure.

Si Nanowire / CNT / Fullerene Embedded devices

- CNT / Si NW embedded devices show better performance than nc-Si embedded MOSCAP.
- HfO₂ is the better choice in combination with SiO₂ in stacked tunnel oxide.

Study of Write Voltage variation with increasing volume fraction of the embedded nanomaterials.

Study of charge decay during waiting time for the different structures.

NC embedded MOSFET NVMs

- We also study nc embedded MOSFET NVM devices.
- Au nc was selected for better performance and based on reliability studies.
- We compare Si and In$_{0.3}$Ga$_{0.7}$As substrates.

- The compound semiconductor (In$_{0.3}$Ga$_{0.7}$As) MOSFET NVM shows lesser F-N onset and lesser leakage.
- Write voltages lowered by 3-4 Volts.

• We also simulated the $I_D$-$V_D$ (output) characteristics.
• Compound semiconductor MOSFET shows higher drain currents.
• The simulated results for Si MOSFET NVM match experimental results of Mikhelashvili et. al. [Appl. Phys. Lett. 98, 212902 (2011)].

• We also simulated the HFCV characteristics using the Berkeley Devices Simulator.
• Compound semiconductor MOSFET shows slightly higher value of normalized capacitance.

NC embedded DGMOSFET NVMs

• DGMOSFETs offer better electrostatic control in the channel, than the planar MOS and therefore are becoming more and more popular.
• Most DGMOSFET memories depend on SONOS architecture.
• Nanocrystal embedded dielectric DGMOSFET NVM may be very useful.

• The energy band diagram of a DGMOSFET NVM under a positive gate bias {simulation results}


![Energy Band Diagram](image)
Nc embedded DGMOSFETs offer better write performance than their SONOS DGMOSFET counterparts, Au nc is the better among the two ncs compared. • Improvement of ~2V in terms of write voltage. • Also more charge stored and higher Threshold Voltage (Vth) Shift.
Almost similar magnitude of drain currents in the nc-Si and nc-Au embedded devices.

Threshold Voltage of nc-Au embedded DGMOSFET, slightly higher.

Slight tendency of V_DS de-clamping due to charging of nanocrystals.

We also study GAA (Gate All Around) MOS NVMs. These structures offer the best electrostatic control over the channel among all the advanced MOSFETs (i.e. better than DGMOS, Fin-FET, Π-Gate, or Ω-gate MOSFETs). GAA SONOS memories have been reported as well as recent experimental works on nc embedded gate dielectric GAA MOSFET memory. [Hung. Et al. Appl. Phys. Lett. 98, 162108 (2011)]

We simulated the surface potentials, energy band diagrams, and the write voltages of Si and Au nc embedded gate dielectric GAA MOSFET NVMs.
• Also more charge stored and higher Threshold Voltage (Vth) Shift with nc-Au embedded GAA MOSFET memory device.
• The simulations tally well with experimental results by Hung et. al.
• Nc-Au is also the better performer in terms of charge retention.
• Therefore we may propose the use of nc-Au in nc embedded gate oxide GAA MOSFET NVM.
Conclusions

- MOS NVM devices are extensively used in flash memory based gadgets and computers.
- Floating Gate MOS memory elements mostly employed in flash memory devices.
- Conventional Floating Gate MOS NVMs suffer from leakage, also write voltages need to be lowered.
- Nanocrystals embedded Floating Gate MOS devices apply nanotechnology to improve device performance.
- Nc embedded MOS NVMs show lesser leakage current and lower write voltages compared to conventional MOS NVMs.
- Metal ncs and High-k dielectrics can improve the situation further.
- Nc embedded MOS NVMs may be the memory device of choice in near future.
Thank You

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