Advanced FinFET Process Technology

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Contents

1. Introduction
   • Merits and Issues of FinFET

2. Advanced FinFET Process Technology
   • Vth Tuning
   • Vth Variation

3. Summary
Multi-Gate FinFETs

- Proposed by AIST in 1980 (named “FinFET” by UCB in 1999)
- Ultrathin and undoped channel and self-aligned double gate
- Extremely high short channel effect (SCE) immunity
FinFETs show the smallest DIBL (=highest SCE immunity)
Issues for Advanced FinFET

✓ However, several technological issues still exist...

- Fin Formation
- Variation
- Vth Tuning
- Low Resistive Source/Drain
- Stress Eng.
- (110) Channel
- Compact Model
- C_{\text{para}}
- I/O, ESD
- SOI or Bulk
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$V_{th}$ for FinFETs

- $V_{th}$ has a linear relationship with Gate Workfunction
- For low $V_{th}$, dual metal gate (dual WF) is needed
Almost symmetrical Vth’s (normally off) are obtained thanks to the midgap work function of TiN (4.75 eV)
Dual Metal Gate Integration

General approach:
“Deposition and etching”

This work:
“Metal Inter-diffusion”

For PMOS
→ Mo(4.95 eV)

For NMOS
→ Ta(4.25 eV)/Mo stack
→ Ta Inter-diffusion in Mo
(No metal etching)

Ref. M.M.Hussain et al., ESSDERC2007, p.207
Ta diffusion in Mo

Ta diffuses in Mo and piles-up at Mo/SiO₂ interface after annealing.

Thus WF for NMOS is determined by Ta (4.25eV)
Features of Dual MG FinFETs

- SiO₂ HM etchback in nMOS region
- Ta and SiO₂ HM etchback in pMOS region
- Patterning of Mo and Ta/Mo gates

No metal residue
I-V for Mo and Ta/Mo FinFETs

- For NMOS, low $V_{th}$ can be achieved by Ta diffusion in Mo
- For PMOS, low $V_{th}$ can be achieved by Mo
- Off leakage $\rightarrow$ Negligible

PMOS

Mo (high WF)  

NMOS

Ta (low WF)  

Mo (high WF)

low gate WF by Ta diffusion

$V_{th} = -0.15V$

$V_{th} = 0.26V$

$L_g = 160\text{nm}$, $T_{fin} = 25\text{nm}$ undoped

$V_{dd} = 1\text{V}$

AIST, IEEE EDL 2008
Four-Terminal FinFET

4T-FinFET = Independent DG FinFET

✓ $V_{th}$ for FinFET can be controlled flexibly and individually by separating the DG
DG Separation

CMP Process

SEM Image after CMP

Local Etch-back Process

FinFET Formation and Lithography

DG Separation by LEB

Stopper Fin

Gate

Resist

BOX

Sub

Gate1

Gate2

Fin Top

Source

Drain

Side Wall

100nm
Vth Tuning by Controlling Vg2

- Vth can be tuned from LSTP to HP flexibly by selecting a proper Vg2 (The Second Gate)
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Possible $V_{th}$ Variation Sources

1. Gate Length ($L_g$)
2. Fin Thickness ($T_{Si}$)
3. Oxide Thickness ($T_{ox}$)
4. RDF
5. Work Function WFV ($\Phi_m$)

✓ FinFET variability sources were systematically analyzed
Main Cause of Vth Variation

- Dimension variation sources are negligible
- Main cause of the Vth variation is the Workfunction Variation
Workfunction Variation

- Rough etched side wall causes randomly aligned metal grain and thus higher WF variation
- If side wall is flat, uniformly aligned metal grain and thus lower WF variation can be expected
Nano-Wet Etching Process

Etchant:
2.38% TMAH (Resist Developer) (Tetramethylammonium hydroxide)

Extremely low ER of (111) in TMAH $\rightarrow$ Flat (111) side wall
SEM and STEM images of FinFET

Min. $L_g = 20$ nm, $T_{Si} = 17.8$ nm, $H_{Si} = 45$ nm

Nano-Wet-Etched FinFET

Undoped channel

$T_{ox}(CET) = 2.3$ nm by C-V

Gate Stack : PVD-TiN/SiO$_2$
AIST, VLSI Symp. 2010

Measured $\sigma V_{\text{th}}$ for Nano-Wet-Etched FinFET

$A_{Vt} = 3 \text{ mV}{\mu}\text{m}$

$A_{Vt} = 1.35 \text{ mV}{\mu}\text{m}$

PVD-TiN Gate
CET = 2.3 nm

$\sqrt{1/(WL)}$ [mm$^{-1}$]

$\sigma V_{\text{th}}$ [mV]

$\checkmark$ $A_{Vt}$ was significantly lowered by flattening the side channel
Avt Benchmark

List of reported $A_{Vt}$ values

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- Obtained Avt meets 22-nm-node SRAM requirement
- For 15nm and beyond, Avt should be further reduced
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Summary

- By introducing Ta/Mo dual metal gate technology, low $V_{th}$ ($\pm 0.2V$) can be obtained for CMOS FinFETs.

- By separating the DG, $V_{th}$ can be tuned from 0.2V to 0.4V flexibly.

- Flattening of Si-fin sidewall channel is very promising for reducing $V_{th}$ variations.

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