Nanoelectronic Devices and Integrations on Silicon Platform Today and Tomorrow

Yoshio Nishi
Professor, Electrical Engineering
Director, Center for Integrated Systems
Stanford University

nishi@stanford.edu
URL: http://nanodevice.stanford.edu

TI Tech Talk, November 11, 2011, TI Tech Nagatsuda Campus
Nanostructure Size Scales

- **Nano-scales (nm):**
  - 0.1 nm: Atom Diameter
  - 1 nm: Carbon Nanotube Diameter
  - 10 nm: Single Quantum States
  - 100 nm: Quantum Mechanics Dominant
  - 1,000 nm: Transistor Films
  - 10,000 nm (1.0 mm): Transistor K. Rim (IBM)

- **Mesoscales (μm):**
  - 1 μm: Double Helix
  - 10 μm: Rhinovirus
  - 100 μm: Small Pox Virus
  - 1,000 μm: Bacterium
  - 10,000 μm: Animal Cell
  - 100,000 μm: Human Hair

- **Macro-scales (mil.):**
  - 0.001" (1 mil.):
    - Min. Feature of Microchips (2005)
    - Micromotors

- **Visible Light Range:**
  - 1 mil. (0.001")

- **Quantum Mechanics Dominant**
  - Double Helix
  - Rhinovirus
  - Small Pox Virus
  - Bacterium
Nanoelectronics at large

- Evolutionary “nano”
  super scaled CMOS
  beyond silicon but with silicon
  MEMS/NEMS
- Revolutionary “nano”
  nanodots,
  nanowires/nanotubes
  graphene
  organic/molecular
  spintronics
  topological insulator
  new functional materials for nonvolatile memory
Transistor Scaling

More non-silicon elements added to MOSFET

Source: Intel
1959: 1st **Planar Integrated Circuit**

Robert N. Noyce

Now non-planar 3-Dimensional Devices?
Germanium to Silicon

John Moll: …...the most dominant reason to switch to silicon was its band gap, i.e. large enough to reduce pn junction leakage, yet small enough to be semiconductor at practical temperature range…and the stable oxide as surface passivation and also as diffusion mask for most of group III and V elements…

Now back to Germanium?
Before going further…

What is our track record in predicting the future?
Roadmap in 1965

- By 1980, Silicon IC (meant bipolar IC mostly) will be replaced by functional device based IC’s, i.e. Gunn effect devices.
- Non-volatile memory, MNOS, will be replacing magnetic thin film memory.
- Geometry shrink will continue within foreseeable future.
Roadmap in 1976

- Optical litho will be replaced by e-beam and/or x-ray circa 1985
- Silicon IC will be replaced by GaAs circa 1985
- Bulk CMOS will be replaced by SOS
- Geometry shrink will continue in .7x in every other year
NTRS to ITRS

Slipped schedules by 3-4 years only from 1994 through 1998!!

Lately decided to put everything on the table, keep growing pages!
Moving Power to the Person

- **1960**: Mainframe
  - 1 MIP
  - Bipolar TTL Compilers
  - Submicron CMOS Speech I/O
  - Decanano CMOS Ubiquitous Communications Access
- **1970**: Minicomputer
  - 10 MIPS
  - NMOS CISC MPU SC Memory Networks Databases
  - Ubiquitous Communications
- **1980**: Workstation
  - 100 MIPS
  - CMOS RISC MPU DSP LAN Graphics Symbolic Computing
  - Virtual Reality
- **1990**: PC
  - 1000 MIPS
  - Submicron CMOS Speech I/O Imaging I/O Global & Mobile Connectivity Visualization Megabit Memories Low-cost DSP
  - Mobile Digital Video
- **2000**: Laptop
  - 1 MIP
  - Bipolar TTL Compilers
  - Submicron CMOS Speech I/O
  - Decanano CMOS Ubiquitous Communications Access
- **Handheld**
  - 10 MIPS
  - NMOS CISC MPU SC Memory Networks Databases
  - Ubiquitous Communications

Enabling Technology

- **Bipolar TTL Compilers**
- **NMOS CISC MPU SC Memory Networks Databases**
- **CMOS RISC MPU DSP LAN Graphics Symbolic Computing**
- **Submicron CMOS Speech I/O Imaging I/O Global & Mobile Connectivity Visualization Megabit Memories Low-cost DSP**
- **Decanano CMOS Ubiquitous Communications Access Mobile Digital Video Virtual Reality Gigabit Memories Super DSP VLIW**
The happy scaling: for how long?

dimensions $t_{ox}$, L, W  
1/$\alpha$

doping 
$\alpha$

voltage 
$1/\alpha$

integration density 
$\alpha^2$

delay 
$1/\alpha$

power dissipation/Tr 
$1/\alpha^2$

Smaller = better
Microprocessor Trends

Higher Transistor Count $\times$ Higher Frequency = Higher Power

Moore’s Law hits the power wall

Mark Bohr, EE310 seminar at Stanford 2011
Paradigm Shift: Hitting the Cooling Limit

• Moving a high power chip to the next node (with limitation on cooling and maximum T rise), actually will slow it down

End of frequency scaling @ ~4 GHz (with 100 W cooling)?
Today
**Changed vs Unchanged**

- Scaling down continues, but is closer to the limit
- Driving force switched from “faster clock” to “less power consuming”
- All kinds of “nano” opportunities in evolutionary nano and revolutionary nano.
- Paradigm change for acceptance of “uncommon” materials
- Variety of new applications in non-traditional field, i.e. bio-, medical-, sensing-…

.....*Let’s take a look*....
Can we reduce power consumption at system level?

• Introduction of multi-core system to suppress the needs for aggressive clock frequency
• 3 D integration at package level, die level, wafer level, monolithic 3D…..
• Interconnect
System Performance from Multi-Cores, as simple scaling cannot deliver solution

G. Shahidi, IBM, at ITPC 2007
Can we further reduce power consumption at individual device level?

- Better electrostatics: Steeper sub-threshold slope by FDSOI, double gate FET, Trigate/Fin FET, Tunnel FETs……..
- Better carrier transport: Power supply voltage reduction by higher mobility channel
- DIBL/GIDL reduction: Source/drain/channel engineering and optimization
- Non-volatile memory and logic
90 nm Strained Silicon Transistors

Strained silicon provided increased drive currents, making up for lack of gate oxide scaling

Mark Bohr, EE310 at Stanford 2011
45 nm High-k Metal Gate Transistors

65 nm Transistor

45 nm HK+MG

SiO$_2$ dielectric
Polysilicon gate electrode

Hafnium-based dielectric

**Metal gate electrode** High-k + metal gate
**transistors break through gate oxide scaling barrier**

Mark Bohr, EE310, at Stanford, 2011
MOSFET geometry shrink is facing challenges...

- $V_{\text{inj}}$ continued to increase with strained-Si technology, as if Si became a different material under strain.
- $V_{\text{inj}}$ for sub 20nm should be much higher than strained-Si can give.
- High mobility channel: Getting there ($L_g=10\text{nm}$) and proceeding beyond...

New channel material beyond strained Si
MuGFET Devices

Tri-Gate, FinFET

K. Kuhn, Intel, 2010

C-C Yeh, TSMC, IEDM 2010
Tomorrow
What’s beyond scaling

• Logic devices: Non-silicon solution
  Germanium channel,
  III-V channel
  nano-wire, nanotube, nano-something
  graphene,
  topological insulator (?)

• Memory devices: New functional materials
  RRAM, PCRAM/polymer memory,
  STTRAM
Ge PMOSFETs

- ~80% mobility enhancement over Si universal mobility
**NMOSFETs?**

**Drive Current, Mobility Enhancement**

- **Gate Voltage (V)**
- **Drain Current (A/µm)**
- **Transconductance (A/V)**
- **Effective Field (MV/cm)**
- **Electron Mobility (cm²/V·s)**

- **Ge (100)**
- **no IL Ge(100)**
- **GeO₂ IL; Ge (100)**
- **no IL Ge(111)**
- **GeO₂ IL; Ge(111)**

**V_{ds} = 10 mV, W/L = 100µm/20µm**

Ge(111) has higher mobility – lower m*  
Samples without GeO₂ – poor mobility - interface/coulomb scattering.  
EOT trade off

---

Rapid Melt Growth Method for GeOI

J. D. Plummer (Stanford)

Integration of Si NMOS and GeOI PMOS

Rapid melt growth of Ge in micro-crucible from seed window shows high crystal quality GeOI devices

II-V Transistor Options with DIBL improvement

M. Radosavljevic, Intel, IEDM 2010
If the future were to be in Heterogeneous Structures for CMOS Devices

Active Device Channel:
- Si nMOS with strain + Ge pMOS w or w/o strain
- Ge CMOS w or w/o strain
- III-V nMOS + Ge pMOS
- III-V nMOS + III-V pMOS with strain

On-chip Interconnect:
- Electrical + optical
Non-silicon high mobility channel approaches

- It will fulfill the needs for “higher speed and lower power consumption”
- High mobility materials-gate insulator interface is the biggest issue
- Ge option may provide an opportunity for on-chip optical interconnect; at least for detector, and maybe for transmitter if Ge laser is realized
- Integration density should stay with Si VLSI trend line (ITRS)??
- Preferential application on top of the Si platform looks rational option to go

Question: “What is the barrier which can rationalize such changes?”
Graphene ribbon vs. Carbon Nanotube

- High on/off GNR comparable to ~1.2nm SWNT FETs
- GNR FETs comparable to high performance SWNT FETs (d~1.4-1.5nm) remains illusive

H. Dai, Stanford, 08
New Functional memory Opportunities

• Resistive switching
  Transition metal oxides
  Perovskites
  Conductive bridges in solid state electrolytes
• Phase change
• Spin torque transfer
• Polymer…
RRAM Switching Operation Polarity

Unipolar

Bipolar

Current (mA range)

Voltage (few volt range)

Top electrode

Transition Metal Oxide

Bottom electrode
Ab-initio modeling/simulation approach to
What is the conduction mechanism for the “on” state?

• Metallic filament?
• Vacancy chain?
• Local density of states arising from vacancy distribution or metallic behavior?
• Transport, electronic or ionic?
• Formation energy of conductive path?
• Macroscopic model vs atomic scale model?
Randomly Distributed Vacancies

- Even though we have more vacancies, lowering resistance is not so big as long as vacancies are randomly distributed.
• Filament type conductive channel which is composed of Ti atoms can be formed in either [001] or [110] direction.

S.G. Park et al., EDL, 32, 197 (2011)
**Stability of Vacancy Ordering**

\[ E_{vf} = E(TiO_{2-x}) - E(TiO_2) + n/2E(O_2) \]

- \( E(TiO_{2-x}) \) : The total energy of a supercell containing oxygen vacancies
- \( E(TiO_2) \) : The total energy of a perfect TiO\(_2\) in the same size of supercell
- \( E(O_2) \) : The energy of oxygen molecule
- \( n \) : The number of oxygen vacancy

S.G. Park et al., EDL, 32, 197 (2011)

\[ E_{vf} = E(TiO_{2-x}) - E(TiO_2) + n/2E(O_2) \]
Charged Vacancy ($V_o^{2+}$)

Even though electrons are removed from vacancies, many defect levels are still in the band gap with strong interactions.
Rupture of Conductive Channel

- The conductive channel is disconnected by the diffusion of oxygen into the channel.
Hydrogen in Conductive Channel

- Hydrogen segregated to the vacancy sites - results in the rupture of the conductive channel by localizing electrons in those sites.

S.G. Park et al., VLSI (2011) (accepted)
**Switching Modeling**

- **Initial (Insulator)**
  - $V_o$ concentration
  - Vacancies in random

- **Electroforming**
  - $V_o$ ordered domains

- **On (LRS)**
  - Thermal heating by high current density
  - $V_o$ diffuse out

- **Off (HRS)**
  - Reset
  - The resistance of each state might be determined by the amount of vacancy ordered domains. (It doesn’t have to be Magneli phase.)

- **Set**
Vision for Memory Cell Configuration

Concept: nonvolatile resistive-switching memory

Advantages:
+ $4F^2$
+ 3D
+ MLC
+ Low cost
+ Fast (<1 μs)

Concerns: scaling (reset current) and reliability (data retention, noise, switching variability)
Paradigm Change in Emerging Memory Devices

- *Electrons and holes in stable structures of Si*

- *Electrons and holes in unstable structures* ions, vacancies, structural polarizations etc

- Flood gate opened for new materials with new understanding and knowledge required chalcogenides, perovskite, binary metal oxide, ferromagnetics, ferroelectrics, organic materials, carbon base materials etc
## Metal Oxide RRAM (IEDM/VLSI) 2004-2010

<table>
<thead>
<tr>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>Structure</td>
<td>1T-1R</td>
<td>1T-1R</td>
<td>1T-1R</td>
<td>1T-1R</td>
<td>1T-1R</td>
<td>1T-1R</td>
<td>1T-1R</td>
<td>1R</td>
<td>1R</td>
<td>1R</td>
</tr>
<tr>
<td>Cell Area (um$^2$)</td>
<td>~0.2</td>
<td>~0.03</td>
<td>~0.49</td>
<td>~0.25</td>
<td>~0.1</td>
<td>0.0009 (30nm)</td>
<td>8.1E-5 (9nm)</td>
<td>0.0036 (60nm)</td>
<td>11300</td>
<td>0.0025 (50nm)</td>
</tr>
<tr>
<td>Speed</td>
<td>~5us</td>
<td>~50ns</td>
<td>~5ns</td>
<td>~10ns</td>
<td>~5ns</td>
<td>~300ps</td>
<td>~1us</td>
<td>~50ns</td>
<td>~20ns</td>
<td>~40ns</td>
</tr>
<tr>
<td>Peak Voltage</td>
<td>&lt;3V</td>
<td>&lt;3V</td>
<td>&lt;3V</td>
<td>&lt;2V</td>
<td>&lt;1.5V</td>
<td>&lt;2.5V</td>
<td>&lt;4V</td>
<td>&lt;3V</td>
<td>&lt;3V</td>
<td>&lt;2V</td>
</tr>
<tr>
<td>Peak Current</td>
<td>~2mA</td>
<td>~45uA</td>
<td>~100uA</td>
<td>~170uA</td>
<td>~25uA</td>
<td>~200uA</td>
<td>~1uA</td>
<td>~1mA</td>
<td>~0.1uA</td>
<td>~50 uA</td>
</tr>
<tr>
<td>HRS/LRS Ratio</td>
<td>&gt;10</td>
<td>&gt;10</td>
<td>&gt;90</td>
<td>&gt;10</td>
<td>&gt;1,000</td>
<td>&gt;1000</td>
<td>&gt;10</td>
<td>&gt;10</td>
<td>&gt;700</td>
<td>&gt;10</td>
</tr>
<tr>
<td>Endurance</td>
<td>$10^6$</td>
<td>600</td>
<td>100</td>
<td>$10^9$</td>
<td>$10^6$</td>
<td>$10^{10}$</td>
<td>200</td>
<td>$10^6$</td>
<td>$10^6$</td>
<td>$10^6$</td>
</tr>
<tr>
<td>Retention</td>
<td>300h@150°C</td>
<td>30h@90°C</td>
<td>1000h@150°C</td>
<td>3000h@150°C</td>
<td>10h@200°C</td>
<td>28h@150°C</td>
<td>280h temp. N/A</td>
<td>2000h@150°C</td>
<td>3h@125°C</td>
<td>28h@125°C</td>
</tr>
</tbody>
</table>

**Key enabler - new materials for NVRAM**

<table>
<thead>
<tr>
<th>Yesterday</th>
<th>Today or in view</th>
<th>Under investigation</th>
</tr>
</thead>
</table>

<table>
<thead>
<tr>
<th></th>
<th>I</th>
<th>IA</th>
<th>II</th>
<th>III</th>
<th>IV</th>
<th>VA</th>
<th>VIA</th>
<th>VII</th>
<th>VIIA</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>H</td>
<td>1.008</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>2</td>
<td>He</td>
<td>4.003</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>3</td>
<td>Li</td>
<td>6.941</td>
<td>Be</td>
<td>9.012</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>4</td>
<td>B</td>
<td>10.81</td>
<td>C</td>
<td>12.01</td>
<td>N</td>
<td>14.01</td>
<td>O</td>
<td>16.00</td>
<td></td>
</tr>
<tr>
<td>5</td>
<td>Al</td>
<td>13.40</td>
<td>Si</td>
<td>14.01</td>
<td>P</td>
<td>15.00</td>
<td>S</td>
<td>16.00</td>
<td>Cl</td>
</tr>
<tr>
<td>6</td>
<td>Ar</td>
<td>39.95</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>7</td>
<td>K</td>
<td>39.10</td>
<td>Ca</td>
<td>40.08</td>
<td>Sc</td>
<td>44.96</td>
<td>Ti</td>
<td>47.87</td>
<td>V</td>
</tr>
<tr>
<td>8</td>
<td>Cr</td>
<td>51.99</td>
<td>Mn</td>
<td>54.94</td>
<td>Fe</td>
<td>55.85</td>
<td>Co</td>
<td>58.93</td>
<td>Ni</td>
</tr>
<tr>
<td>9</td>
<td>Cu</td>
<td>63.55</td>
<td>Zn</td>
<td>65.38</td>
<td>Ga</td>
<td>69.72</td>
<td>Ge</td>
<td>72.63</td>
<td>As</td>
</tr>
<tr>
<td>10</td>
<td>Se</td>
<td>78.96</td>
<td>Br</td>
<td>79.90</td>
<td>Kr</td>
<td>83.80</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>11</td>
<td>Na</td>
<td>22.99</td>
<td>Mg</td>
<td>24.31</td>
<td>Al</td>
<td>26.98</td>
<td>Si</td>
<td>28.09</td>
<td>P</td>
</tr>
<tr>
<td>12</td>
<td>S</td>
<td>32.06</td>
<td>Cl</td>
<td>35.45</td>
<td>Ar</td>
<td>39.95</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>13</td>
<td>K</td>
<td>39.10</td>
<td>Ca</td>
<td>40.08</td>
<td>Sc</td>
<td>44.96</td>
<td>Ti</td>
<td>47.87</td>
<td>V</td>
</tr>
<tr>
<td>14</td>
<td>Cr</td>
<td>51.99</td>
<td>Mn</td>
<td>54.94</td>
<td>Fe</td>
<td>55.85</td>
<td>Co</td>
<td>58.93</td>
<td>Ni</td>
</tr>
<tr>
<td>15</td>
<td>Cu</td>
<td>63.55</td>
<td>Zn</td>
<td>65.38</td>
<td>Ga</td>
<td>69.72</td>
<td>Ge</td>
<td>72.63</td>
<td>As</td>
</tr>
<tr>
<td>16</td>
<td>Se</td>
<td>78.96</td>
<td>Br</td>
<td>79.90</td>
<td>Kr</td>
<td>83.80</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>17</td>
<td>Rb</td>
<td>85.47</td>
<td>Sr</td>
<td>87.62</td>
<td>Y</td>
<td>88.91</td>
<td>Zr</td>
<td>91.22</td>
<td>Nb</td>
</tr>
<tr>
<td>18</td>
<td>Mo</td>
<td>95.94</td>
<td>Tc</td>
<td>99.90</td>
<td>Ru</td>
<td>101.10</td>
<td>Rh</td>
<td>102.91</td>
<td>Pd</td>
</tr>
<tr>
<td>19</td>
<td>Ag</td>
<td>107.87</td>
<td>Cd</td>
<td>112.41</td>
<td>In</td>
<td>114.82</td>
<td>Sn</td>
<td>118.71</td>
<td>Sb</td>
</tr>
<tr>
<td>20</td>
<td>Te</td>
<td>127.60</td>
<td>I</td>
<td>126.90</td>
<td>Xe</td>
<td>131.30</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>21</td>
<td>Cs</td>
<td>125.80</td>
<td>Ba</td>
<td>137.30</td>
<td>La</td>
<td>138.90</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>22</td>
<td>Ce</td>
<td>140.11</td>
<td>Pr</td>
<td>140.91</td>
<td>Nd</td>
<td>144.24</td>
<td>Eu</td>
<td>152.00</td>
<td>Gd</td>
</tr>
<tr>
<td>23</td>
<td>Tb</td>
<td>158.93</td>
<td>Dy</td>
<td>162.50</td>
<td>Ho</td>
<td>164.93</td>
<td>Er</td>
<td>167.26</td>
<td>Tm</td>
</tr>
<tr>
<td>24</td>
<td>Yb</td>
<td>173.04</td>
<td>Lu</td>
<td>176.63</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>25</td>
<td>Th</td>
<td>232.03</td>
<td>Pa</td>
<td>231.04</td>
<td>U</td>
<td>238.03</td>
<td>Np</td>
<td>237.04</td>
<td>Pu</td>
</tr>
<tr>
<td>26</td>
<td>Am</td>
<td>241.01</td>
<td>Cm</td>
<td>244.06</td>
<td>Bk</td>
<td>247.07</td>
<td>Cf</td>
<td>251.07</td>
<td>Es</td>
</tr>
<tr>
<td>27</td>
<td>Fm</td>
<td>255.08</td>
<td>Md</td>
<td>254.09</td>
<td>No</td>
<td>258.04</td>
<td>Lr</td>
<td>257.04</td>
<td></td>
</tr>
</tbody>
</table>
After passing the test at “device” level..

Integration!!
CMOS Technology Based Products in mid 2000s

- 2Gb DRAM, SAMSUNG
- 8Gb NAND, SAMSUNG
- 70 Mb SRAM, INTEL
Likely “Road Block” for all of “nano” or “novel” materials

“Variability”
“Reproducibility”
“Integration”

Are we ready?? Perhaps “Not yet”!
However, this is not the first time......
MOSFET in early 60’s

I can make the same numbers of PhDs as the number of MOSFETS I make!

This is a great toy for 2D quantization!

Integration!? No way!

Those are, however, in the situation where we had only Si, SiO2 and Al!
So, this is truly an exciting era for young bright people with tons of challenges ahead!
Technology & Topics in 60’s

- Silicon replaced germanium, *Ge again*
- Self-aligned silicon gate from Intel/Fairchild, *Back to metal gate*
- Silicon VLS, *Nanowires of Ge, III-V etc*
- Dielectric breakdown of insulators *ReRAM*
- Ionic impurity in SiO$_2$ *CBRAM*
- Ovonic devices became popular after their press release in ’69, *phase change memory*
New Technology & Topics in 70’s

- Si CMOS, **CMOS with non-silicon channel**
- SOS viewed as the major break through, **SOI**
- Ovonic devices became popular after their press release in ’69, **phase change memory**
- Strained channel physics in SOS, **Strained silicon MOS**
- Soft X-ray lithography and e-beam lithography, **EUV lithography**
Future Technology Directions

New Applications
- Digital + analog + optical
- Silicon + III-V
- Electrical + Mechanical

New Technologies
- Carbon Based?
- Spintronics?
- Magnetic Domains?
- Molecular Switches?

New device technology will be needed by 2020

Mark Bohr, EE310 seminar at Stanford, 2011
Summary

• Si as the dominant design in the past 3 decades because of cost/bit or logic superiority
• High speed switch may end up using non-silicon channel for better power-speed advantage, while traditional memory may be replaced with new material based nonvolatile memory only if they are integrated on silicon platform
• Potential road blocks
  variability
  reproducibility
  integration
• Colleagues at Stanford: Krishna Saraswat, Philip Wong, Simon Wong, Paul McIntyre and Bruce Clemens for discussions and sharing some of their slides

• Friends in industry: Mark Bohr, Ghavam Shahidi, Hans Stork, M. Brillout

• Nishi group students and research staff members

INMP, NMTRI, CIS, MARCO, SRC, NSF, INTEL, IBM, TOSHIBA, TI, Samsung, Hynix, AMAT, TEL...

Thank you!!