NANOELECTRONICS AS INNOVATION DRIVER FOR A GREEN SUSTAINABLE WORLD

Cor Claeys
TECHNOLOGY IN EVERY ASPECT OF OUR LIFE
SMART PHONE
EASY TO USE INNOVATIVE APPS
54 MILLION UNITS IN 2011

208 MILLION BY 2014

2011 EXPLOSION TABLET PC
SMARter MOBILITY
ROAD VIEW TRANSMITTING SYSTEM
KEEP INCREASE OF THE NUMBER OF COMPONENTS.
COST PER COMPONENTS DECREASES!

Integrated Circuit Complexity

Transistors Per Die

- 1965 Actual Data
- MOS Arrays
- MOS Logic 1975 Actual Data
- 1975 Projection
- Memory
- Microprocessor

More Moore
TECHNOLOGY ROADMAP: STRATEGIC AGENDA

- More than Moore: Diversification
- CNT, nanowire, TFET
- Graphene
- Quantum computing
- Spintronics
- Polymer electronics

Beyond CMOS

More Moore: Miniaturization

Baseline CMOS: CPU, Memory, Logic

130nm
90nm
65nm
45nm
32nm
22nm

Information Processing

Digital content System-on-chip (SoC)

Other Value Systems
SCALING HAMPERED BY LEAKAGE CURRENTS

1. Subthreshold leakage
   - Shorter channel lengths
   - Threshold voltage not scaling as fast as $V_{DD}$

2. Gate oxide leakage or Tunneling current
   - As oxide thins down, leakage increases exponentially

Need new materials and/or new architectures!
TACKLING THE POWER PROBLEM

Solution → New Material
e.g., High-K dielectric
TACKLING THE POWER PROBLEM

Gate Leakage

Solution → New Material
e.g., High-K dielectric

Sub-$V_T$ Leakage

Solution → New Architecture
e.g., Fully Depleted Devices for better Short-Channel control
TRANSISTOR SCALING

New process modules

New materials

New device concepts

90-65-45
Strain, USJ

45-32
High-k, Metal Gate

32-22-16
Non-planar devices

Front End

time

>=130

C-COE PICE, TOKYO, OCTOBER 4, 2011 C. CLAEYS
STRESS ENGINEERING : A DRIVING FORCE

90nm
- e-SiGe + tCESL
- (100)/[100] + tCESL

65nm
- SMTx1
  - e-SiGe + tCESL
  - (100)/<100> + tCESL
  - DUAL CESL

45nm
- SMTx2
  - e-SiGe + tCESL
  - e-SiGe + DUAL CESL
  - DUAL CESL
  - SPT
    (Stress Proximity Technique)

32nm
- SMTx3
  - e-SiGe + tCESL
  - e-SiGe + DUAL CESL
  - DUAL CESL
  - SPT
    (Stress Proximity Technique)
  - Surface Engineering:
    (110)/<110> pMOS;
    (100)/<100> nMOS
  - e-SiC

Stress engineering does not solve the power problem!
TRANSISTOR SCALING

New process modules
New materials
New device concepts

Front End

Silicide

USJ

strain

90-65-45

Strain, USJ

time

=130

High-k, Metal Gate

45-32

32-22-16

Non-planar devices

16 and......

New process modules
New materials
New device concepts

C-COE PICE, TOKYO, OCTOBER 4, 2011     C. CLAEYS
Ge PMOS

This work:
- $I_{ON} = 478 \mu A/\mu m$
- $I_{OFF} = 37 nA/\mu m$

65nm Ge pFET

J. Mitard et al., IEDM 2008, p. 873
Ge PMOS – INTERFACE ENGINEERING

HfO₂

Thin SiO₂

Two Si ML

Ge

HfO₂

SiOₓ layer

Si

Ge

10 nm
Cross-sectional TEM images of a high-k gate stack on a Ge surface passivated by different thicknesses of Si. At 12 MLs of silicon, the layer relaxes, giving rise to misfit dislocations at the interface.
HIGH-MOBILITY GE-BASED IMPLANT-FREE QUANTUM WELL DEVICES

2nd generation SiGe QW with additional eSiGe S/D booster achieved extremely **high performance** ($I_{on} = 1\, mA/\mu m$) combined with intrinsically **superb Short-Channel control** (DIBL ~ 130mV/V, Lg ~ 30nm).
### CMOS WITH HIGH-MOBILITY CHANNEL MATERIALS

S. Takagi, The University of Tokyo, INC4 2008

<table>
<thead>
<tr>
<th></th>
<th>Si</th>
<th>Ge</th>
<th>GaAs</th>
<th>InP</th>
<th>InAs</th>
<th>InSb</th>
</tr>
</thead>
<tbody>
<tr>
<td>electron mob.</td>
<td>1600</td>
<td>3900</td>
<td>9200</td>
<td>5400</td>
<td>40000</td>
<td>77000</td>
</tr>
<tr>
<td>(cm²/Vs)</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>electron effective mass (/m₀)</td>
<td>m₁: 0.19</td>
<td>m₁: 0.916</td>
<td>m₁: 0.082</td>
<td>m₁: 1.467</td>
<td>0.067</td>
<td>0.082</td>
</tr>
<tr>
<td>hole mob.</td>
<td>430</td>
<td>1900</td>
<td>400</td>
<td>200</td>
<td>500</td>
<td>850</td>
</tr>
<tr>
<td>(cm²/Vs)</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>hole effective mass (/m₀)</td>
<td>m₃H: 0.49</td>
<td>m₃L: 0.16</td>
<td>m₃H: 0.28</td>
<td>m₃L: 0.044</td>
<td>m₃H: 0.45</td>
<td>m₃L: 0.082</td>
</tr>
<tr>
<td>band gap (eV)</td>
<td>1.12</td>
<td>0.66</td>
<td>1.42</td>
<td>1.34</td>
<td>0.36</td>
<td>0.17</td>
</tr>
<tr>
<td>permittivity</td>
<td>11.8</td>
<td>16</td>
<td>12</td>
<td>12.6</td>
<td>14.8</td>
<td>17</td>
</tr>
</tbody>
</table>

- Ge has lightest hole m* \( \Rightarrow \) good for pMOS
- Many III-V materials have light electron m* \( \Rightarrow \) ideal for nMOS

**Combination of high mobility III-V nMOS and (strained) Ge pMOS integrated on Si substrate for ultimate CMOS performance**

![CMOS with high-mobility channel materials diagram](image-url)
A wide range of materials could be grown on a Silicon wafer with Ge as an intermediate material to achieve low defect-density III-V Silicon

- Most interesting candidates: GaAs, InGaAs, InAs, …..
Demonstration of:
- Common gate stack for IIIV & Ge based devices
- Selective IIIV integration, directly on Silicon substrate
- Issue left of Dit @ interface IIIV – gate stack
SELECTIVE EPI GROWTH OF Ge AND III/V AFTER STI

- Selective growth of Ge epi after STI formation on Si wafer
  - Low defect densities obtained after proper annealing
  - Provides flat surface that allows further scaling of transistor gate length

- Good quality selective growth of thin (In)GaAs on Ge demonstrated
  - No large defects or dislocations can be observed by TEM
Local selective growth after STI allows integration of Ge and III/V materials on Si wafers, also for FinFET's.

- confined growth to grow materials with high lattice mismatch to Si, $>> t_c$
MULTI-GATE STRUCTURES

“1 Gate”

“2 Gates”

“3 Gates”

“Gate-all-Around”

Gate

Source

Drain

Box

Polysilicon Gate

Silicon Fin

Buried Oxide

Source

Gate

Drain
MATERIALS AND DEVICES

SRAM

Strained Si
High-k
Metal gate
Multi gate

FINFET

poly-Si

Fin
SRAM CELL SIZE ROADMAP

- 2nd generation FinFET-based 22nm SRAM cell (10% smaller)
- ... and already gearing for 16nm!
CONCEPTS FOR FULLY DEPLETED CHANNEL

Thin body channel (<10nm)

2nd Gate (FinFET)
Buried Oxide (UTB-SOI)
High-bandgap + QW

FinFET
UTBox-SOI
Quantum Well
EXPLORATORY CONCEPTS

Tunnel FET

Graphene FET
DEVICES WITH REDUCED POWER CONSUMPTION

- Improved subthreshold slope devices can have high $I_{ON}/I_{OFF}$ ratio at low switching voltage → reduced supply voltage and power consumption
  - For carrier transport limited by thermionic emission over a barrier: $d\psi_S/d(\log_{10}I) \approx 60 \text{ mV/decade}$ at room temperature

- TunnelFET basic idea: *use the band-to-band tunneling as an energy filter to overcome the 60mV/decade subthreshold slope limitation*
  - ON/OFF switching determined by band-to-band tunneling at source side
CHOICE TFET MATERIAL: EFFECT OF BANDGAP

- tunneling probability $\sim (E^2 m_r^{1/2} E_g^{-0.5} \exp(-A E_g^{1.5})$

$E_{g, Si} = 1.12 \text{ eV}$
$E_{g, Ge} = 0.66 \text{ eV}$

- $I$-$V$ curves show:
  $I_{ds, Ge} \approx 100 I_{ds, Si}$

- smaller bandgap improves tunneling, but want silicon-based

Remark: Ge TFET-curve is shifted to the left for easier comparison
COMPLEMENTARY HETERO-STRUCTURE TFETS

Ge-source n-TFET  InAs (In_{0.6}Ga_{0.4}As) -source p-TFET

V_{DD} \sim 0.25V ("Green" Transistor)

Literature

TFET

Mayer et al., IEDM (2008)

FinFET

Leonelli et al., SSDM (2009)

Nanowires

Vandooren et al., VLSI Workshop (2009)

Vertical

Gate

Source

Bhuwulka et al., IEEE TED (2004)

Gate

Drain

Source

Vandooren et al., VLSI Workshop (2009)

Gate

Drain

Gate

Source

Drain

Gate

Source

Nanowires

Vandooren et al., VLSI Workshop (2009)
TUNNEL FET BASED ON NANOWIRES

- Possible implementation of Tunnel FETs using etched nanowires

- Templated and constrained growth of nanowires

Growth can be performed partially or fully constrained, with or without catalyst.
III-V AND GRAPHENE TFETS

Tunneling // to the gate oblique to the gate field

Tunneling ⊥ to the gate in-line with the gate field

Tunnel transistors geometries

nanowire TFET
gate-all-around - best electrostatics

graphene nanoribbon (GNR) TFET
$n$ and $p$ channel currents commensurate

A. Seabaugh – ESSDERC 2011
0D

Fullerenes
Curl, Kroto & Smalley 1985
Nobel prize 1996

1D
Carbon nanotubes
Multi-wall 1991
Single-wall 1993

2D
Graphene
2004
Geim, Novoselov
Nobel prize 2010

3D
Graphite
XVI century
“Classical” field-effect approach

- Top and bottom gates
- Ion/Ioff ratio ~10 at 300K

Cannot switch it off!

CNT INTERCONNECTS

- CNT exhibit enhanced electrical and thermal properties over Cu
  - Current capacity:
    - Cu ~ $10^6$ A/cm²
    - CNTs ~ $10^9$ A/cm²
  - Thermal conductivity:
    - Cu ~ 400 W/m.K
    - CNTs ~ 5000 W/m.K

- High-density of MW CNT obtained with Fe on Ti
  - Approaches density needed for interconnects ~$10^{12}$ MWCNT or ~$10^{13}$ cm⁻² CNT shells
    - Outer diameter of 6.5 – 8.0 nm (with 7-10 sheets), inner diameter ~ 5nm

- Carpet of densely aligned CNT
  - XRR 0.43 g/cm³
  - ~$10^{12}$ CNTs/cm²
  - 650°C*
  - 36 µm
  - 10 µm
Nano-bio vision: bio and ICT meet at the nanoscale

BIOTECH

NANOTECH

NANOELECTRONICS

Nano building stone

Water, Glucose, Antibody, Virus, Bacteria, Cancer cell, A period, Tennis ball

Nanometers

$10^{-1}$, 1, $10^2$, $10^3$, $10^4$, $10^5$, $10^6$, $10^7$, $10^8$

nm, µm, cm

x $10^9$

Chip
**ARTIFICIAL SYNAPSE** = functional interface allowing **bi-directional communication** between a neuron and an integrated circuit = neurons-on-chip

![Artificial Synapse Image]
A MEDICAL LAB OF ONLY 1X1 cm²

Detection platforms for low concentrations of disease molecules:

- Fast
- Easy to use
- Cost effective
ORGANIC MICROPROCESSOR
1971: Intel 4004
First Si μProc.
10 μm
4 bit
pMOS
-15V Vdd
2300 TOR
108 KHz

2011: imec & Holst
First plastic μProc.
5 μm
8 bit
pMOS, dual Vt
-10V Vdd
2000 TOR
6 Hz

Courtesy P. Heremans
Photovoltaics: IMEC's terrestrial solar cells roadmap

- Thick (>180µm) bulk Si
  - Single X ⇒ Multi X

- Thin-film c-Si < 20 µm
  - Epitaxial cells
  - Cells on ceramic/glass

- Fully organic
  - Thin-film cells for large-scale power generation

Organic cells for consumer applications

Achievable direct cost module level (€/W_p)

- 2.7-3.5 300µm multi
- 1.3-1.5 150µm multi
- 1.1-1.3 Thin ribbon
- 0.5-1.0 Thin-film
- < 0.5 Organic cells

- Near-term
- Intermediate term
- Long term
ORGANIC SOLAR CELLS
EFFICIENCIES ABOVE 5%
MULTI-JUNCTION SOLAR CELLS: STATE-OF-THE-ART (WORLDWIDE)

Record conversion efficiencies obtained (32% under 1 sun, 40.1% under concentration)

Key technologies:

- current matching of top and middle cell
- wide-gap tunnel junction
- exact lattice matching (1% Indium added in GaAs cell)
- InGaP disordering
- Ge junction formation
GaN ON Si FOR LOWER COST POWER & LED DEVICES

GaN growth on Si

Power HEMTs

LEDs

Thickness (nm)

Vds=60V

12W

19dB

Pout(dBm), GP(dB), PAE(%)

TDD reduction

Si, N, IL

GaN

AlGaN intermediate layers

0.5 μm

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GaN FOR POWER CONVERSION AND SOLID-STATE LIGHTING
CMORE

MEMS

Bio-
Electronic
Interface

RF
BiCMOS

CMOS

Photonics

Thermal
sensors

Chemical
sensors

Optical
detectors