IBM Research

On SOI CMOS as Technology Platform for SoC and Hybrid Device and Function Integration

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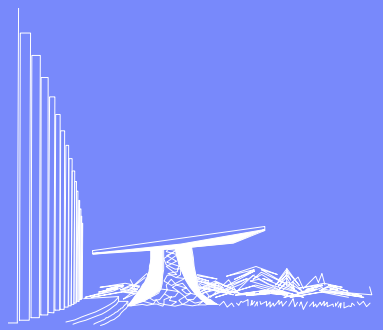
Presented at IS-AHND 2011
Tokyo Institute of Technology, Tokyo, Japan

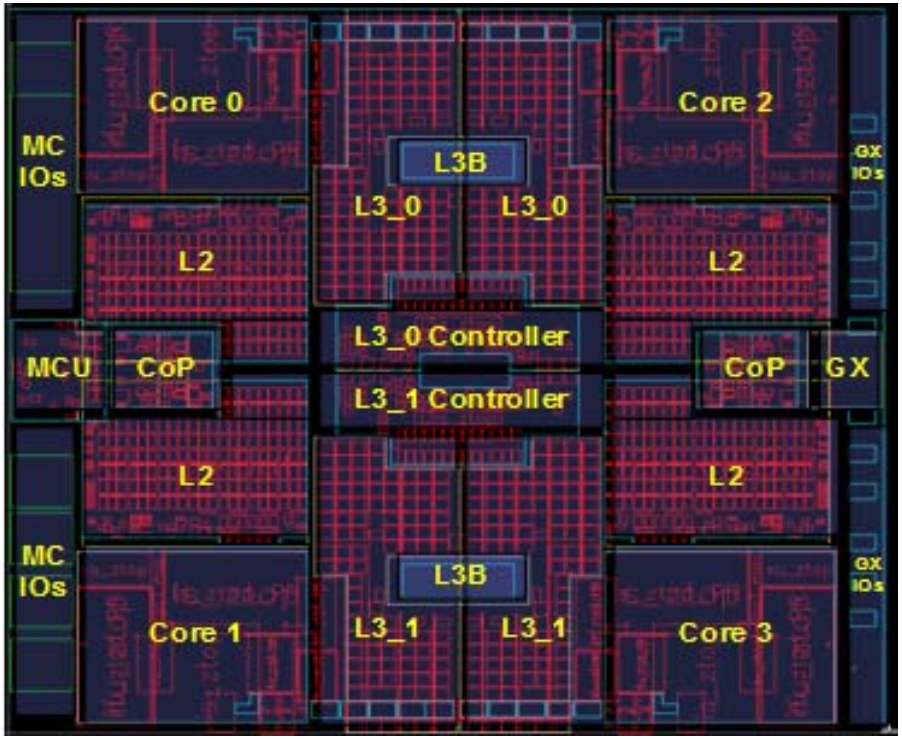


Outline

- CMOS Platforms
  - Bulk silicon
  - Silicon on insulator (SOI)
- Considerations for SoC Functions and Embedded Hybrid Devices
- Examples of SOI-Enabled Embedded Devices and Functions
- Summary

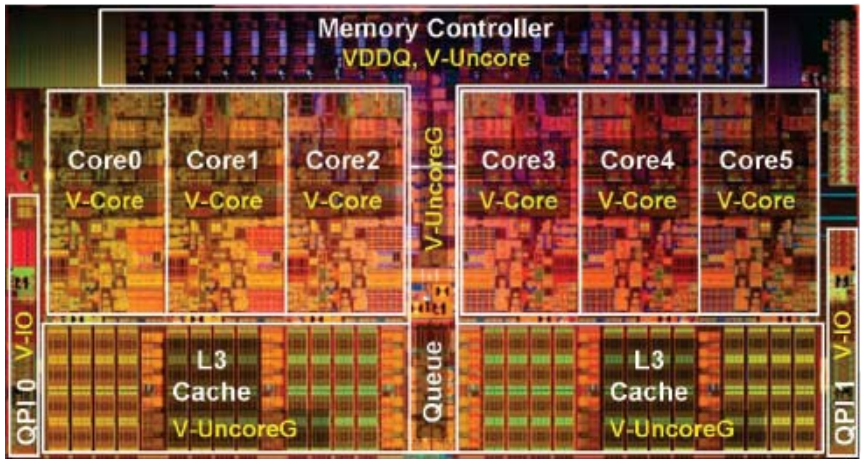
CMOS in Systems Today

SOI CMOS



IBM's 45 nm 4-core 5.2GHz z196

Bulk Silicon CMOS



Intel's 32 nm 6-core Westmere

A 45SOI vs. 45LP CMOS Design Comparison

Conclusion

- ARM1176 design and silicon implementation with standard commercial EDA flow using SOI physical IP
  - Standard cell library
  - Single-port SRAM compiler
  - GPIO
  - PLL
- Silicon demonstration of high-performance and low-power capability of 45SOI vs 45LP
  - 40% power reduction at 500MHz
  - 20% higher speed with still 28% power reduction
  - 1GHz achievable with same implementation
  - Static power reduction at room temperarure may be achieved with power management techniques

13 The Architecture for the Digital World® ARM

Source: R. Pottier et al, ARM_IMEC SOIConf 2009

System-on-Chip and Hybrid Integration

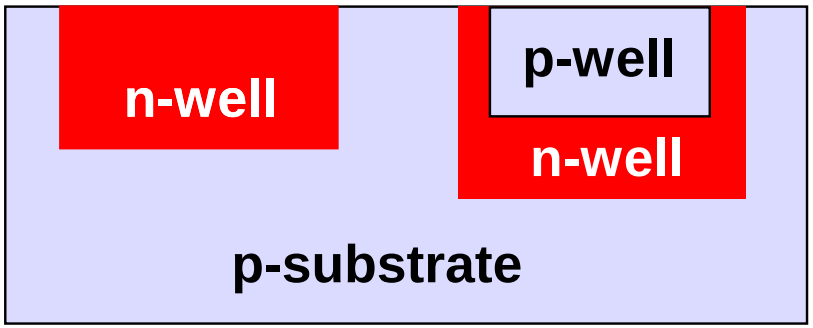
- **Why?**
  - **The ultimate goal in *INTEGRATED-CIRCUIT* technology**
  - **Higher performance and/or lower power dissipation, ideally at lower cost**
- **What devices and functions to integrate?**
  - **Integration of CPU and cache memory already routine**
  - **Devices and functions to be developed and integrated on chip ➔ whatever the system designers need to deliver winning products to their customers**

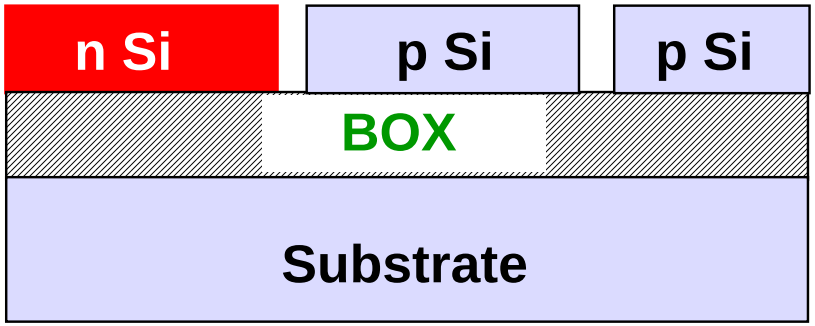
What Devices and Functions to Integrate, and How?

- **What?**
  - **From TSMC website: "No longer is a logic focused process technology able to meet all market requirements. Rather, today's industry innovator requires special feature technologies such as mixed-signal/RF, embedded high density memory, non-volatile memory, high voltage devices and CMOS image sensor technologies."**
- **How?**
  - **Integrate these and other devices and functions, as many as reasonable from a system product cost, performance, and power dissipation perspective**

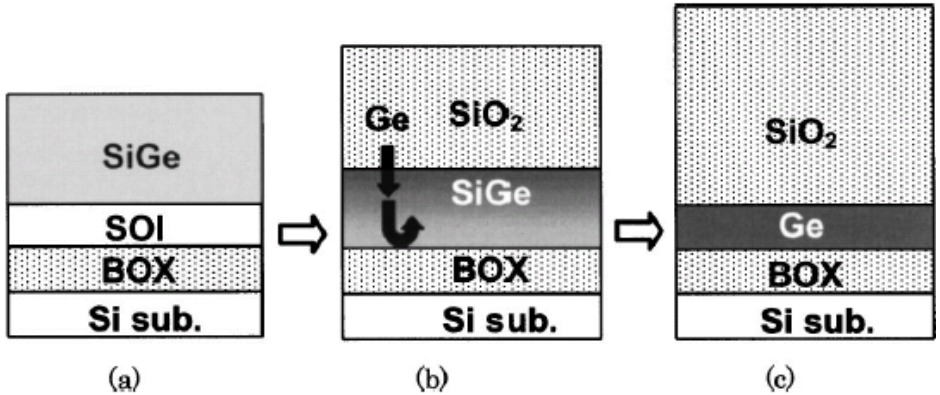
Electrical Isolation – a Major Challenge in Integration

- **Bulk silicon CMOS**
  - Isolation by doped well regions
  - Large area
  - Large parasitic capacitance
  - Less complete isolation; isolation noise
- **SOI CMOS**
  - Isolation by BOX and oxide filled shallow trenches
  - Isolation feature size small and scalable
  - Small parasitic capacitance
  - Isolation noise can be small; especially with “substrate” engineering



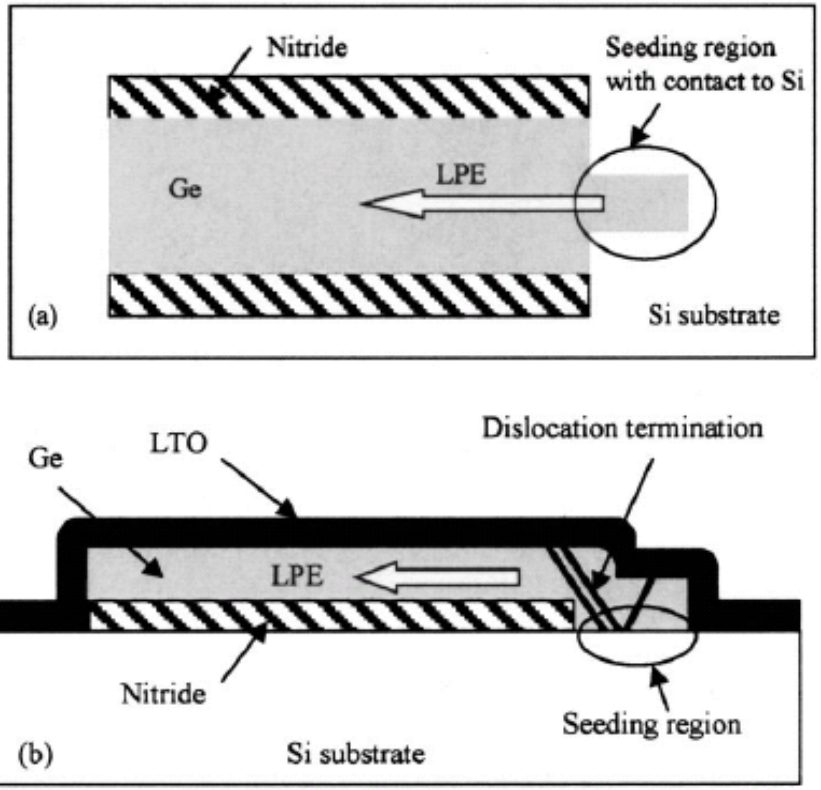


Ge on Insulator



Ge condensation by oxidation

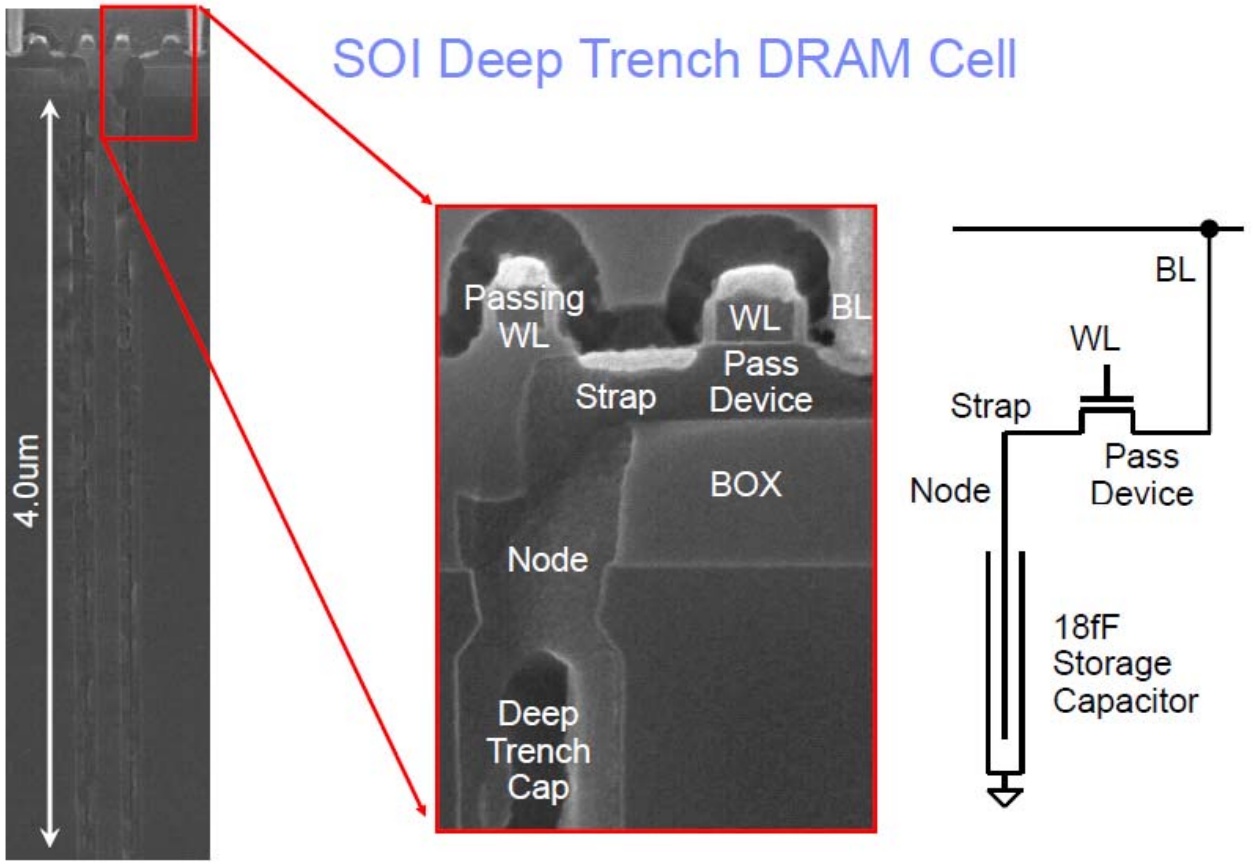
Ref: S. Nakaharai et al., APL vol. 83, p. 3516 (2003)



Growth by liquid phase epitaxy

Ref: Y. Liu et al., APL vol. 84, p. 2563 (2004)

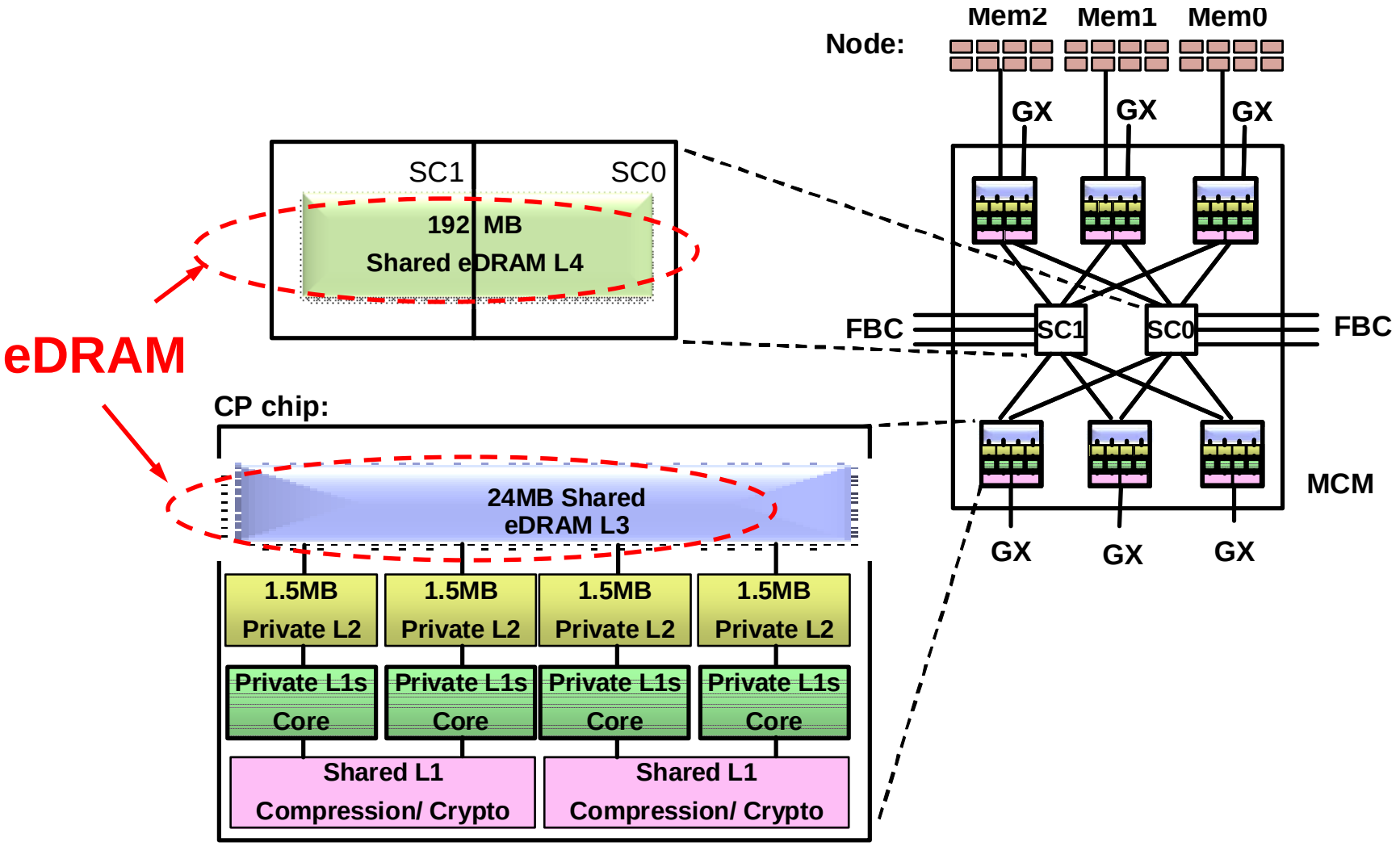
eDRAM in High-Performance SOI Microprocessors



- **45nm SOI processors for IBM's Power7 servers and z196 mainframes**

Reference: J. Barth et al., 2010 ISSCC

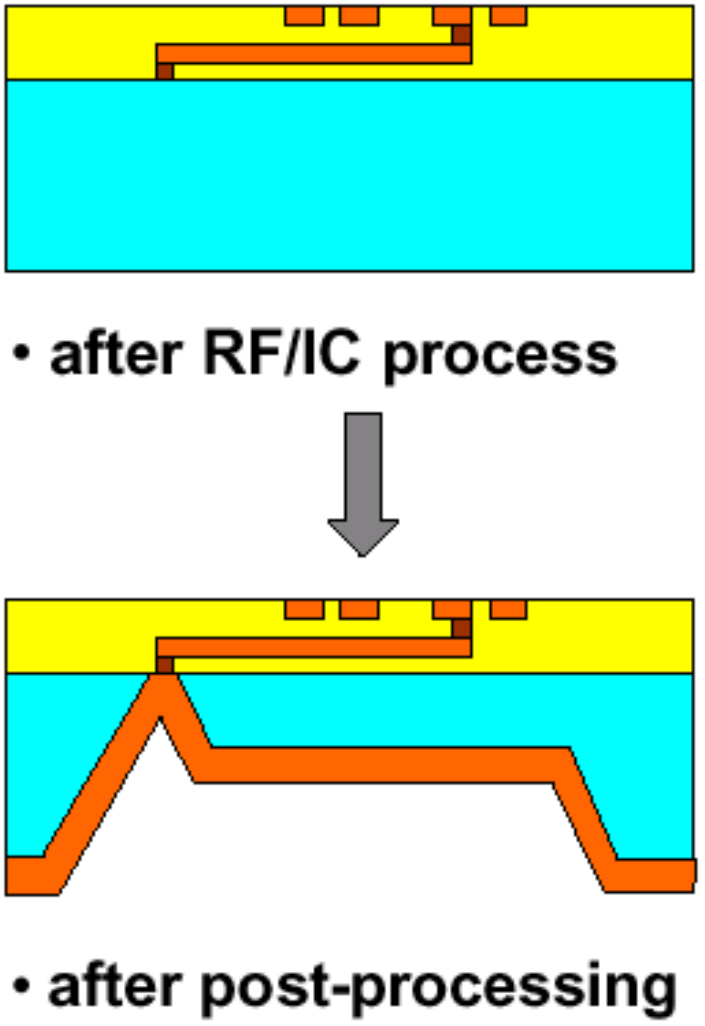
Z196 (IBM Mainframe) Cache / Node Topology



Source: B. Curran, HOT CHIP Conference, Aug. 21, 2010

Substrate Engineering for RF

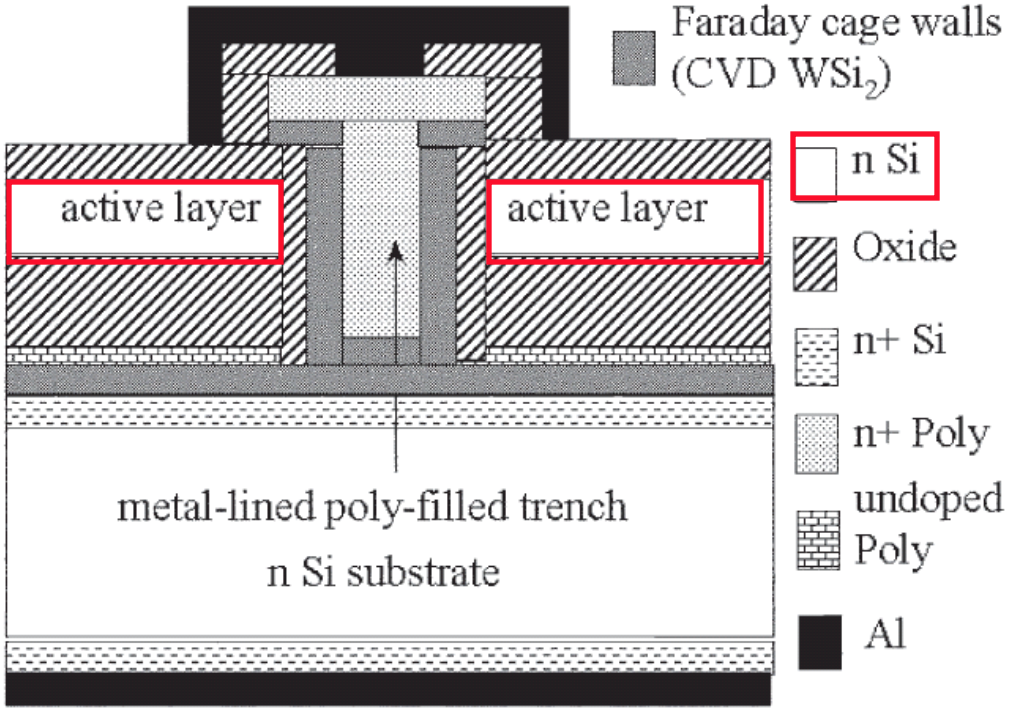
- **SOI substrate can be engineered to meet system requirement**
  - **High resistivity**
  - **Patterned doped regions**
  - **Etched and/or processed**
  - **...**



Reference: J. Burghartz et al., 2002 BCTM

Substrate Engineering for Crosstalk Reduction

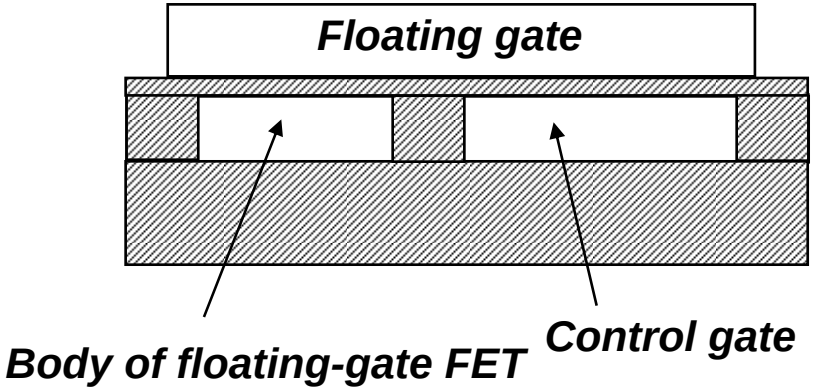
- **Ground-plane with Faraday cage**
  - **"Over ten times reduction in crosstalk is demonstrated up to 10 GHz, compared to previously reported substrate crosstalk suppression technologies."**

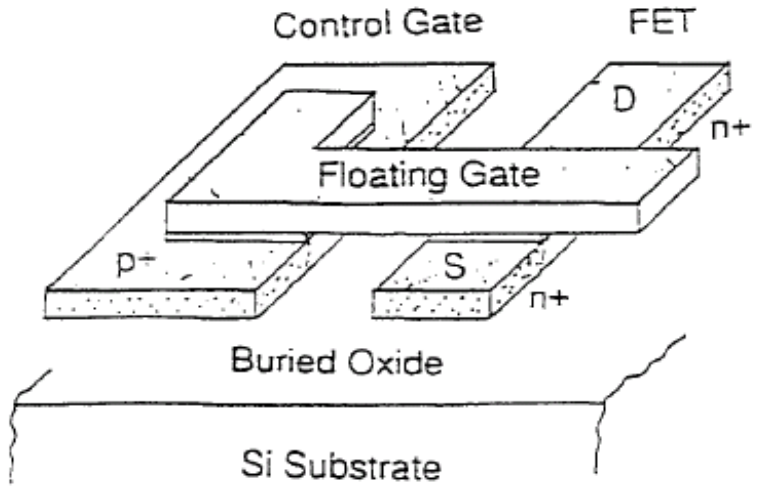


Reference: S. Stefanou et. al., IEEE TED, p. 486 (2004)

Single-Poly Embedded EEPROM in SOI

- **Silicon body layer used as control gate**
- **Only requirement is a thick Tox for floating-gate operation**





References: Acovic, Ning and Solomon, US Patent 5,886,376;
Solomon and Su, 15th IEEE NVRAM Workshop, paper 4.2, 1997.

Single-Poly Embedded EEPROM in SOI

- ***Experimental data based on SOI CMOS with Tox = 4.5 nm***

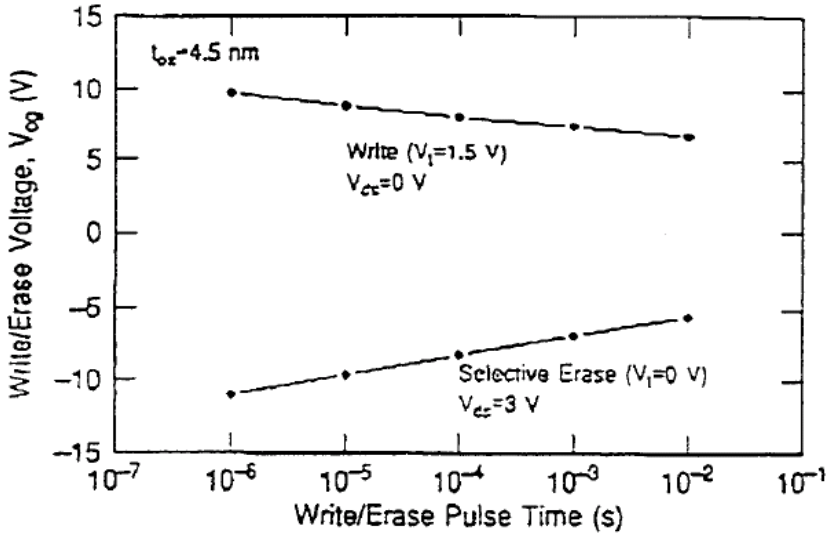


Figure 5. Write/erase threshold voltage vs. pulse time.

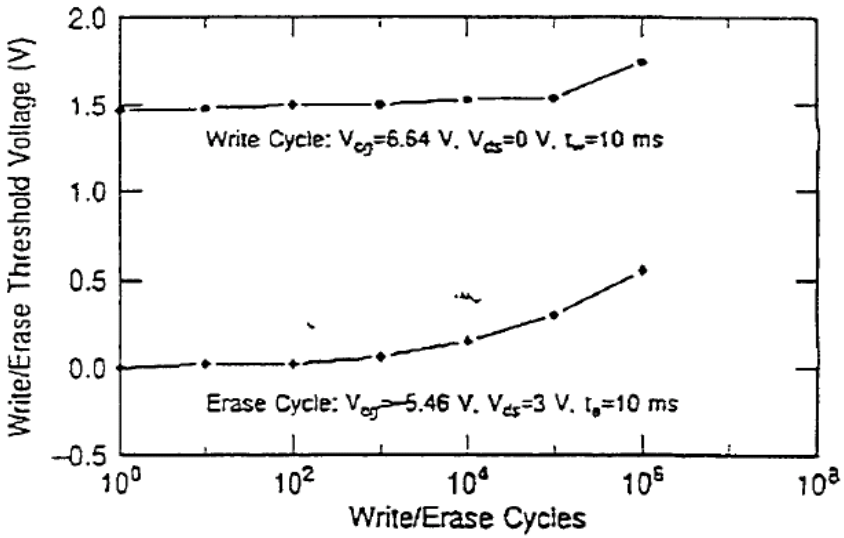
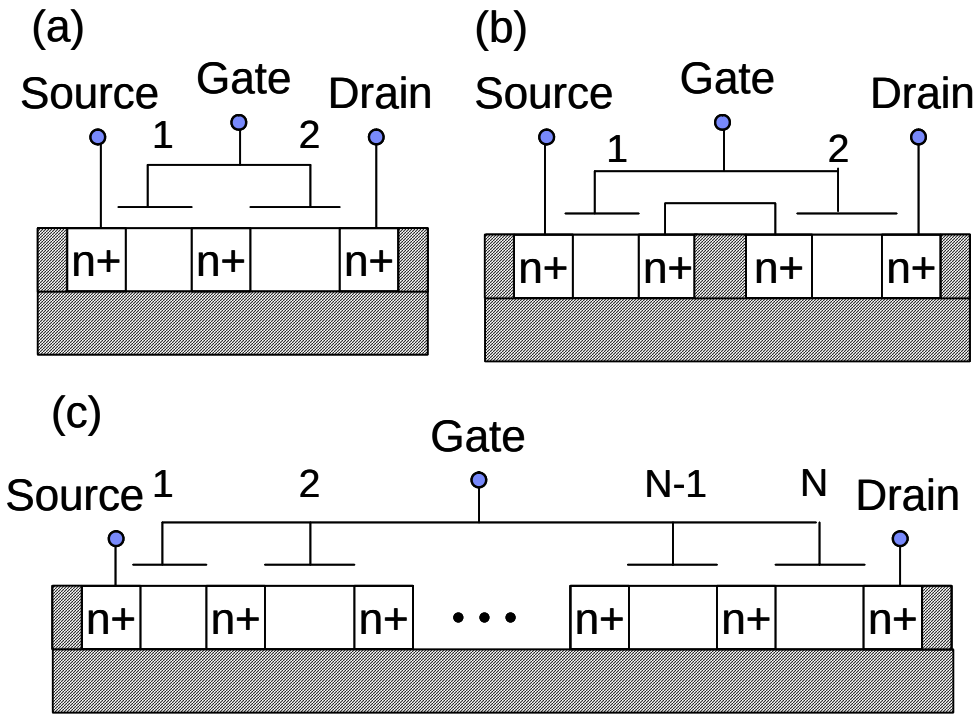
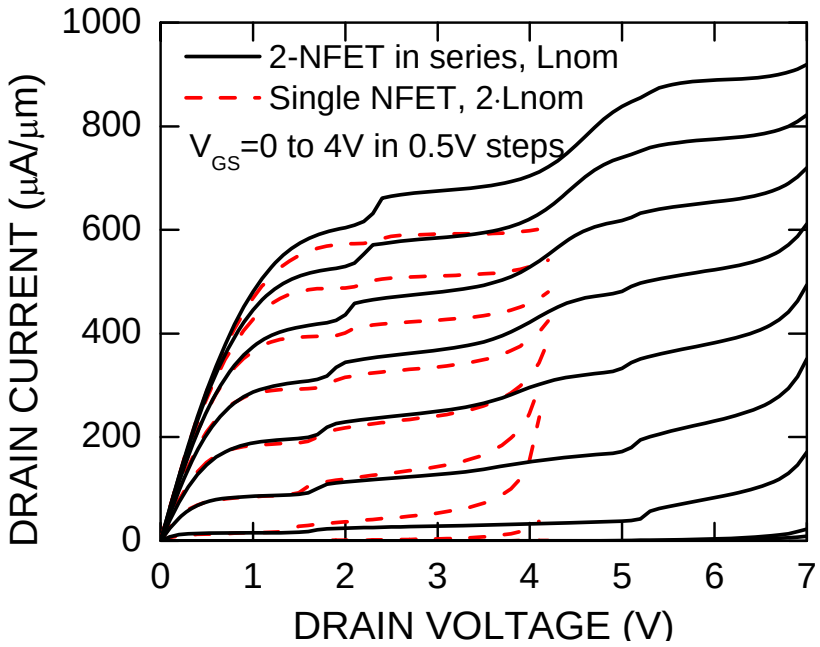


Figure 6. Write/erase threshold voltage vs. number of cycles.

References: Solomon and Su, 15th IEEE NVRAM Workshop, paper 4.2, 1997.

SOI Series-Connected (Stacked) FETs

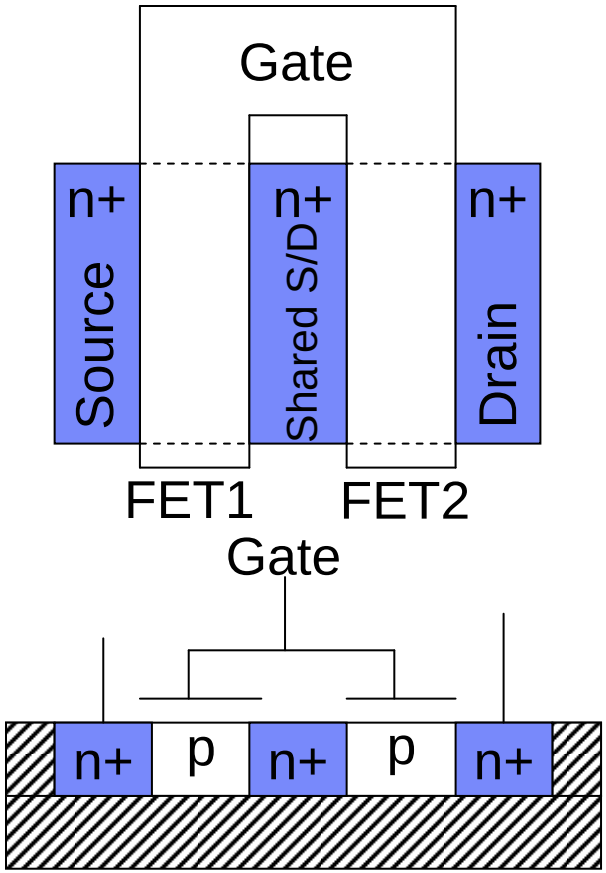


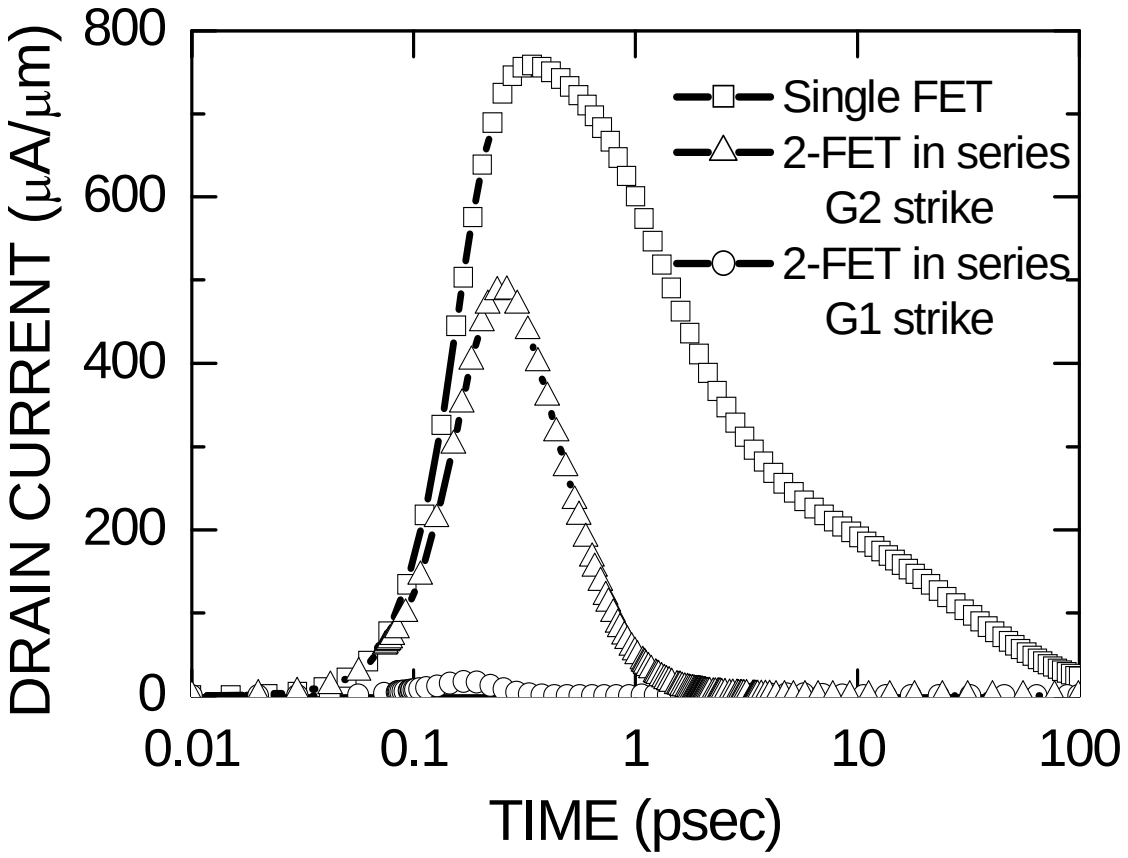


- **Stacked device for high voltage and for soft-error immunity**

Reference: J. Cai et al., 2008 IEEE Int. SOI Conference, pp. 21-22

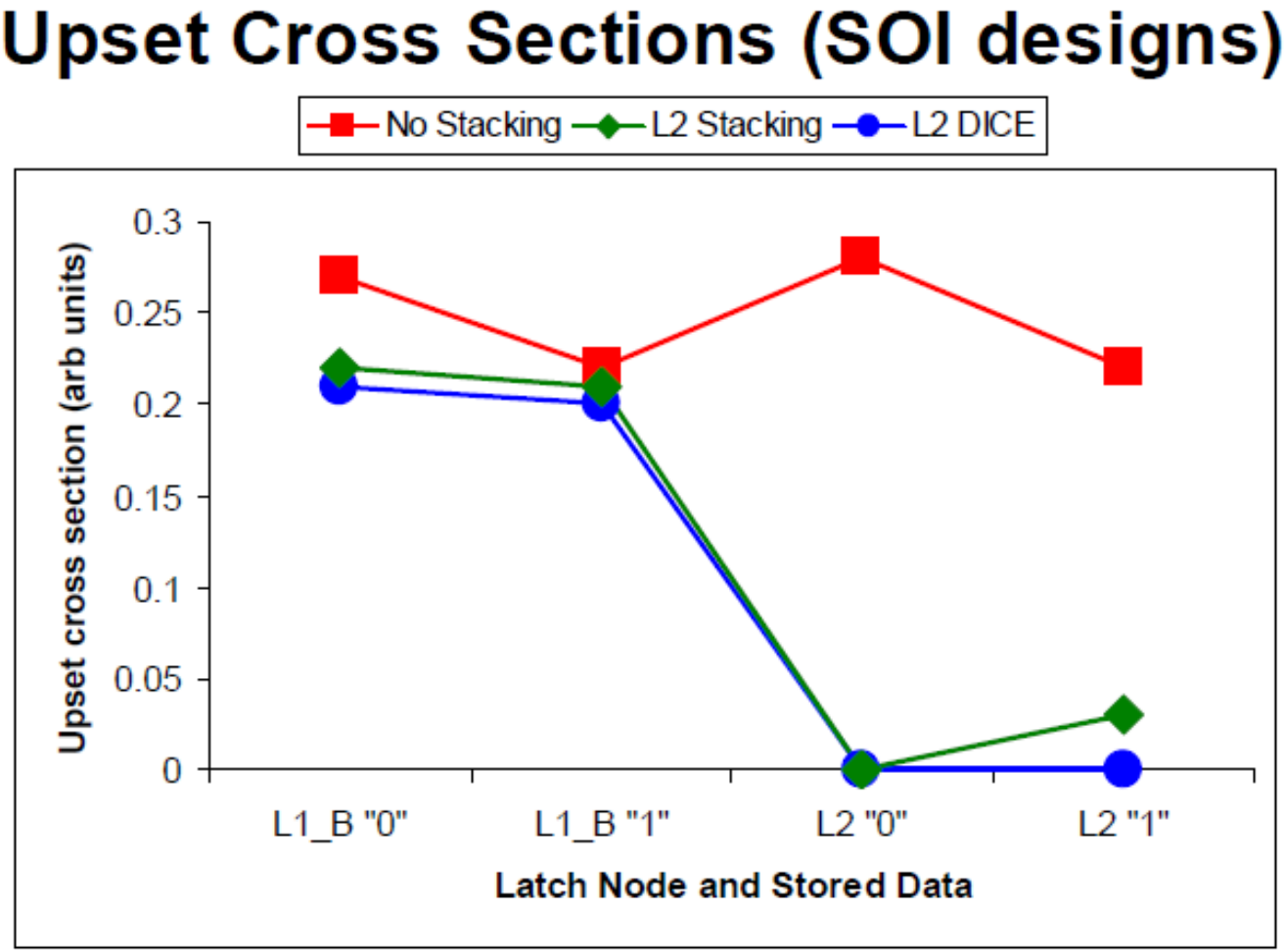
Stacked SOI Device for SEU Immunity





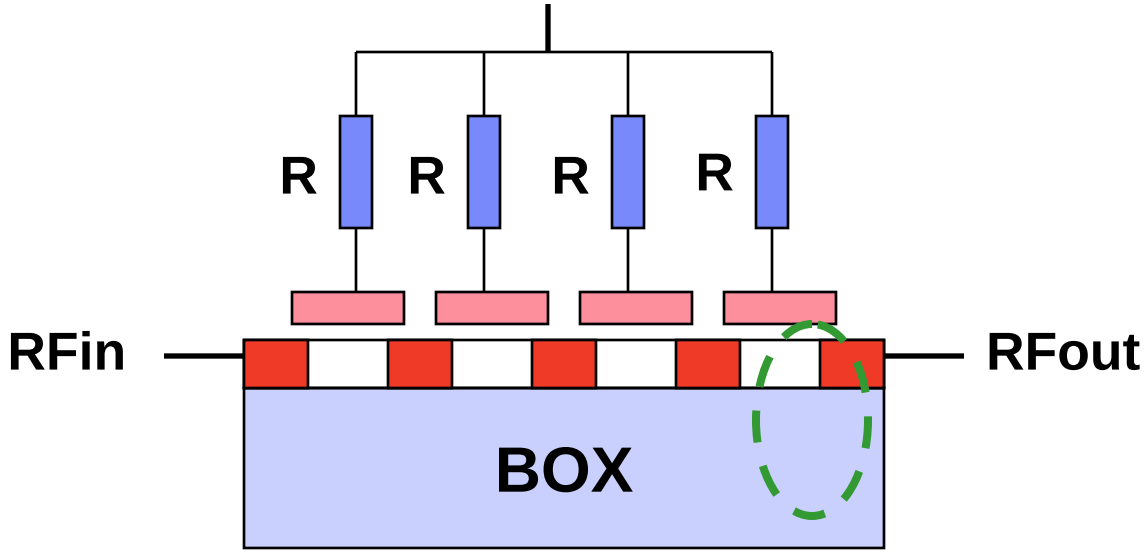
Reference: J. Cai et al., 2008 IEEE Int. SOI Conference, pp. 21-22

Latches Employing Stacked SOI Device as Effective as Dual Interlock Cell (DICE) Latches for SEU



Reference: J. Warnock et al, 2010 ISSCC

High-Voltage SOI FET RF Switch



No diffusion-to-substrate breakdown

SiGe-CBiCMOS on Thick SOI

- **Thick SOI with high resistivity substrate; deep and shallow trench isolation**
- **Vertical SiGe npn and pnp**
- **3.3V and 2.5V CMOS**

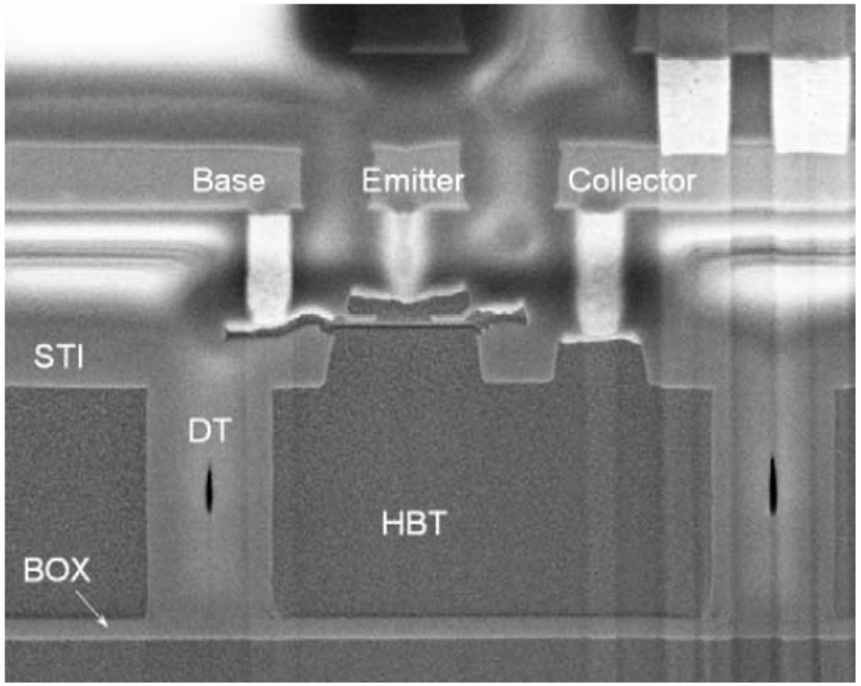


Fig. 2. SEM X-section showing an HBT with DT/STI isolation on SOI.

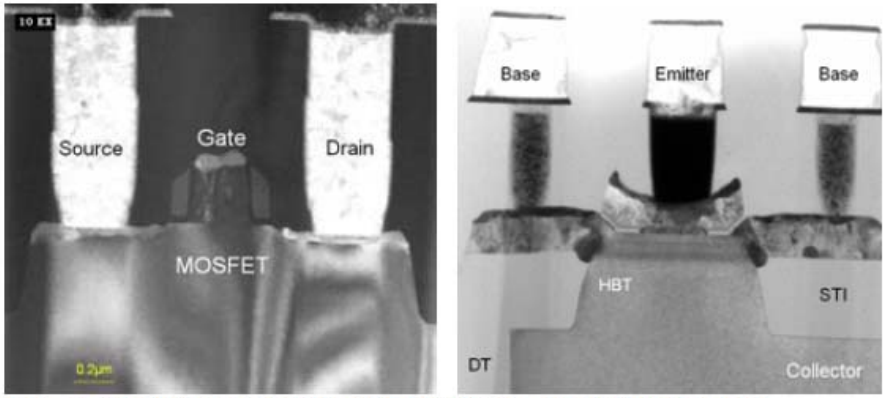
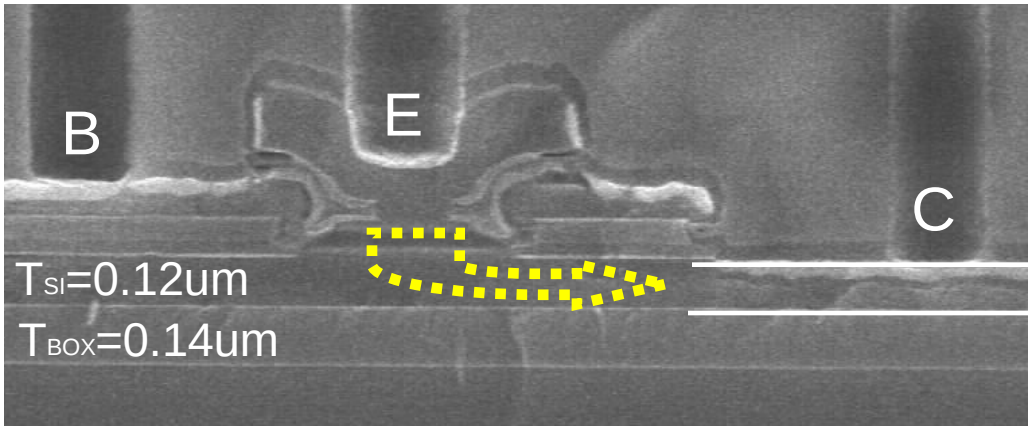


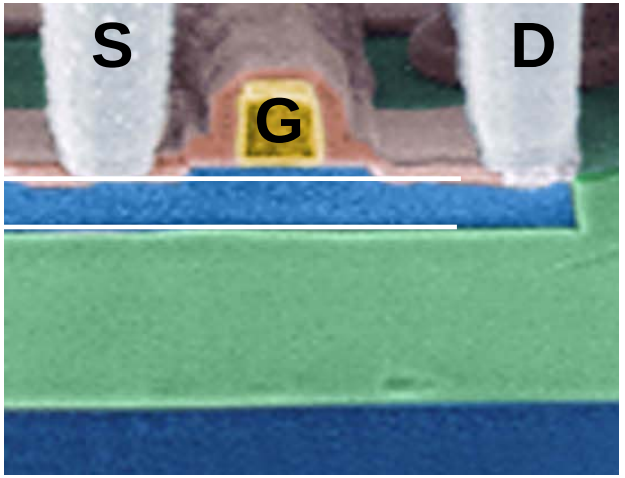
Fig. 3. (A) TEM x-section of LVCMOS. (B) TEM of HBT

Reference: J. Babcock et. al., 2010 BCTM

Vertical SiGe-Base Bipolar on CMOS-Compatible SOI



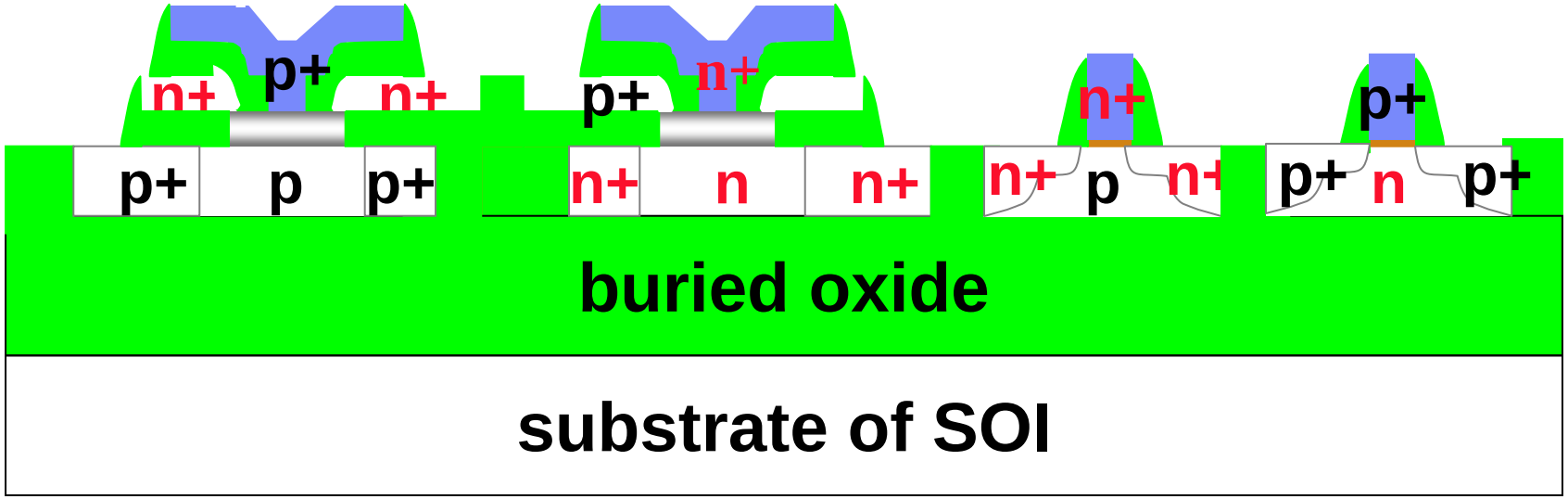
Thin-SOI vertical SiGe-base bipolar



SOI CMOS

Source: J. Cai et al., 2003 BCTM

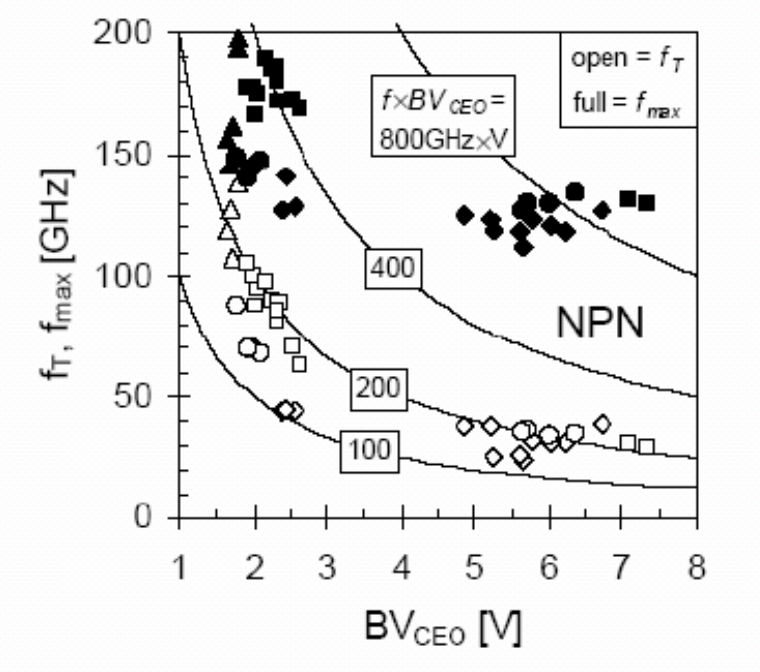
Thin-SOI Complementary BiCMOS



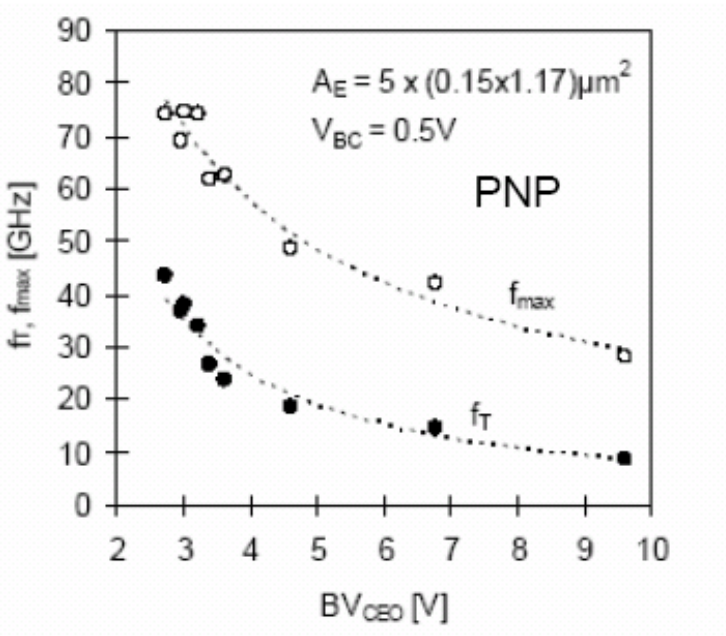
- **Vertical** npn and pnp, and CMOS on same thin SOI
- Opportunity for circuit innovation

Source: T.H. Ning, Symp. VLSI Technology, 2003

Bipolar on thin SOI – FOM



A. Chantre et al, ECS – SiGe, 2006



J. Duvernay et al, BCTM 07

- First integration of both NPN and PNP ***vertical bipolar devices in a thin SOI film*** (160nm SOI over 400nm buried oxide) with high BVCE0 and f_T , f_{max} has been demonstrated recently

- This integration is fully compatible with a 130nm SOI CMOS process

The Problem with SOI CMOS

- **Cost, cost, cost**
  - **SOI substrate cost**
  - **What else?**
- **However, we need to consider**
  - **Cost at the system level**
  - **Cost-benefit tradeoff**
  - **System-level benefit enabled by SOI**

Summary

- SoC and hybrid integration are natural trends in integrated-circuit technology
- SOI CMOS provides an ideal platform for SoC and hybrid integration
  - Electrical isolation
  - SOI-unique beneficial device and circuit characteristics
- In considering SOI versus bulk silicon CMOS as platform, need to bear in mind cost-benefit tradeoff
  - Additional benefit must be well worth the additional cost
- With innovation, the *silicon technology glass remains half full*