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# Unification of MOS Compact Models with the Unified Regional Modeling Approach

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## **Models and Modeling Groups**



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### **MOSFET Compact Models: History and Future**



### Need for an Extendable Core Model for Future Generation





## New Challenges in SOI/MG/GAA MOSFET Modeling

**Generic Double-Gate MOSFET with Any Body Doping** 



## DG FinFETs / GAA SiNWs



## The Generic SOI/DG/GAA MOSFET



#### The Poisson–Boltzmann Equation and Solution

$$\begin{aligned} \text{FEEE-EDS/DL} \\ \text{FEEE-EDS/DL} \\ \text{FURCH INSTRUCTION CONSTRUCTION FOR A Constraint of the product of the$$

### The Complete ("Sah–Pao") Voltage Equation



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#### **The Surface-Potential Solutions – Piecewise Regional**

$$\frac{V_{gb} - V_{FB} - \phi_s = \operatorname{sgn}(\phi_s) \Upsilon \sqrt{f_{\phi}}}{V_{gb} - V_{FB} - \phi_s = \operatorname{sgn}(\phi_s) \Upsilon \sqrt{f_{\phi}}} = \begin{cases} -\Upsilon \sqrt{v_{th}} e^{-\phi_s/v_{th}} & (V_{gb} \ll V_{FB}), \text{Accumulation} \\ +\Upsilon \sqrt{\phi_s} & (V_{FB} < V_{gb} < V_t), \text{Depletion} \\ +\Upsilon \sqrt{v_{th}} e^{-(2\phi_F + V_{cb})/v_{th}} e^{\phi_s/v_{th}}} & (V_{gb} \gg V_t), \text{Strong inversion} \end{cases}$$

#### Piecewise regional solutions

 $\mathcal{L}{W}$  is the **Lambert W** function, which is the solution of the equation:  $\exp(X) + aX + B = 0$ 

where 
$$X_{cc} = \frac{-\phi_{cc}}{2v_{th}}, B_{cc} = \frac{V_{gb} - V_{FB}}{\gamma \sqrt{v_{th}}}, X_{ss} = \frac{\phi_{ss} - 2\phi_F - V_{cb}}{2v_{th}}, B_{ss} = -\frac{V_{gb} - V_{FB} - 2\phi_F - V_{cb}}{\gamma \sqrt{v_{th}}}, \text{ and } W = \frac{1}{a} \exp\left(-\frac{B}{a}\right), a = \frac{2\sqrt{v_{th}}}{\gamma}$$

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## The Surface Potential: Unified Regional Modeling (URM)

## **Surface-Potential Derivatives and Regional Components**



http://www.springerlink.com/content/x8t0742r3m051650/

#### Doping-Dependent $\phi_s$ : "Depletion" vs. Volume Inversion



### Paradigm Shift: B/G-reference and Source/Drain by Label

IEEE-EDS / DL EEE / NTU □ S/D by convention (nMOS)  $\begin{array}{l} \bullet \ V_d > V_s : \ I_{ds} > 0 \ (`D' \rightarrow `S') \\ \bullet \ V_d < V_s : \ I_{ds} > 0 \ (`D' \leftrightarrow `S') \end{array}$ • By convention, nMOS I<sub>ds</sub> always flows from 'D' to 'S' • Terminal swapping for  $-V_{ds}$ : involving  $|V_{ds}|$  in model □ S/D by label (layout) □ Effective drain-source voltage (V<sub>ds.eff</sub>) FB:  $V_{ds,eff} = V_{d,eff} - V_{s,eff}$  BC:  $V_{ds,eff} = V_{db,eff} - V_{sb,eff}$ Always Source Always Drain  $I_{ds} = \overline{\beta} \left( \overline{q_i} + \overline{A_b} v_{th} \right) V_{ds,eff} = I_d - I_s$  $=\overline{\beta}\left(\overline{q_{i}}+\overline{A_{b}}v_{th}\right)V_{db,eff}-\overline{\beta}\left(\overline{q_{i}}+\overline{A_{b}}v_{th}\right)V_{sb,eff}$ l<sub>ds (B)</sub> > Key: Bulk/Ground-reference — auto switch to B/G-ref when body-contact is biased or floating Sub Intrinsic I<sub>ds</sub> is an exact odd function of V<sub>ds</sub> •  $V_d > V_s$ :  $I_{ds} > 0 (D \rightarrow S)$ •  $V_d < V_s$ :  $I_{ds} < 0 (S \rightarrow D)$ Physical modeling of asymmetric MOS (nontrivial) with "terminal swapping" for negative  $V_{ds}$ )

## Modeling Asymmetric Source/Drain MOSFET



Gummel Symmetry Test on Undoped s-DG Without BC



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## **Harmonic-Balance Simulation**

Undoped-Body DG FinFET vs. GAA SiNW



#### s-DG/FinFET: Short-Channel Transfer Characteristics

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Transfer Ids-Vgs

Transfer gm-Vgs

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#### Symmetric-DG FinFET model comparison with Measurement.



### s-DG/FinFET: Short-Channel Output Characteristics



#### Symmetric-DG FinFET model comparison with Measurement.



## **GAA: Model Comparison with Measurement**

GAA: Model Comparison with Measurement (1<sup>st</sup> Derivative)









**GAA: Measured Gummel Symmetry Test** 



### Schottky-Barrier MOSFET: Ambipolar Current



SB-MOS: Total Current = (Electron + Hole) Currents





DSS-SiNW MOS **subcircuit model** comparison with Measurement. G. J. Zhu, *et al.*, SSDM, p. 402, Oct. 2009; T-ED, 57(4), p. 772, Apr. 2010.

### **DSS-SiNW: Subcircuit Model for Two Measured Devices**



## **Xsim: Basic Bulk-MOS Model Parameters**

