

ED Japan Chapter  
by Mitsumasa Koyanagi, Chair

A DL talk entitled "Circuit Parameter Optimization of Various MOS Structures for Process Variability using Plackett- Burman Technique" was given by Prof. Arun N. Chandorkar of Indian Institutes of Technology, India, at Tokyo Institute of Technology, Yokohama, Japan, on July 11, 2008. His DL talk initially looks into various variability issues in technology scaled-down devices including FinFETs from ITRS point of view and then suggest a statistical method namely Plackett-Burman technique which can predict the influence of multiple process parameters on various circuit parameters. More than 20 people attended this DL meeting and enjoyed the lecturer's meaningful talk.

Another DL talk entitled " Defect Engineering Challenges of Advanced Ge Technologies" was given by Dr. C. Claeys of IMEC, Belgium, at Tokyo Institute of Technology, Yokohama, Japan, on August 21, 2008. Dr. Claeys is president of EDS and director of advanced semiconductor technologies in IMEC. In his lecture, some advanced Ge processing modules were reviewed from a viewpoint of defect control and engineering. Shallow junctions, contact technology and integration aspects were discussed. This DL meeting attended by 30 people was very stimulating and fruitful.

In addition, in the third quarter of this year from July 2008 to September 2008, ED Japan Chapter had 3 joint technical meetings with the Japan Society of Applied Physics, etc.



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Photo caption:

The DL meeting on July 11, 2008. From the fourth person from the left at the back: Prof. T Arun N. Chandorkar, Indian Institutes of Technology, India.

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Photo caption:

The DL meeting on August 21, 2008. From the fifth person and the seventh person from the left at the back: Dr. C. Claeys of imec, Belgium, and Prof. Hiroshi Iwai, Partner and EDS Jr. Past President, respectively.

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