

## ED Japan Chapter

- by Mitsumasa Koyanagi, Chair

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The officers of the EDS Japan Chapter retired upon termination of their 2 year term at the end of 2007. For 2008-2009, the chapter has a new chair and staff. They are Prof. Mitsumasa Koyanagi (Tohoku Univ.), Chair; Dr. Shinichiro Kimura (Hitachi Ltd.), Vice-chair; Prof. Tetsu Tanaka (Tohoku Univ.), Secretary; and Dr. Kazuyoshi Torii (Hitachi Ltd.), Treasurer. We would like to thank the former executive officers for their great contributions to the EDS Japan Chapter.

On January 8<sup>th</sup>, the annual meeting of the EDS Japan Chapter was held in Tokyo. The new executive officers were introduced to the members. The 2007 activities and the 2008 plans of the chapter were unanimously approved. At the meeting, the 2007 EDS Japan Chapter Student Award was given to four students for their outstanding activities in the research of electron devices last year. They are Kenichi Abe (Tohoku Univ.), Ken Shimizu (Univ. of Tokyo), Toshitake Takahashi (Univ. of Tokyo), and Kazuyuki Hiramata (Waseda Univ.). They received the metallic certificate plaques and premiums from Dr. Atsushi Kurobe (Toshiba Corp.), the 2006-2007 chapter chair.

Following the annual meeting on the same day, the briefing session regarding the 2007 IEDM was held. Seven speakers gave summary talks on the highlights of the IEDM. This session has gained widespread popularity among engineers and researchers in Japan who did not have a chance to attend the last IEDM. They obtained the latest information on electron device technologies. The session, with 120 participants, was very successful.

In addition, on January 25<sup>th</sup>, EDS Japan chapter provided a seminar to members in the field of workfunction control of high-k insulator at Suzukakedai Campus in Tokyo Institute of Technology, Yokohama, Japan. The lecturer was Prof. John Robertson of Cambridge University, and the title of the seminar was, "Work function control in HfO<sub>2</sub> - metal gate stacks". Ideal interfaces without Fermi level pinning, Fermi level pinning effect, SiO<sub>2</sub>+O vacancy model, and layer model were explained. The seminar was very useful for the researchers in the field of high-k metal gate stack technology for advanced integrated circuits.



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Photo caption: The committee meeting of the EDS Japan chapter (January, 2008).

From the left at the front: Dr. Tadashi Nishimura, EDS Kansai Chapter Chair; Prof. Fumio Harashima, IEEE Japan Council Chair; Prof. Mitsumasa Koyanagi, new Chair; Dr. Atsushi Kurobe, ex-Chair; and Dr. Tsutomu Sugawara, IEEE Japan Council Secretary.

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Fig. Caption: Prof. John Roberson and the audience.