Charge-Trap NAND Flash Memory

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Support: Applied Materials, Intel Corporation, SRC/GRC

Outline

FG NAND Flash scaling challenges

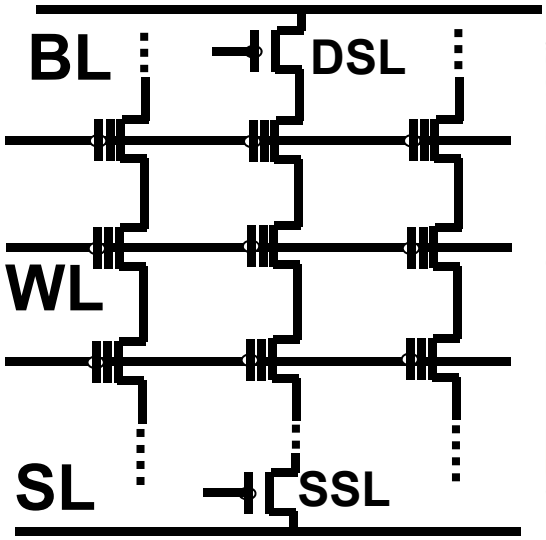
SiN based charge trap flash – material dependence

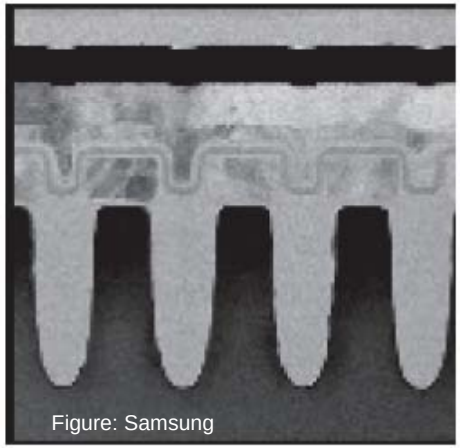
P/E simulation of SiN Flash

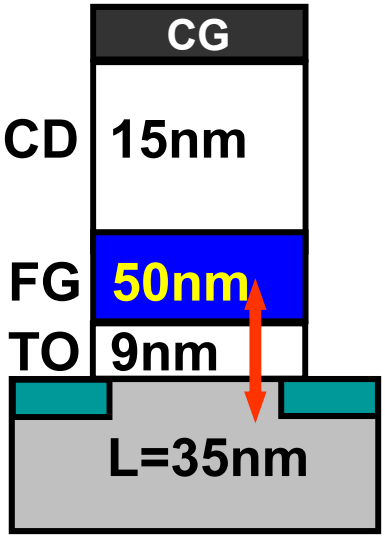
Metal nanodot Flash

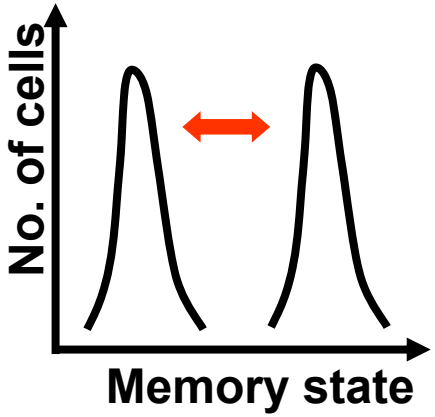
Scalability simulation of m-ND Flash

NAND Flash Background



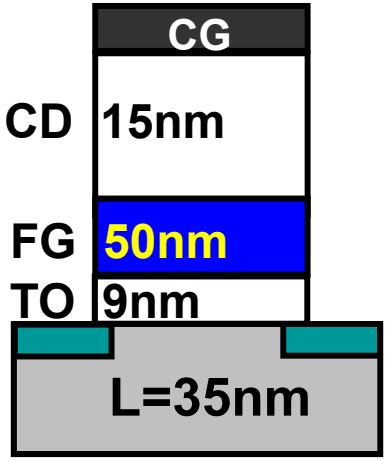






- Electron transfer between substrate & FG define memory state (write & erase)
- FG surrounded by TO & CD acts as electron storage well (non-volatility, need 10yrs), though leak out occurs over time (retention loss)
- Repeated Write/Erase (10-100K needed) causes memory wear out (cycling endurance)

NAND Flash Scaling

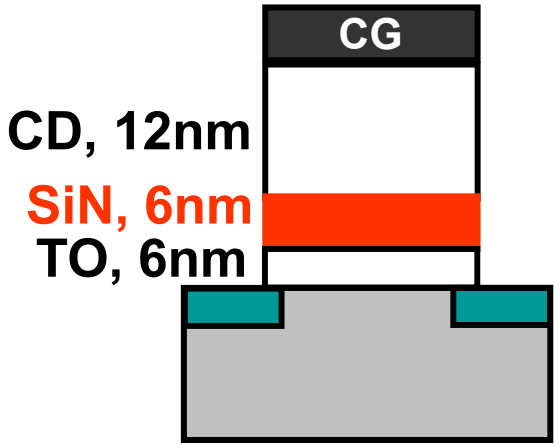


- More memory, faster access, reduced cost
- Guideline (ITRS roadmap): L=35nm (2009), 28nm (2010/11), 22nm (2013/14)…
- SLC (1bit/cell), MLC (2 or 3 bits/cell) for higher density, higher reliability issues

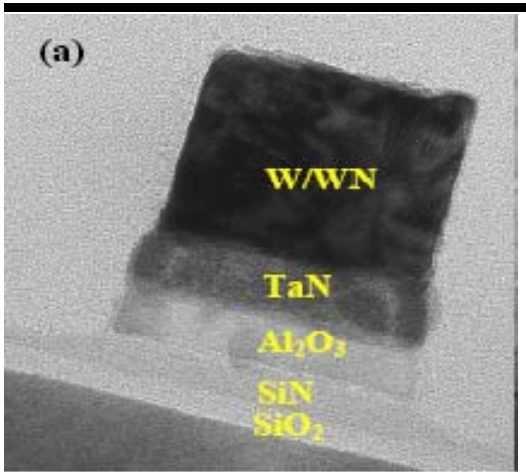
Scaling penalty:

(1) Loss of CG – FG coupling
(2) Cell to cell cross talk
(3) Non-scaling of TO, FG and CD thickness
(4) Non-scaling of operating voltage
(5) Higher reliability concern

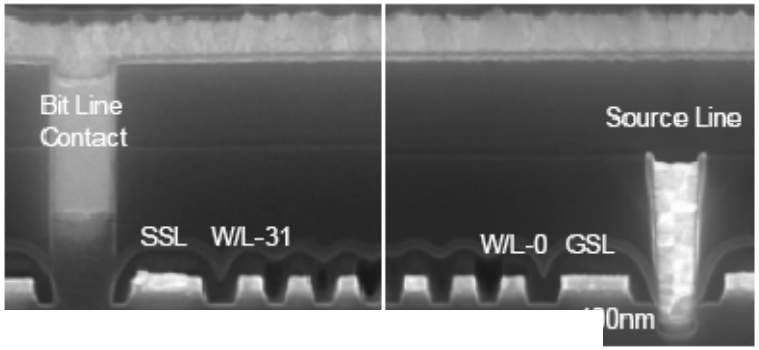
Solution: Discrete trap-based charge storage

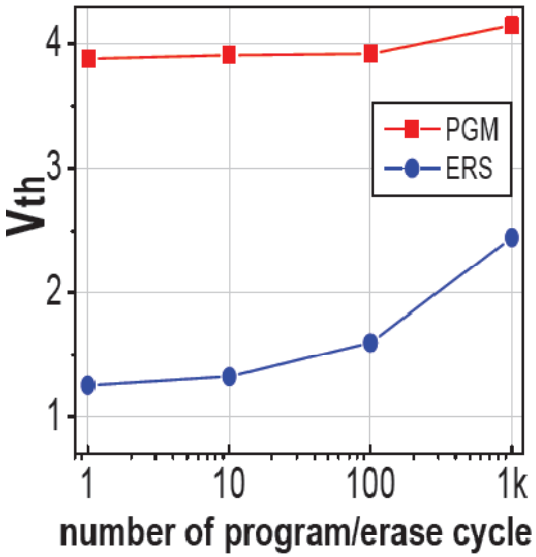


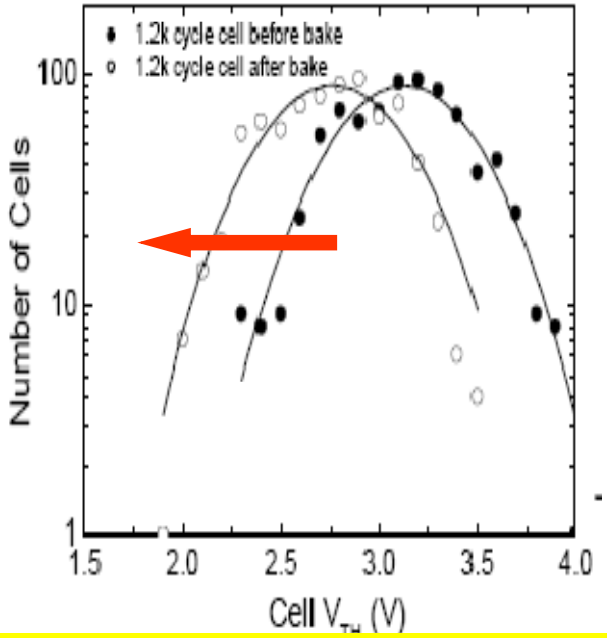
Planer CTF



Devices & test chip demonstrated (Samsung)





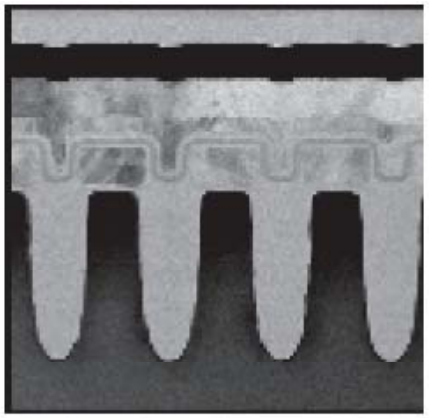
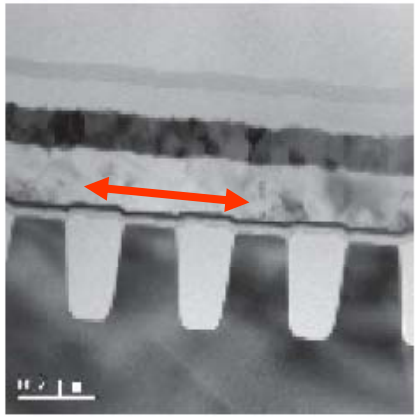


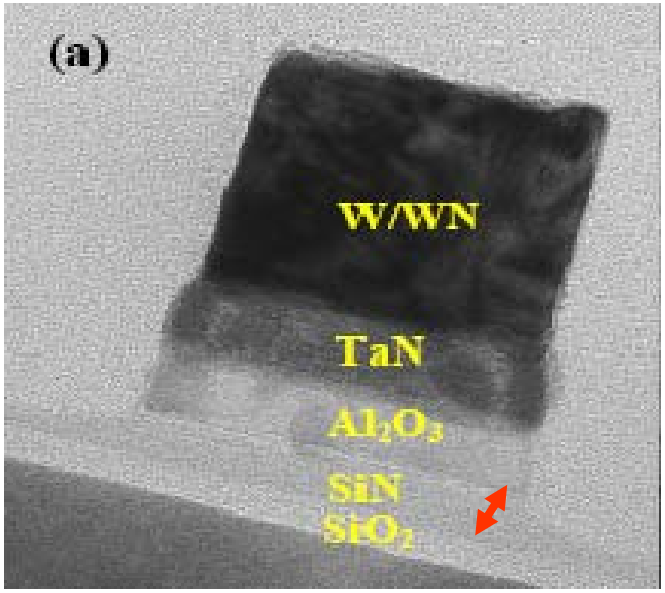
- **Memory window close down with W/E cycling**
- **Data keeps leaking out (worse than FG!)**
- **Loss of memory operation**

CTF reliability worse than FG, no product yet

Retention Issue

Lateral or Vertical charge migration

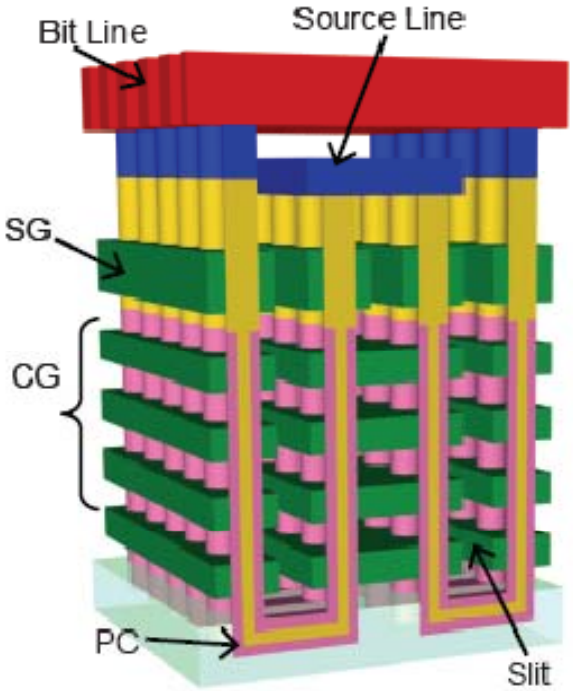
Floating Gate	SONOS
	

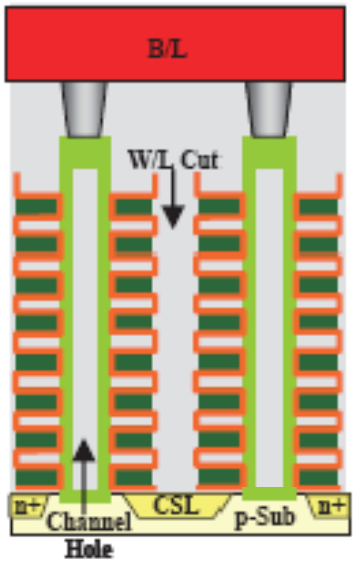


Trap depth of SiN is key to control charge migration
Solution – to cut SiN above STI (Samsung, 2007)

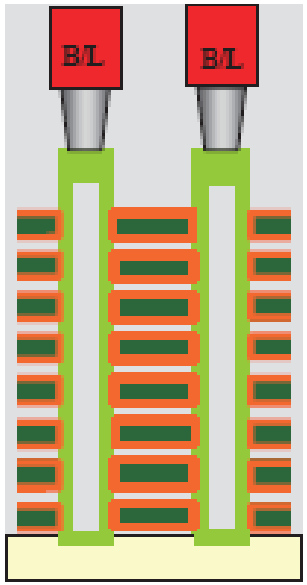
NAND 3D Memory

3D CTF proposed as a way to move forward below 20nm node: BiCs (Toshiba), TCAT (Samsung)





(a) X-Direction



(b) Y-Direc

Motivation

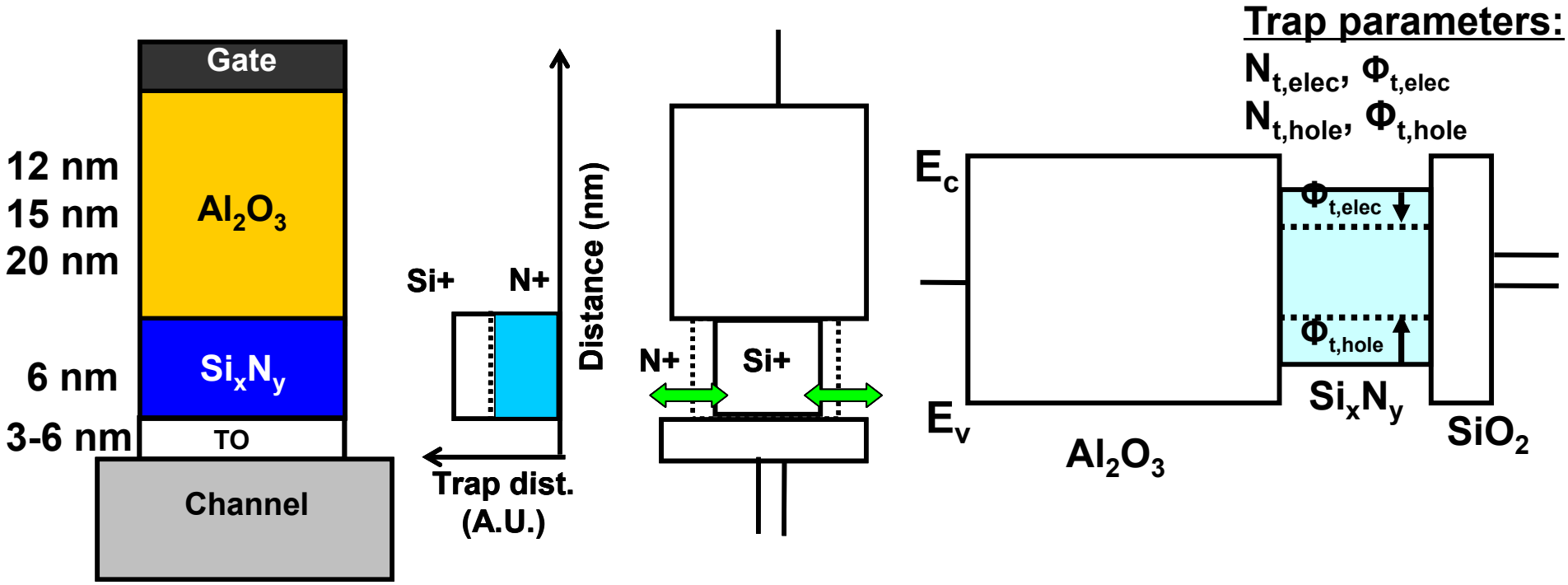
CTF reliability improvement needs:

Understanding impact of device processing on material and electrical properties

Proper device design (structure, composition)

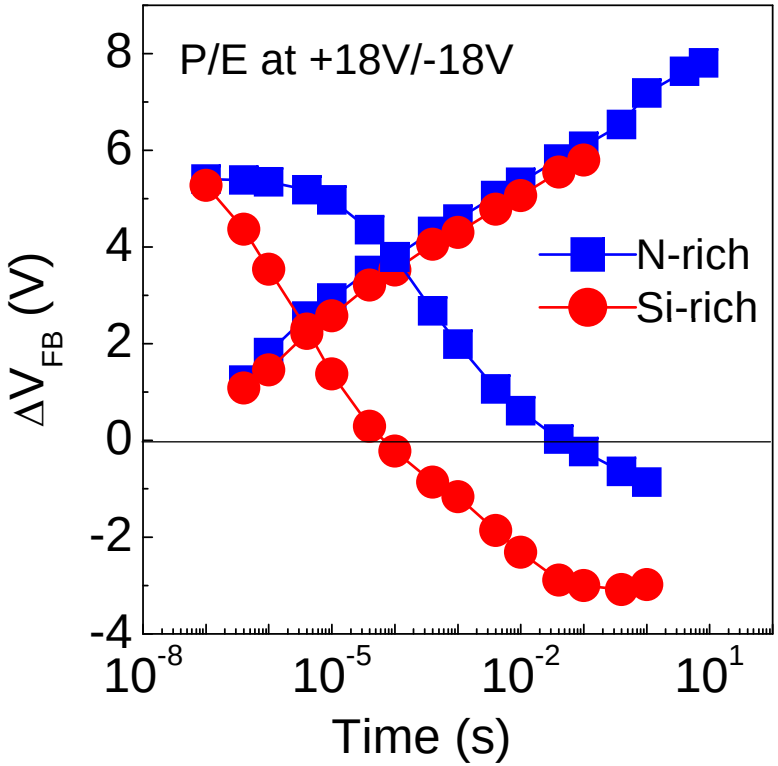
Detailed electrical characterization & modeling – feedback for intelligent manufacturing

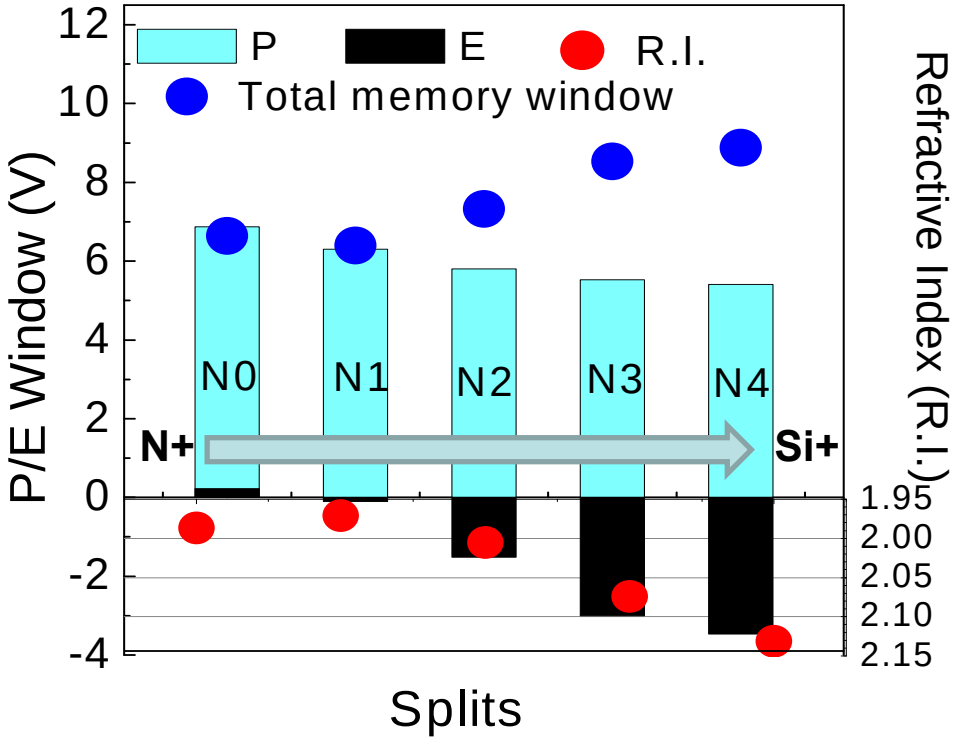
SANOS Device Structure



Charge tunnel from substrate to SiN via TO, Al_2O_3 used for leakage blocking

P/E Transients



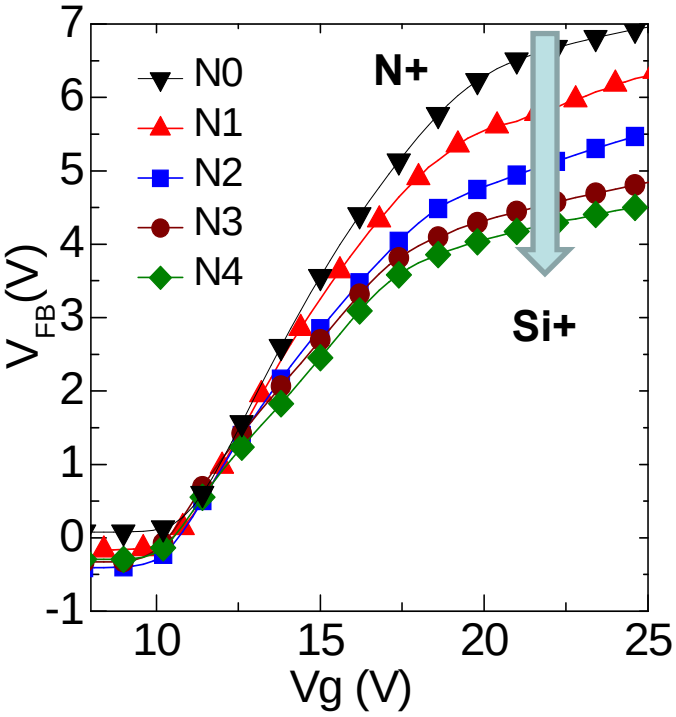


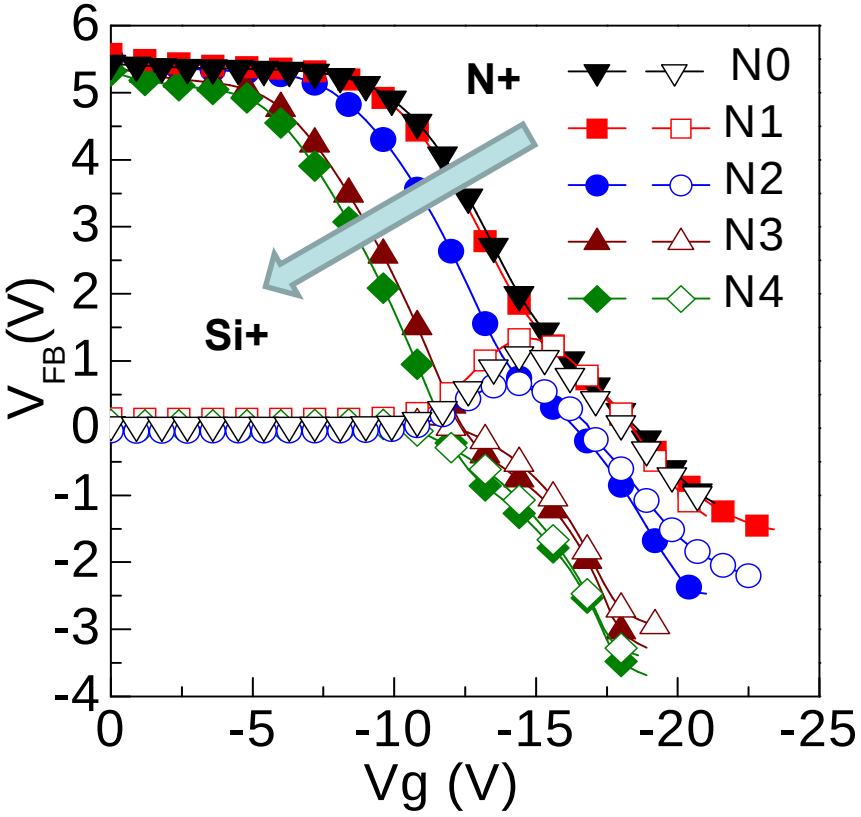
High-k blocking dielectric:

- **Better coupling to channel**
- **Larger memory windows**

P / E state (memory window) depend on SiN composition

ISPP and ISPE





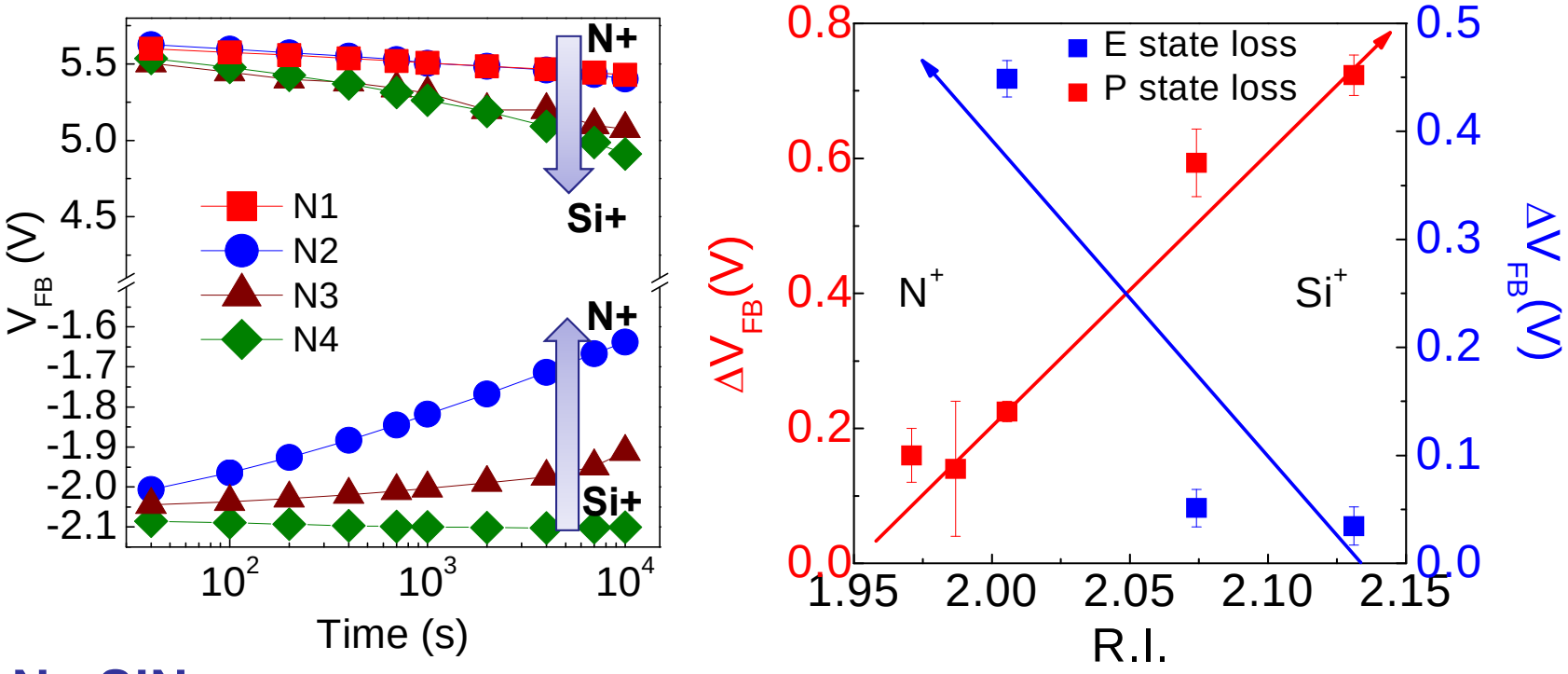
N+ SiN

- **Higher electron trapping efficiency**
- **Poor erase characteristics**

Si+ SiN

- **Low P saturation levels**
- **Higher erase efficiency**

Charge loss (Retention)



N+ SiN

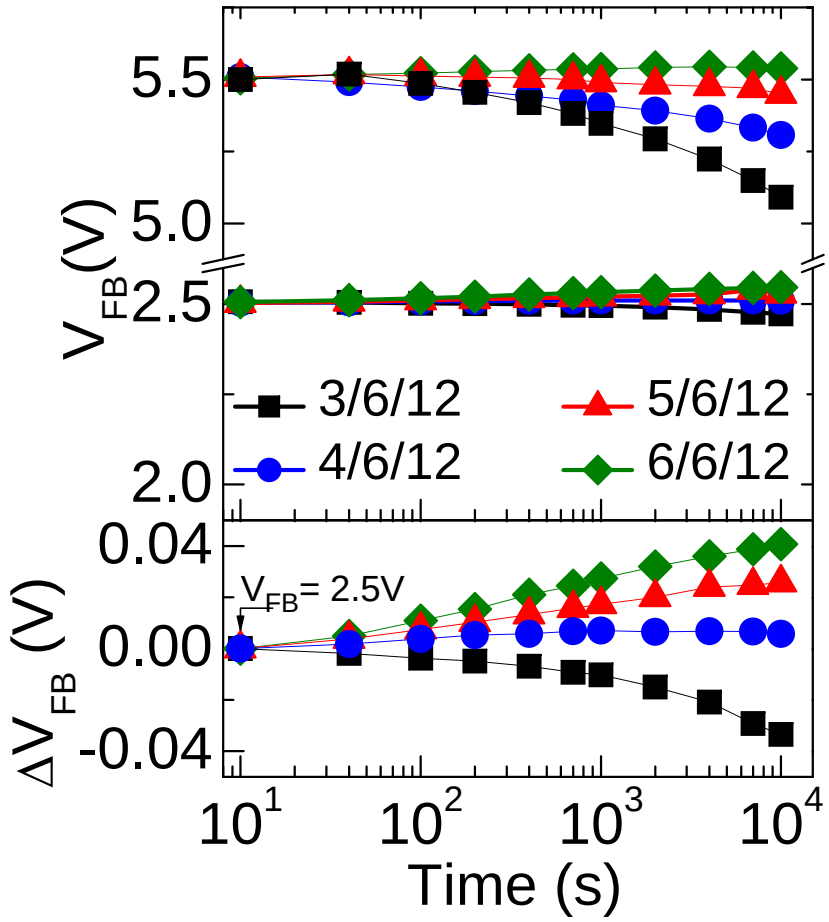
- **Deep electron traps - shallow hole traps**

Si+ SiN

- **Shallow electron traps - deep hole traps**

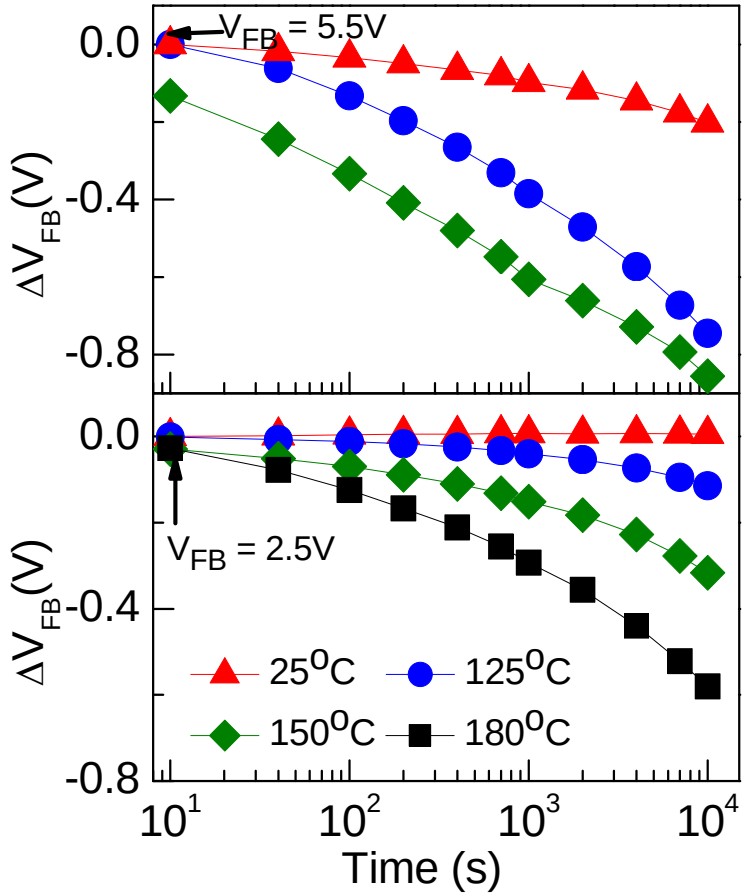
P/E state retention dependent on SiN composition

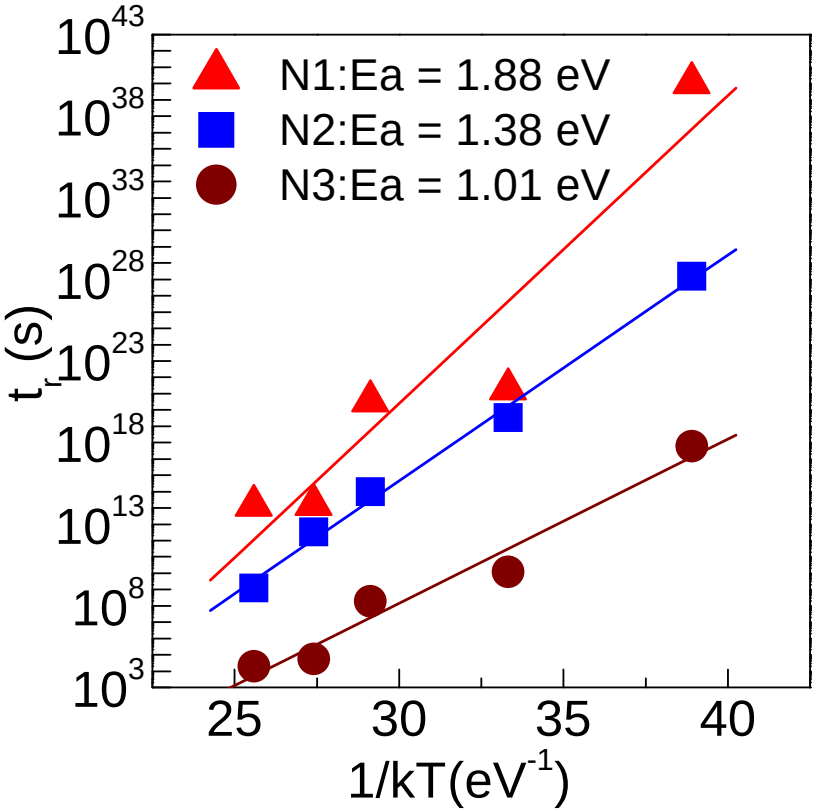
Tunnel oxide thickness dependence



Thinner TO → Increased electron tunnel out from SiN

Retention – T dependence





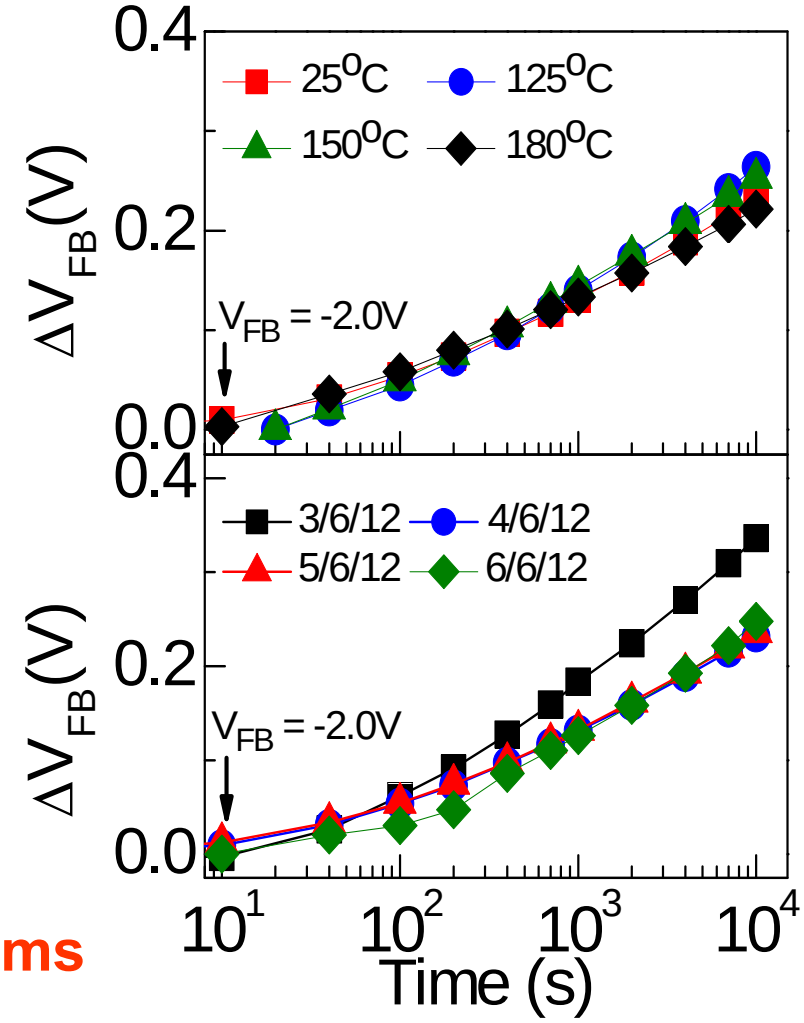
Higher activation energy in N+ ⟶ Deeper electron traps

Retention – E state TO thickness & T effect

E state retention loss

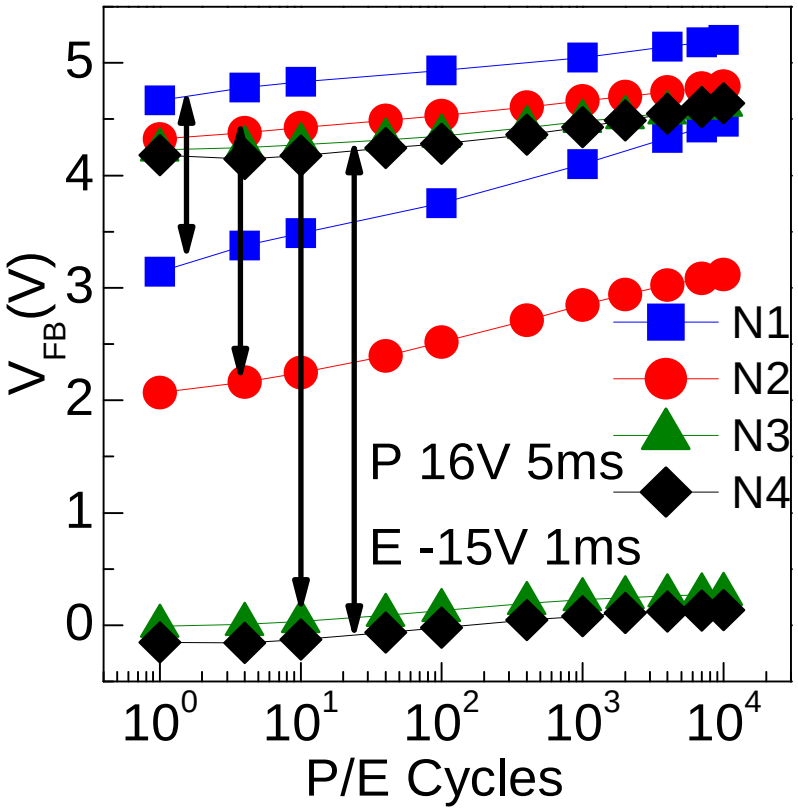
- T independent
  No thermal emission of holes

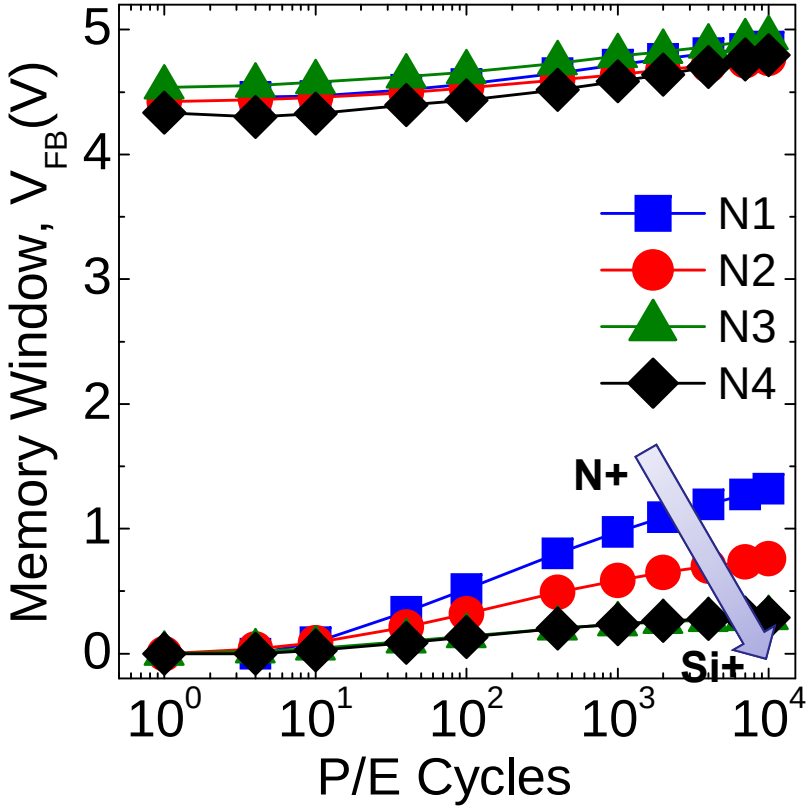
- TO independent for > 3nm
  No Trap to Band tunneling of holes



Different charge loss mechanisms for electrons and holes

Endurance – SiN Composition





Endurance degradation SiN composition dependent

Si-rich devices cycle with negligible erase state degradation

Summary

- Comparison of SiN Compositions

Parameter	N+	Si+
Electron trap depth	**Deep**	**Shallow**
Hole trap depth	**Shallow**	**Deep**
Hole trap density	**Very low**	**High**
Split window operation	**Not possible**	**Possible**
Endurance degradation	**High**	**Low**

P/E Simulation of SiN Flash

- **Develop a Simulation framework capable of providing useful insight into the physics involved during Program /Erase (P/E) operations.**

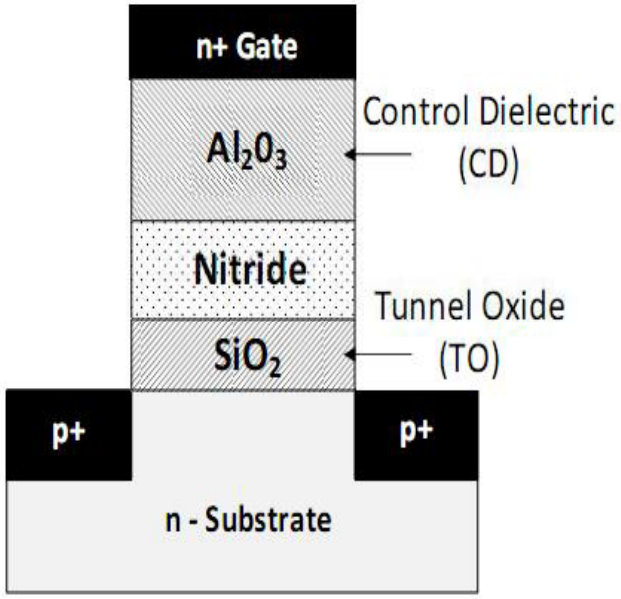
- **Accurately predicting P/E behavior of SANOS/SONOS memories**

- **Simulation up to long time instants, large biases**

- **For different gate stack dimensions**

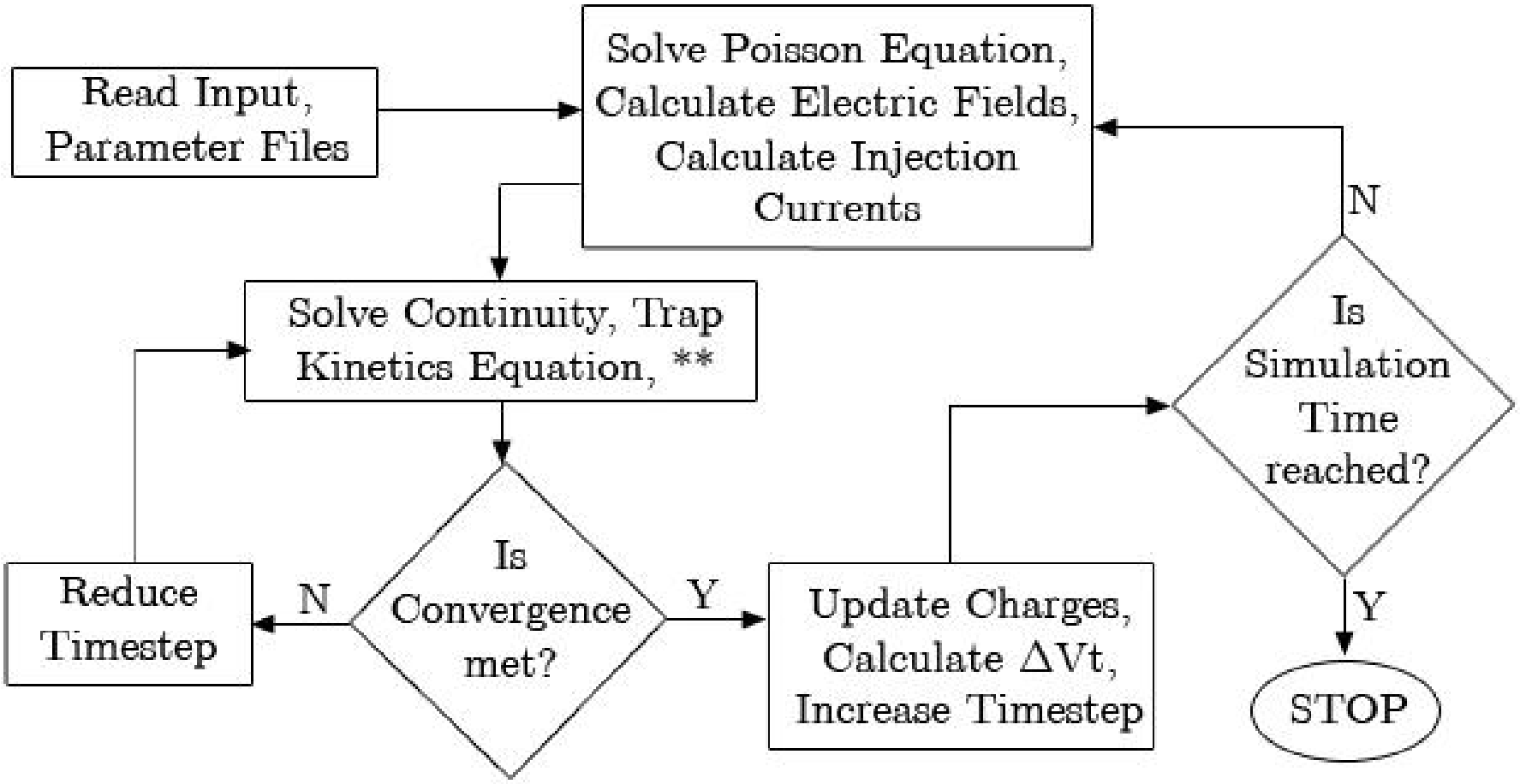
- **For different Nitride Compositions**

Simulation Methodology



- Set P/E bias
- Compute Poisson throughout gate stack
- Assume TO and CD as pure tunnel barriers, compute tunneling currents in and out of SiN
- Compute transport, continuity and SRH (trapping detrapping) in SiN
- Compute trapped charges, update Poisson
- Continue till end of P/E time

Simulation Flow



Key Models Incorporated

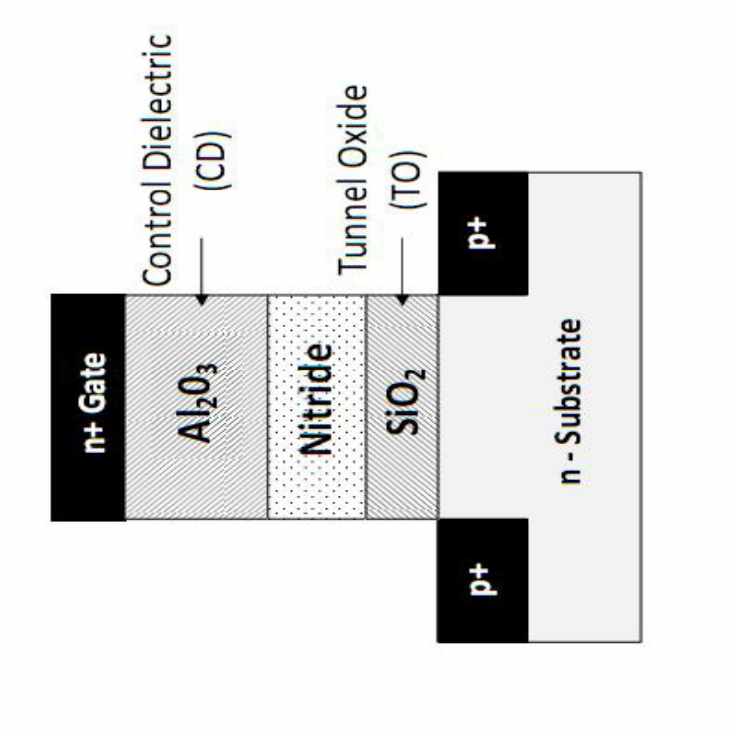
Tsu-Esaki tunneling formulation

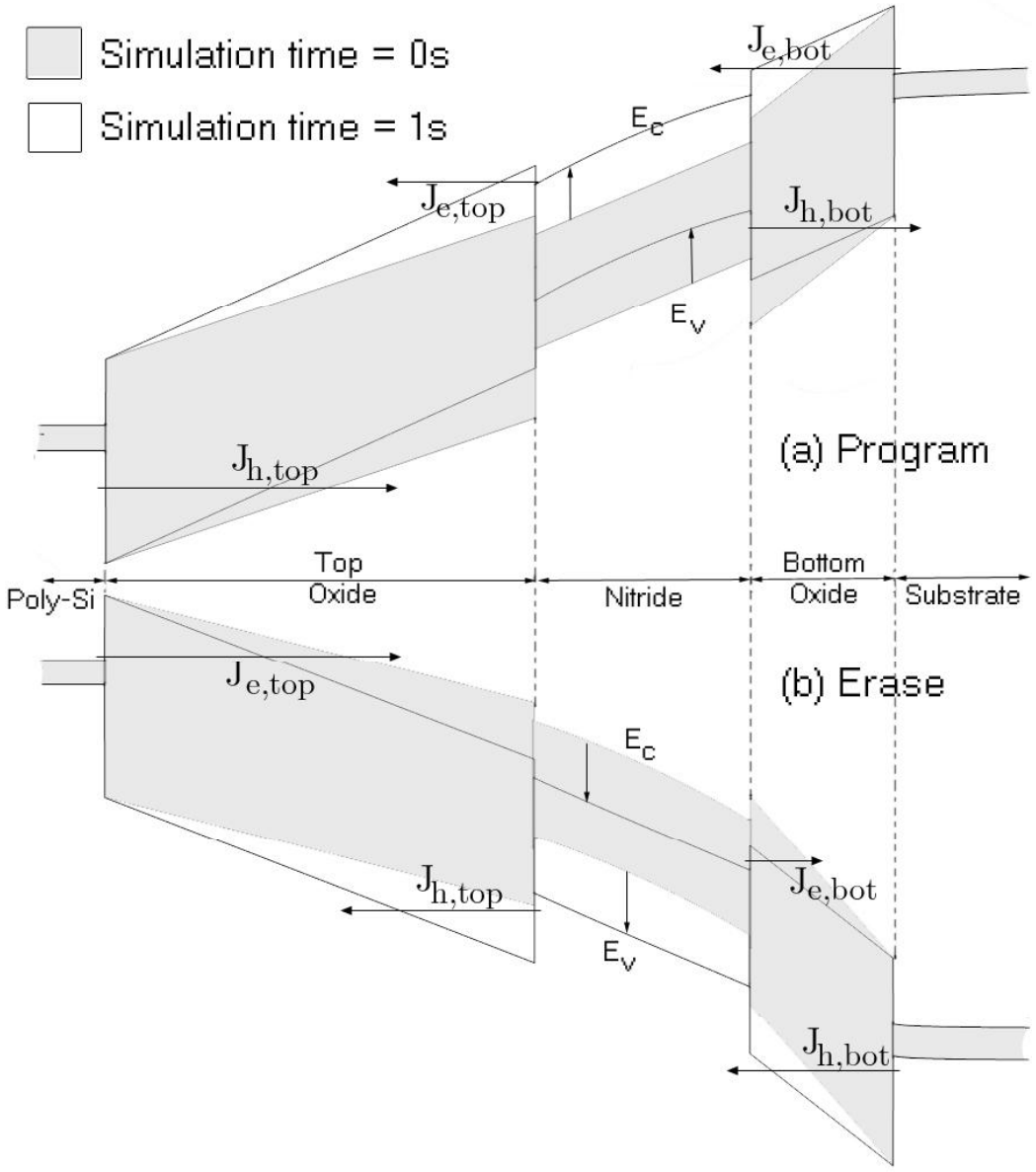
Field dependent capture cross section

Poole Frenkel detrapping from traps

Trap to band tunneling

P/E: Stack Energy Band Diagrams





SANOS sample stack properties

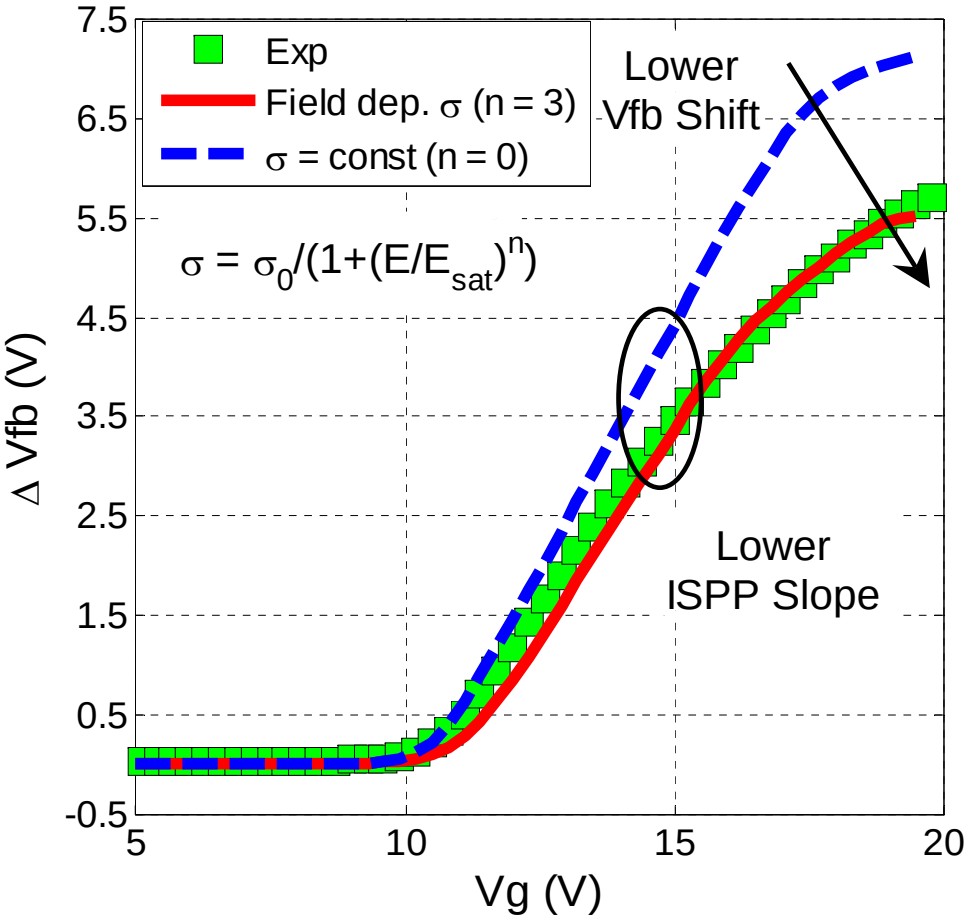
SiN type	Si_2H_6/N_3 flow ratio	Dep. Temp (° C)	RI	Gate Stack Dimensions (nm)		
				TO	SiN	CD
N2	0.005	650	2.006	4	6	**15**
N2	0.005	650	2.006	**6**	6	12
N2	0.005	650	2.006	4	6	12
N0	0.01	**800**	1.987	4	6	12

N_0 → More N rich SiN; N_2 → More Si rich SiN
Different stack dimensions used to check robustness

ISPP Matching

Less than 1V change in V_T (or V_{FB}) for every 1V increment in applied V_G (ISPP slope <1V/V)

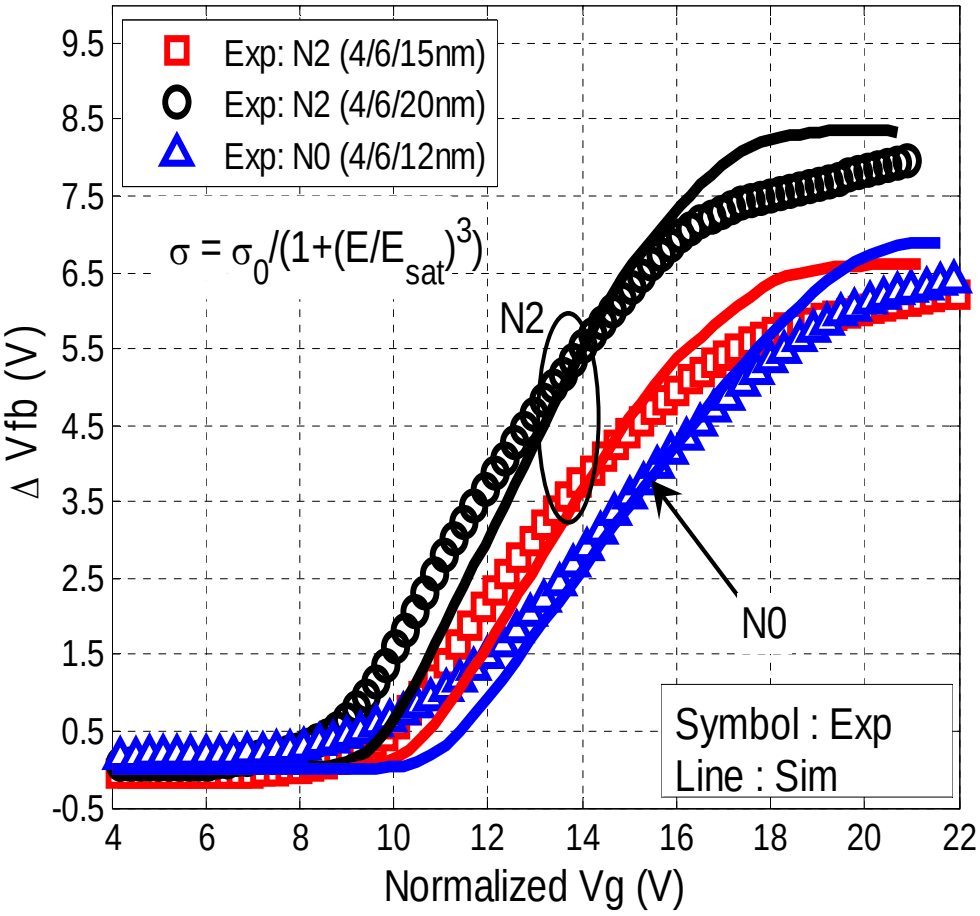
Employing the field dependent σ enables accurate prediction of ISPP



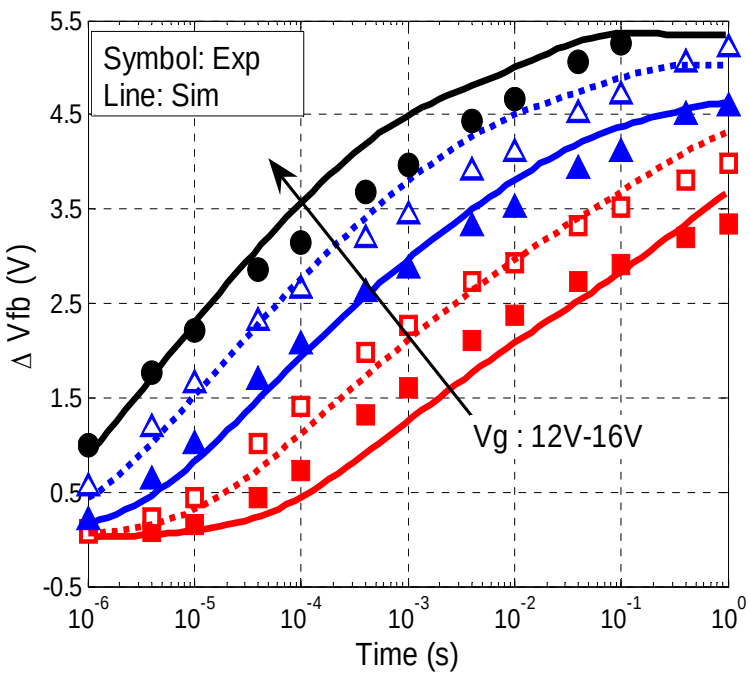
ISPP Matching

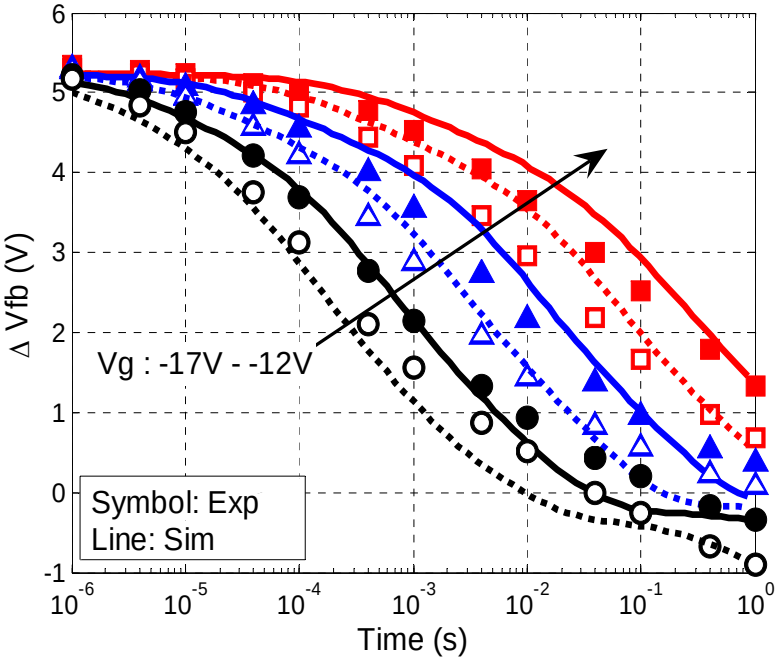
Good matching with ISPP data for varying gate stack thickness and nitride compositions

Same parameter values used during P/E transient matching (to follow)



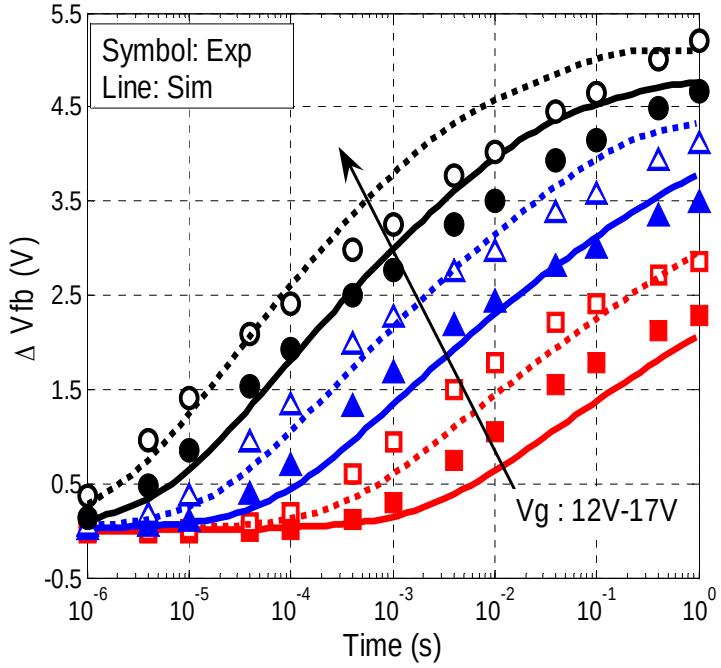
P/E Matching

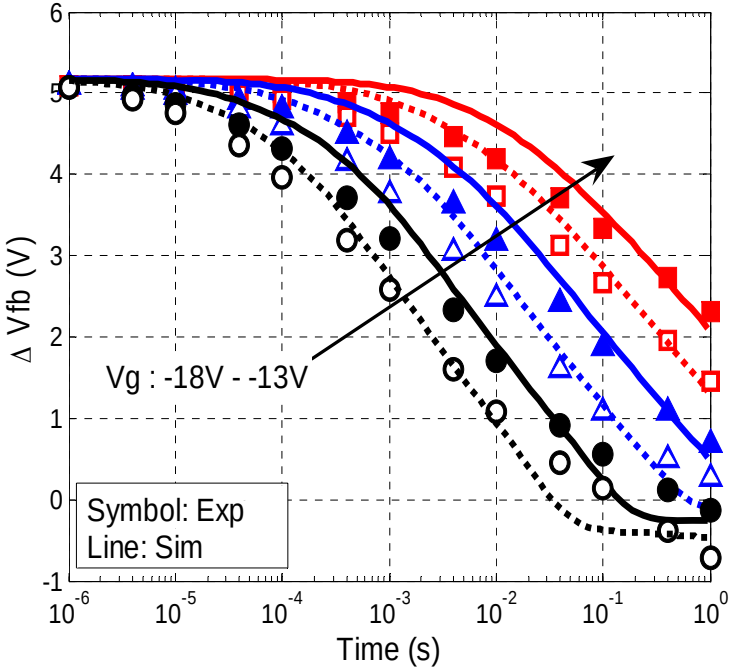




Program and Erase transients (N2-4/6/12 nm SANOS)

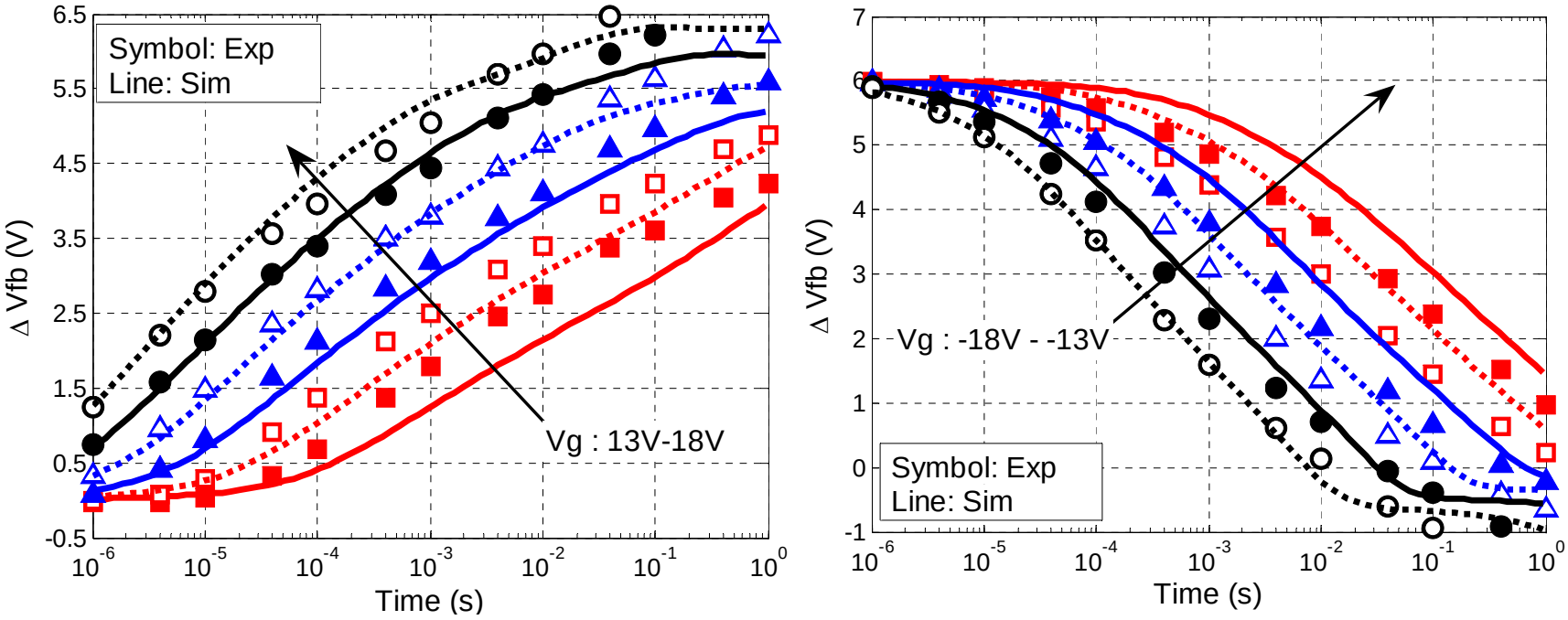
P/E Matching (Change in TO)





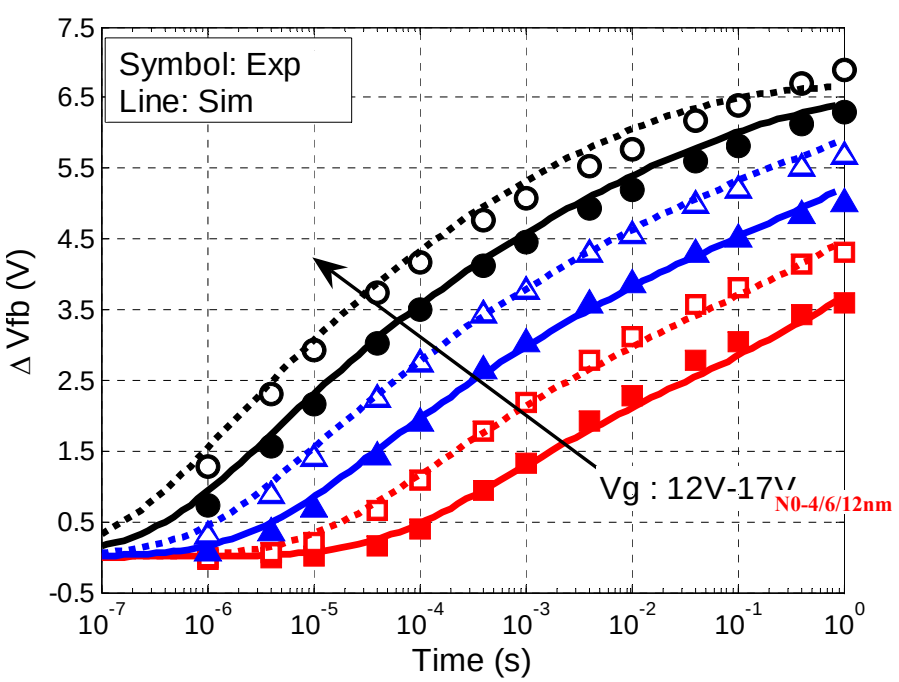
Program and Erase transients (N2-6/6/12 nm SANOS)

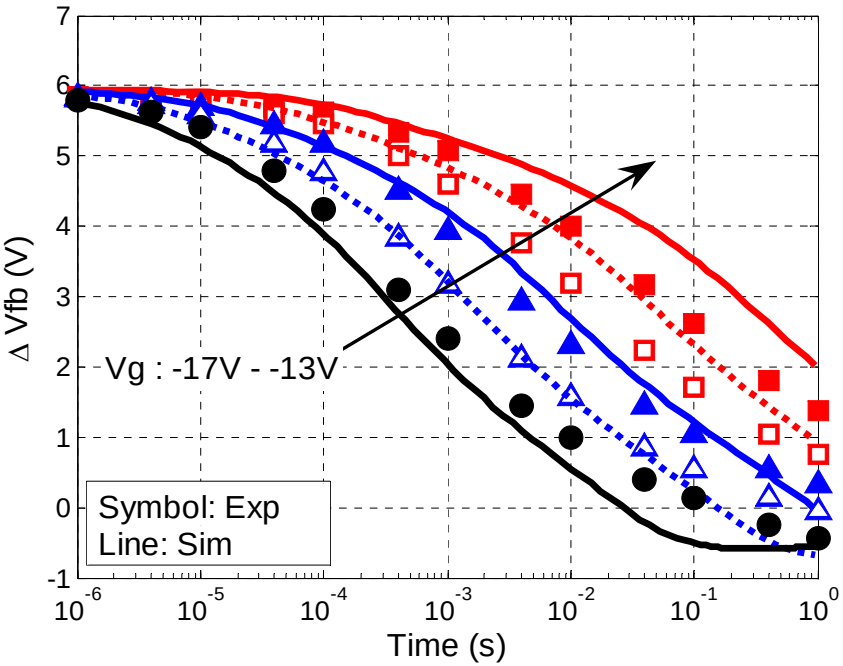
P/E Matching (Change in CD)



Program and Erase transients (N2-4/6/15 nm SANOS)

P/E Matching (Change in SiN)





Program and Erase transients (N0-4/6/12 nm SANOS)

Extracted parameters (SiN dependence)

Parameter	N0	N2	Parameter	N0	N2
Electron trap depth (eV)	1.8	1.63	Hole Trap Depth (eV)	1.73	1.95
Electron trap density ($10^{19}cm^{-3}$)	3.3	3.9	Hole Trap Density ($10^{19}cm^{-3}$)	1.6	2.6
Electron σ const. , σ_0 (10^{-12} cm^2)	5.7	5.7	Hole σ const. , σ_0 (10^{-10} cm^2)	8	8
Trap-band emission freq. υ_{tbt}(10^{13} s^{-1})	4	4	Saturation electric field E_{sat} (10^5 V/cm)	6.25	6.25

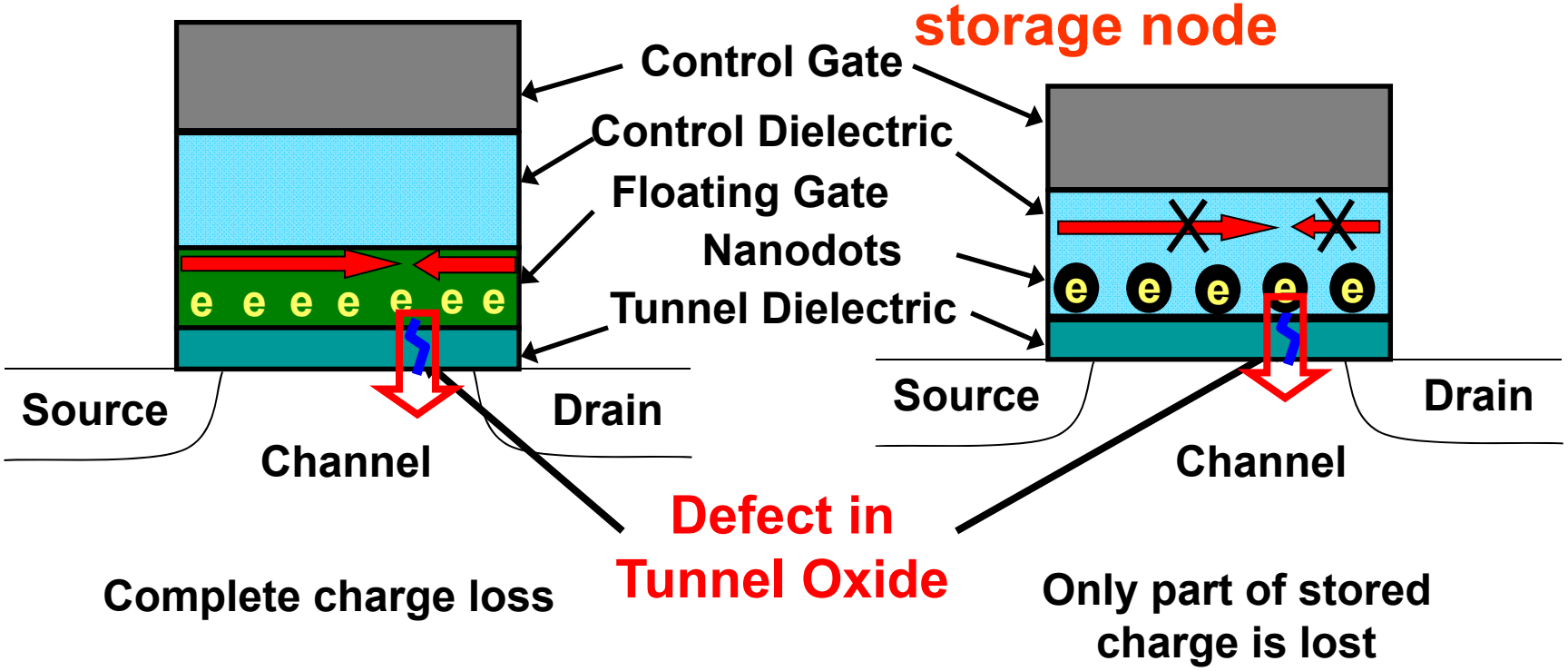
Values of carrier effective masses, band gaps and dielectric constants taken from published literature

Summary

- New models for electric field dependent capture cross section has been proposed which gives excellent agreement with experimental results
- The robustness of the simulator is verified across different stack thicknesses and different nitride compositions to accurately predict the P/E and ISPP transients

Metal Nanodot (m-ND) Flash: Motivation

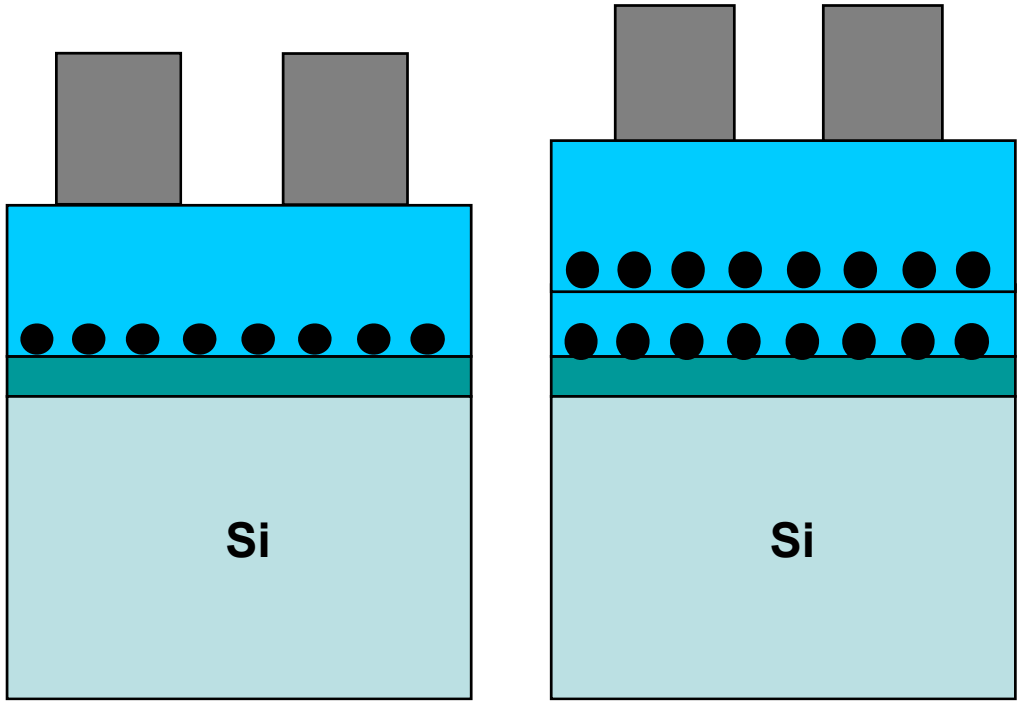
- Floating Gate Cell
  - **poly-Si storage gate**
- **Nanodot Cell**
  - **discrete nanodots as storage node**



Charge storage in discrete nanodots increases immunity to tunnel oxide defects

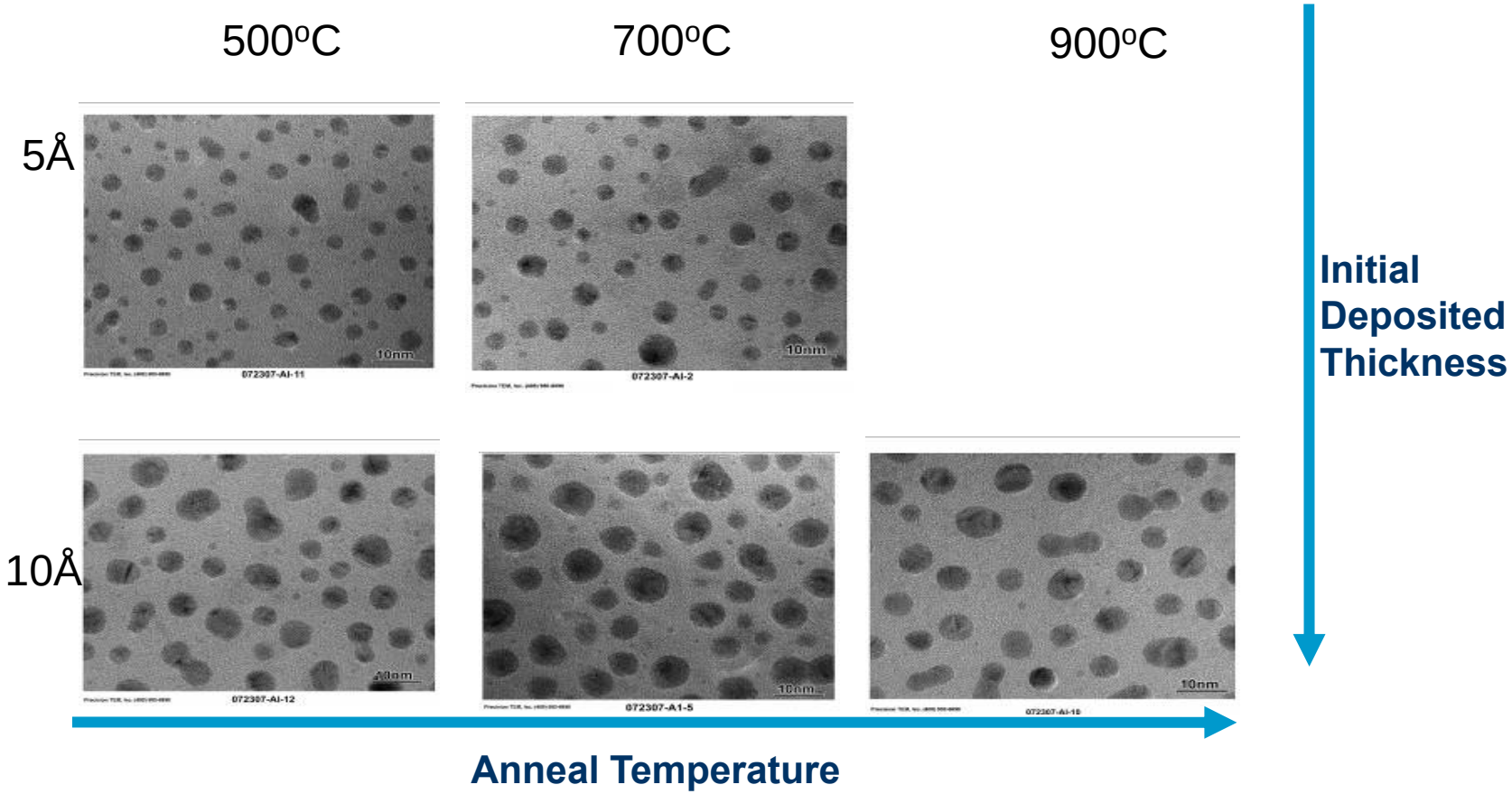
m-ND Flash Process Flow

SL	DL
Wafer Clean Tunnel Oxide 40Å Metal Deposition Anneal	
--	ILD deposition Metal Deposition Anneal
Control Oxide: 120Å Al_2O_3 Post Deposition Anneal Metallization: 1000Å Pt	



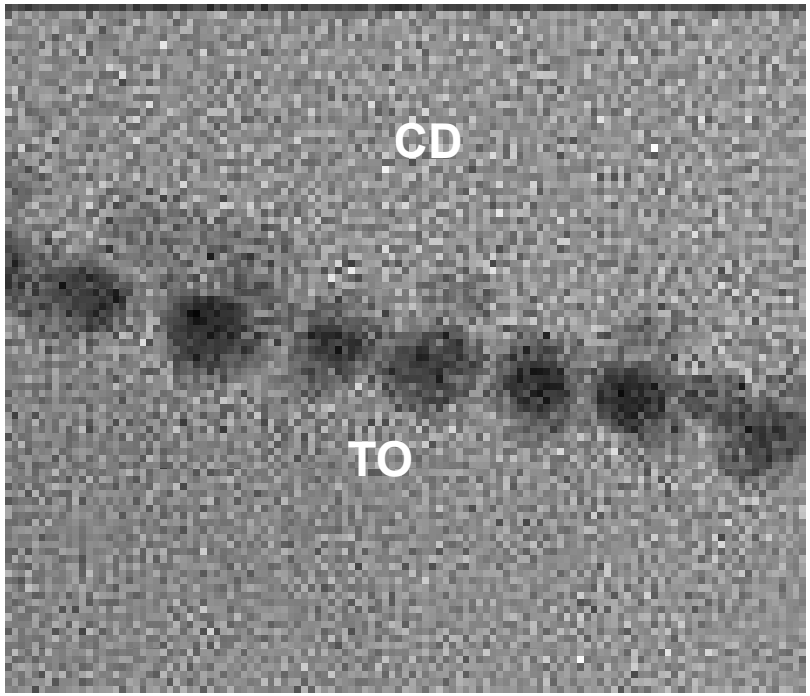
Single Layer (SL) Dual Layer (DL)

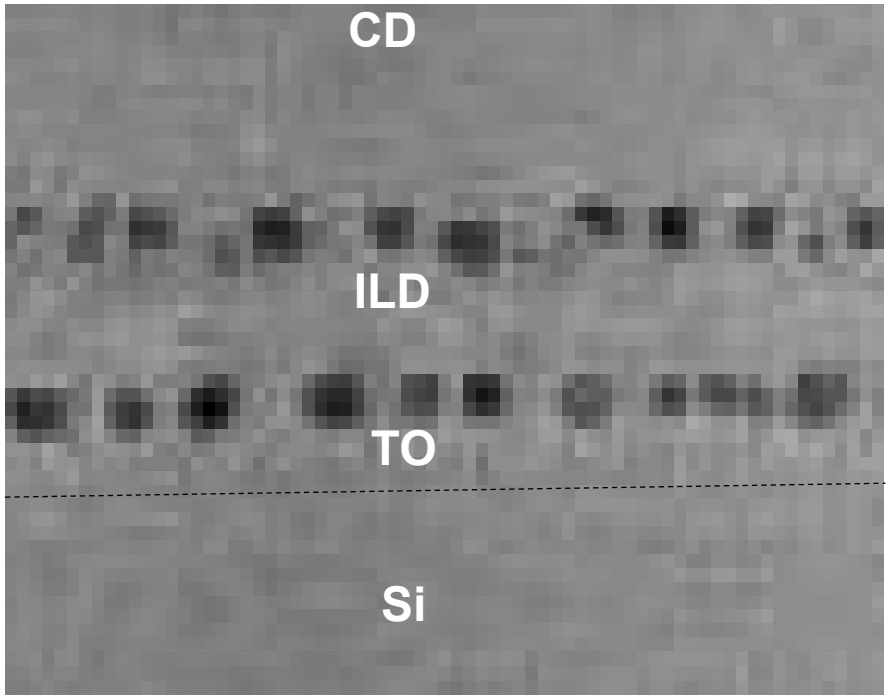
Pt Nanodot formation



Optimization of deposition and annealing processes results in large density (~$4x10^{12}cm^{-2}$), small size (~3nm) and large area coverage (~30%)

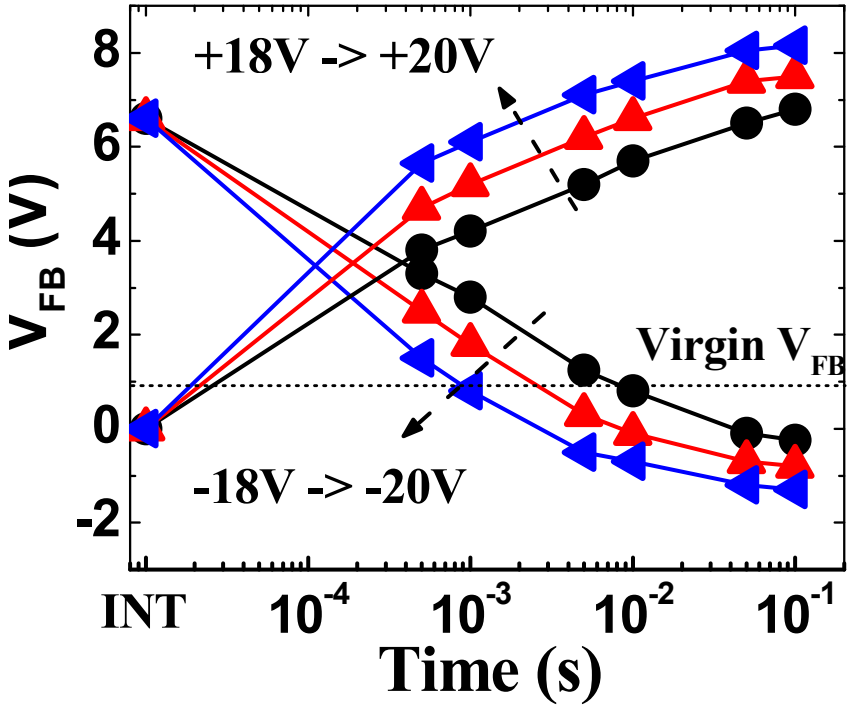
Cross-Section TEM

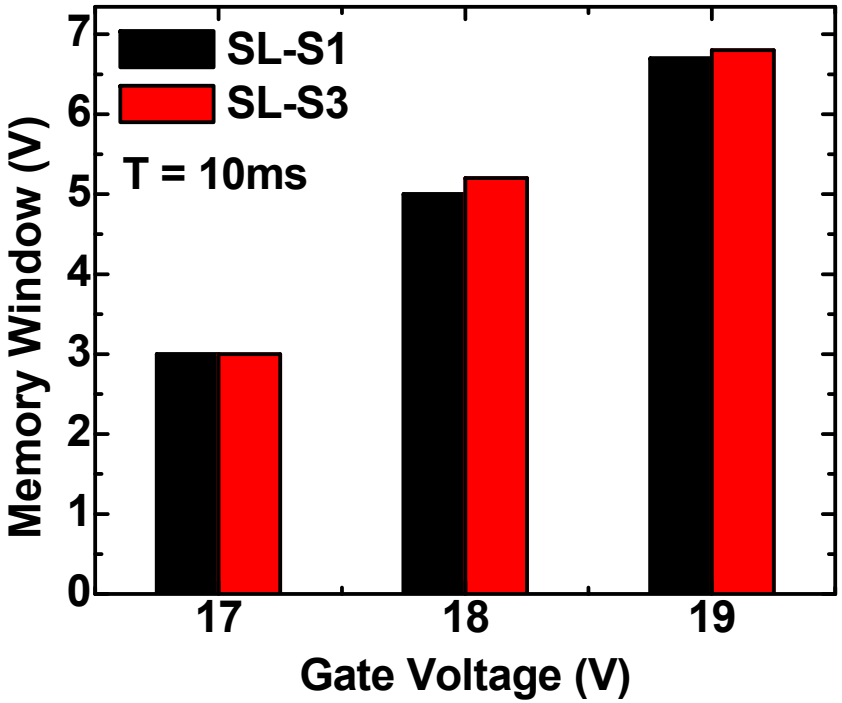




Discrete SL and DL nanodot formation clearly visible

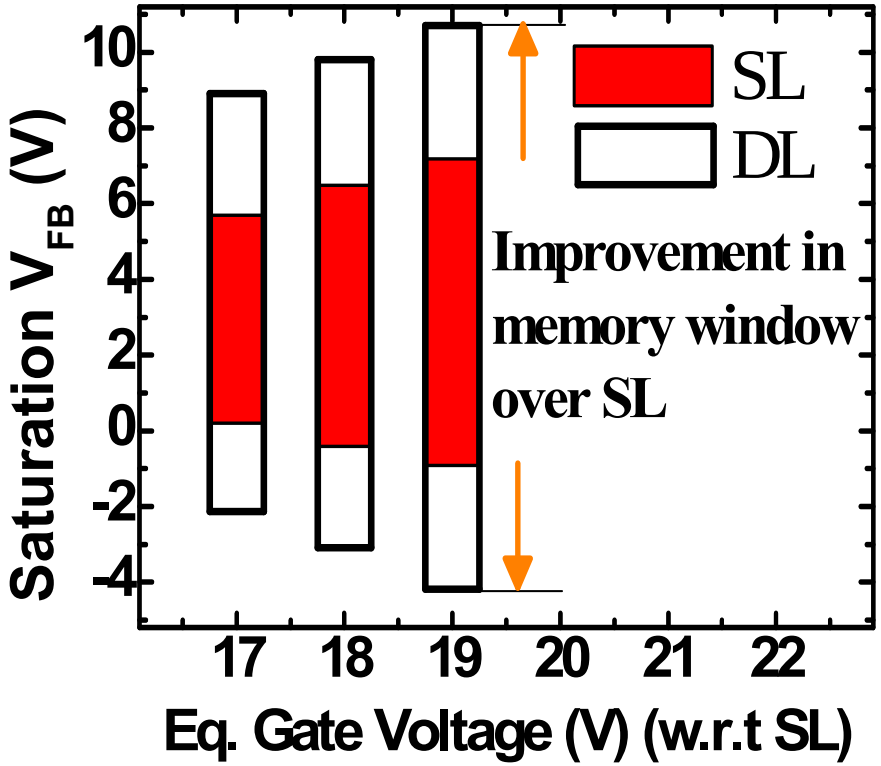
SL Memory Window

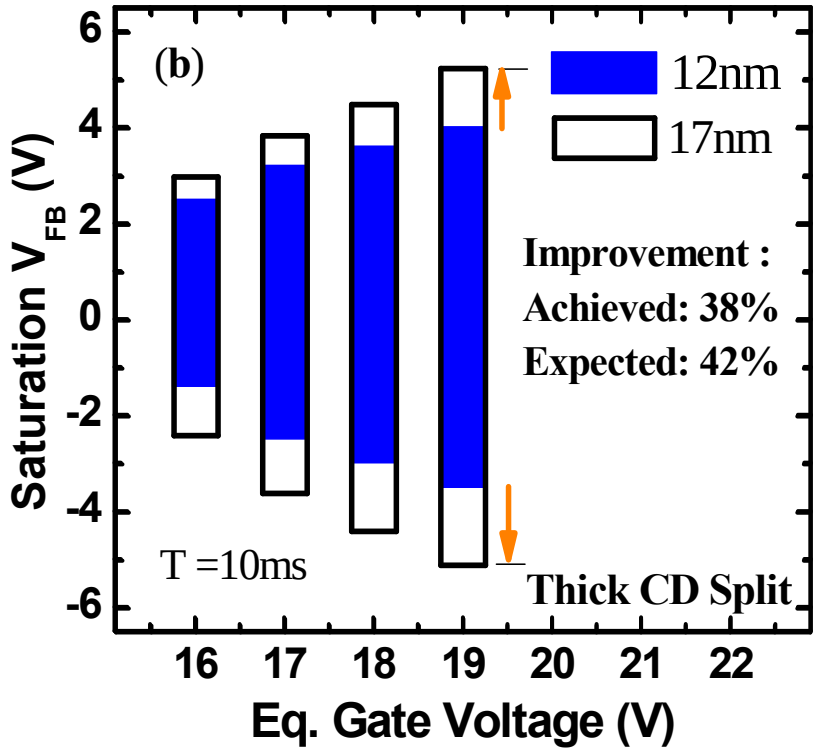




Large Memory window & significant over erase (split window possibility)

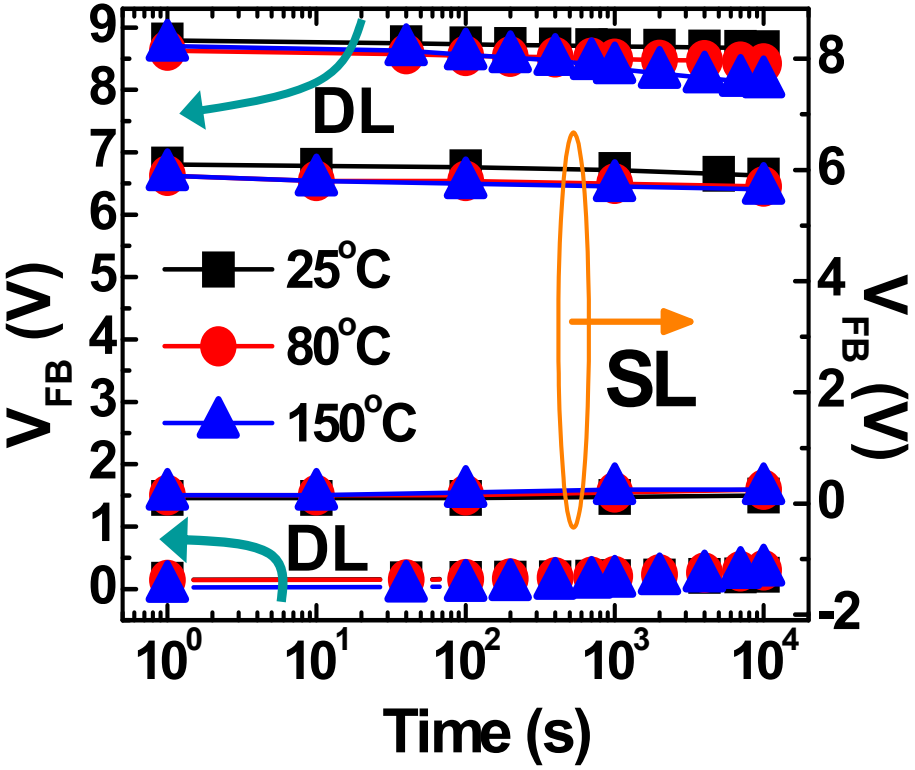
Memory Window: SL vs. DL

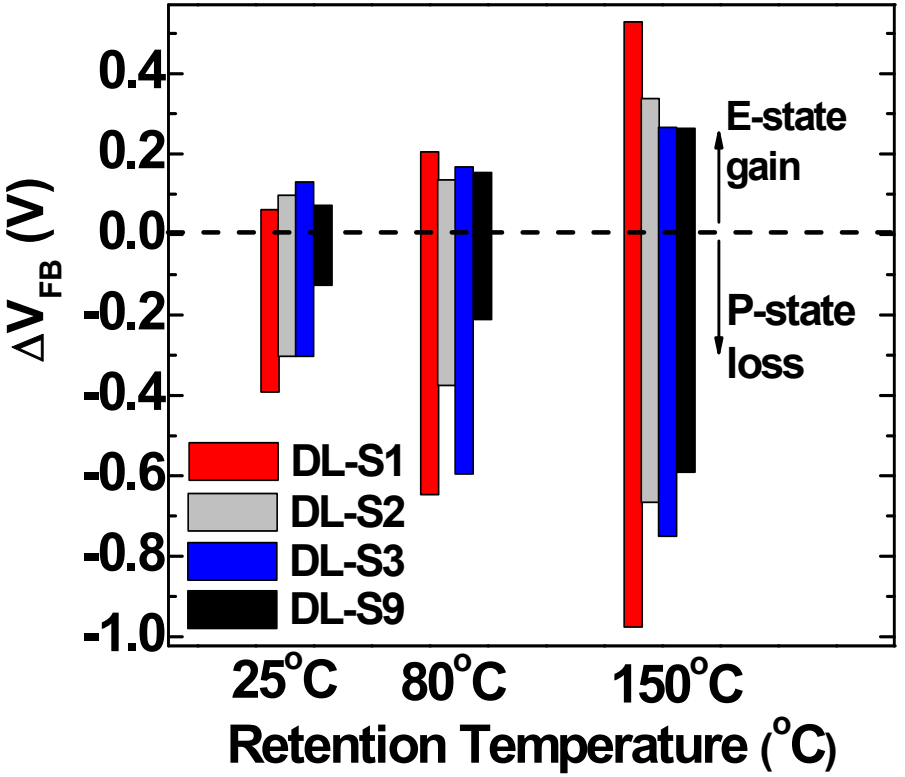




- 90% improvement in DL window over SL due to increased CD thickness and charge storage in 2nd layer
- Memory window improvement only with thick CD: 38%, expected (40%)

High Temperature Retention

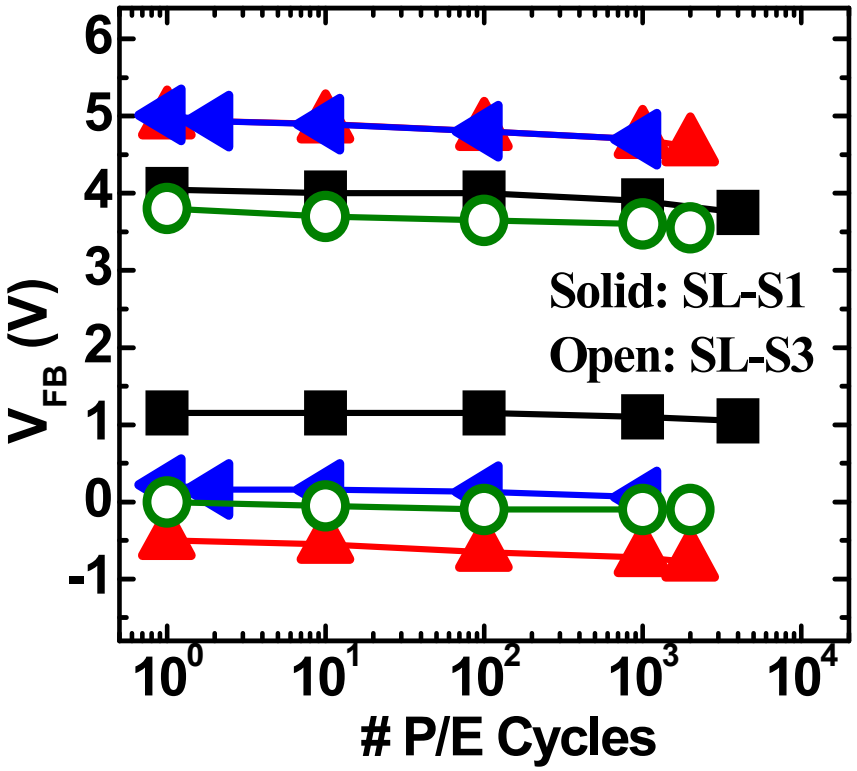


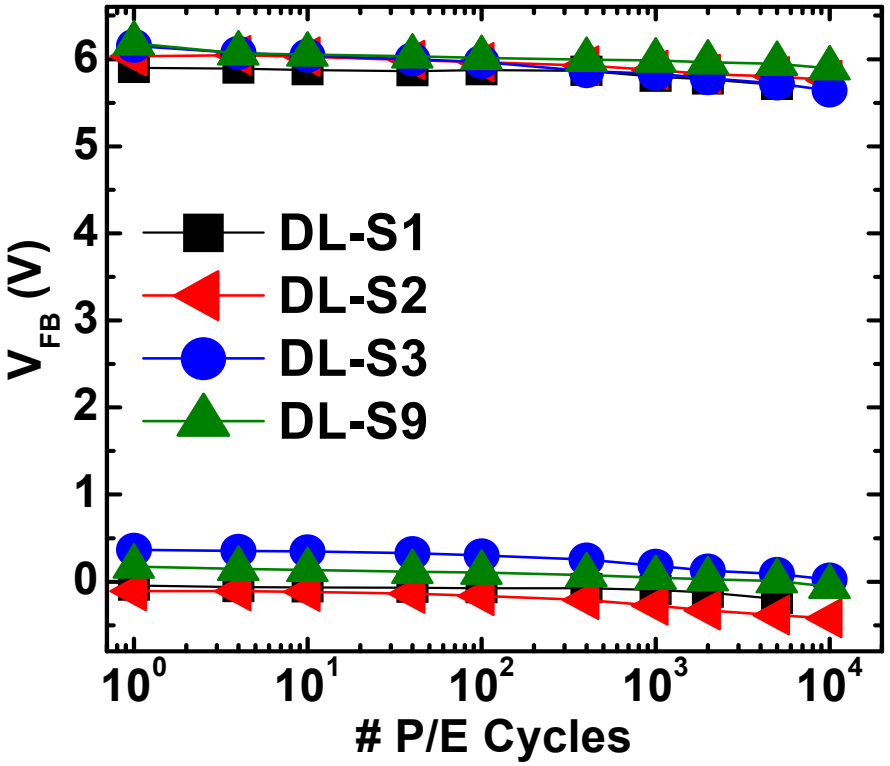


Insignificant retention loss

Retention better than SiN memory due to deeper potential well for m-ND's

SL vs. DL P/E Endurance

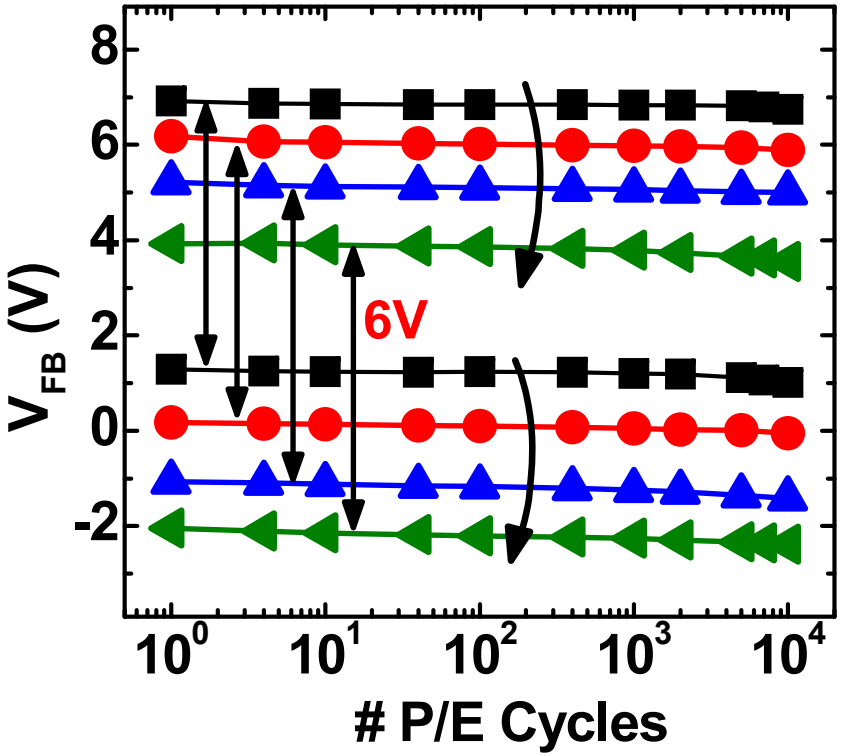


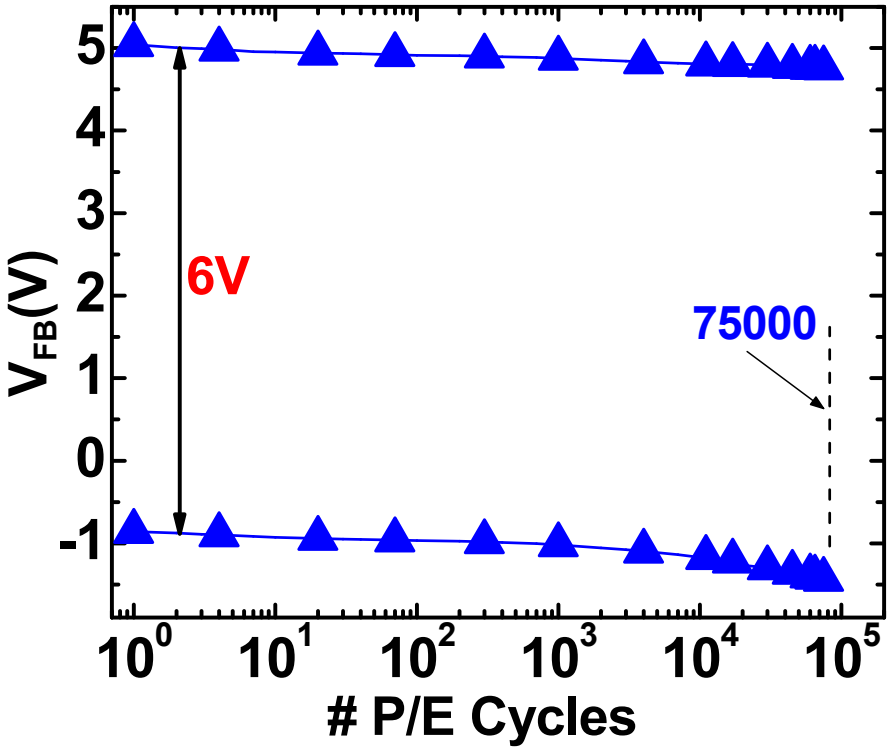


Better endurance for DL w.r.t SL

No window closure till breakdown

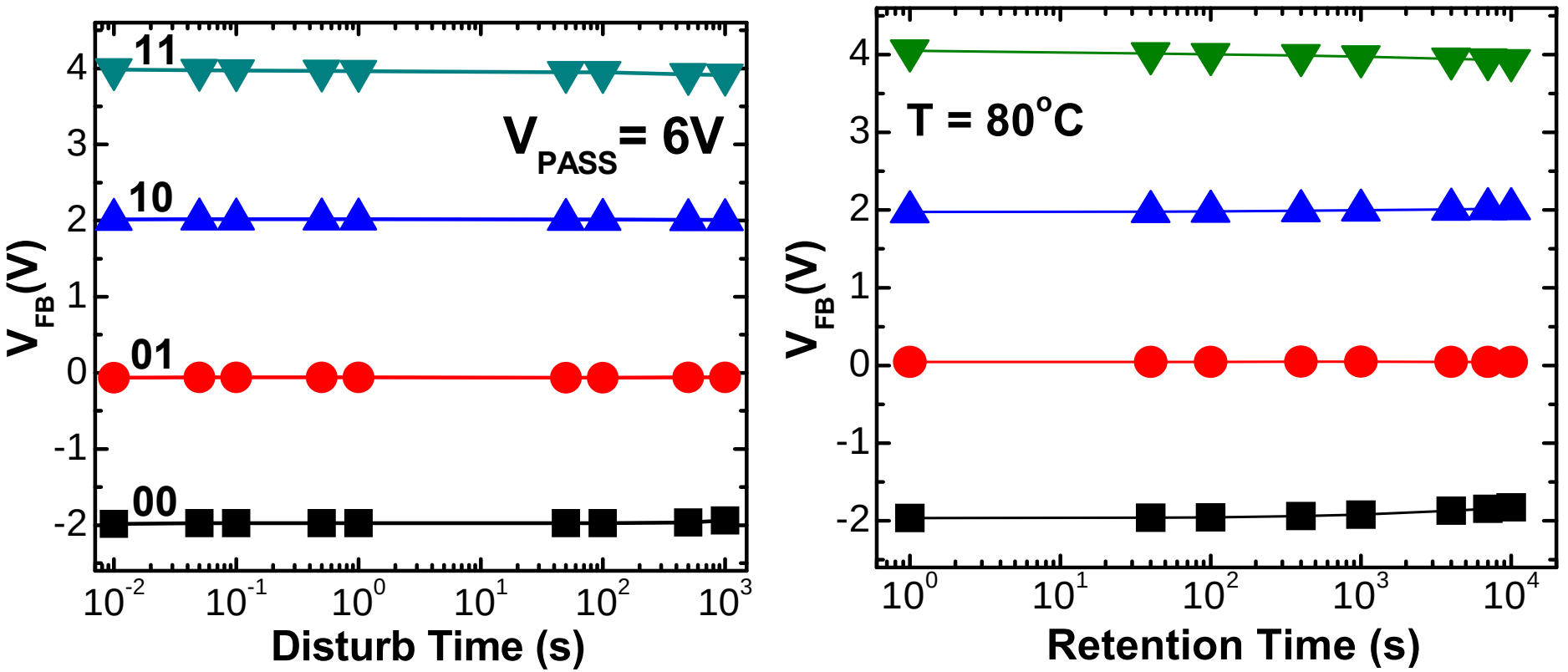
P/E Endurance (DL-S9)





- 10^4 cycles with 6V and 7V memory window, $2x10^3$ cycles with 8V memory window
- Maximum endurance seen when P/E-states are within +6V/-2V
- No window closure till breakdown

MLC Operation (DL-S9)



Excellent separation maintained between the P/E levels after read disturb and high-T retention stress

Summary

- Single and dual layer Pt metal Nanodot memory gate stacks demonstrated
- Excellent memory window, cycling endurance (>10K with 6V window), pre- and post-cycling retention
- MLC capabilities
- No fundamental reliability show stopper for metal dots in gate stack
- Need feasibility demonstration in scaled (sub 20nm node) cells

Simulation of m-ND Flash

- To demonstrate viability of m-ND cells in sub 20nm cells (impact of cell size, no. of dots, area coverage, fluctuations, missing dots, dot to dot leakage…..)

- Full 3D electrostatics and tunneling implementation

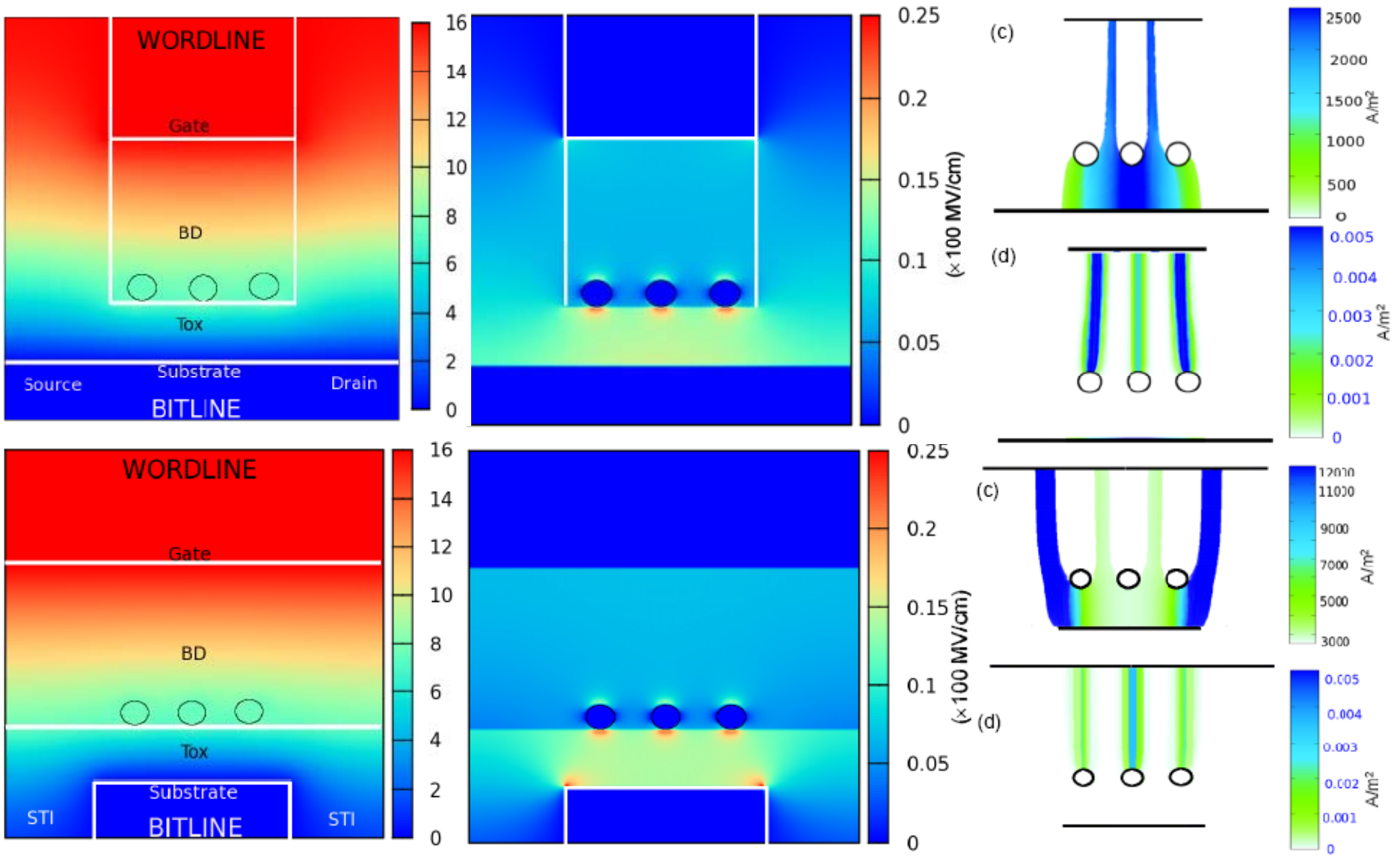
- Solve Laplace for potential & electric field in gate stack

- Non-local tunneling implementation (Tsu-Esaki) for charging of dots (substrate to dot, dot to gate, dot to dot)

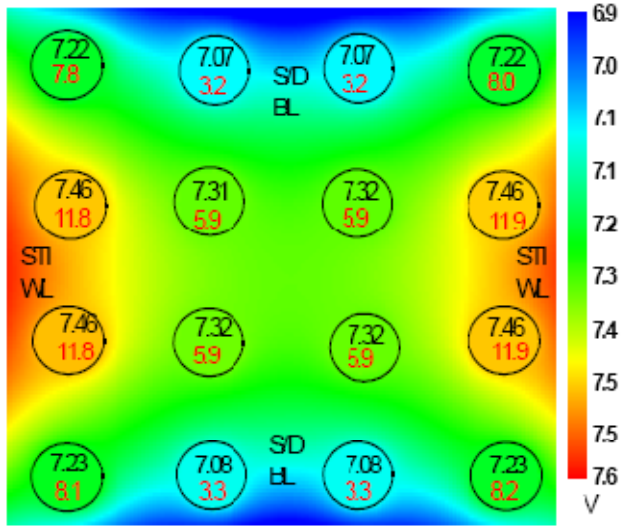
- Calculate charges in iterative manner

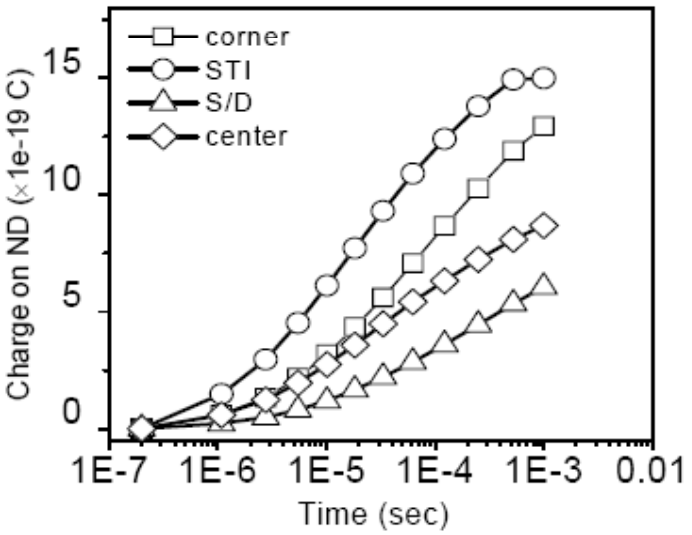
- Port dot charges in equivalent device simulated using Sentaurus Device for VT calculation

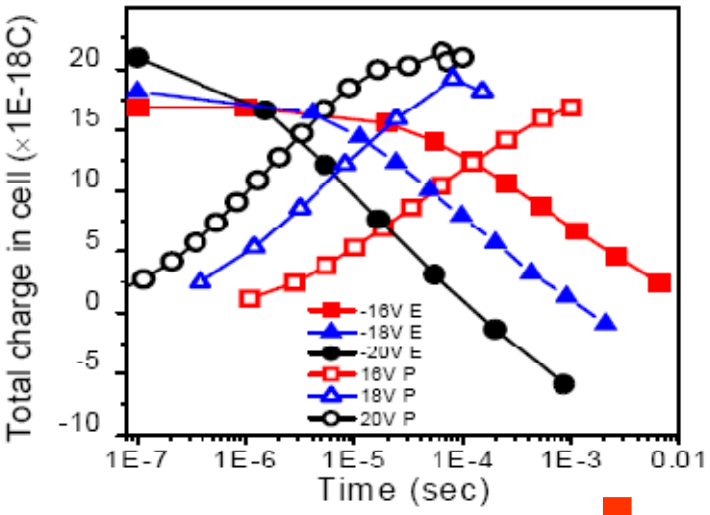
Potential, E-field, Tunnel current (2D cuts)

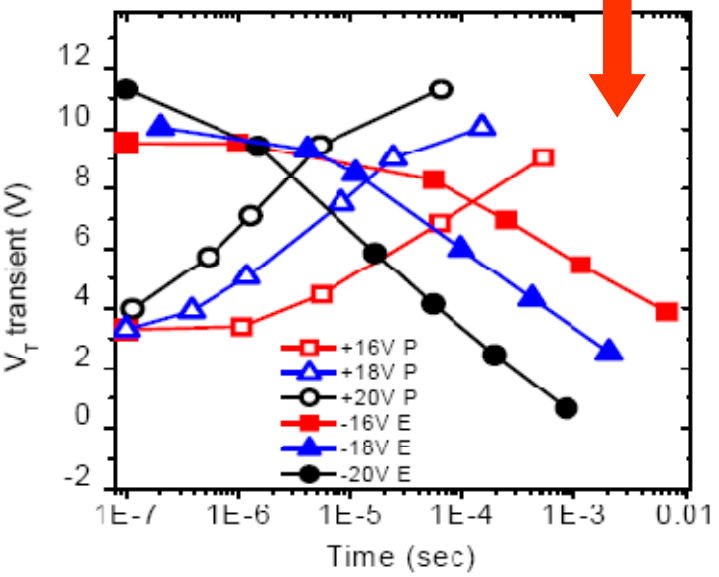


Charge Transients



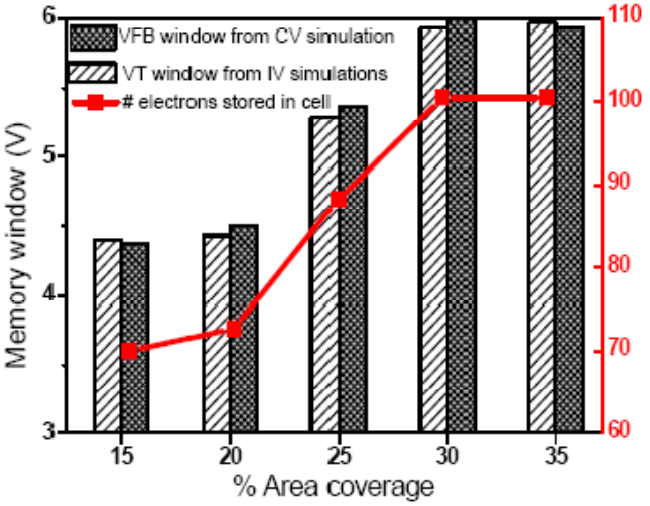


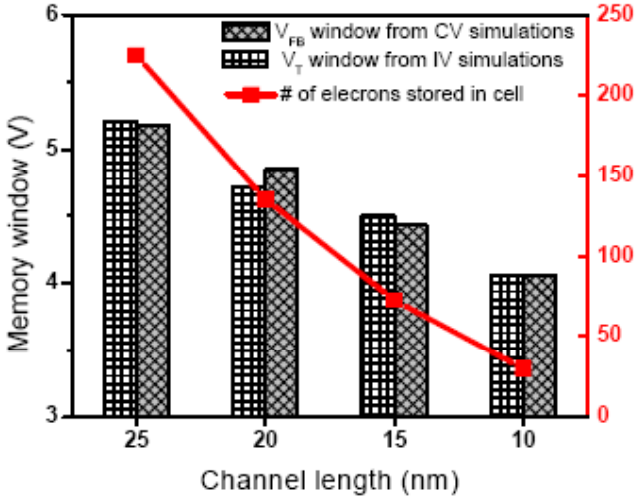


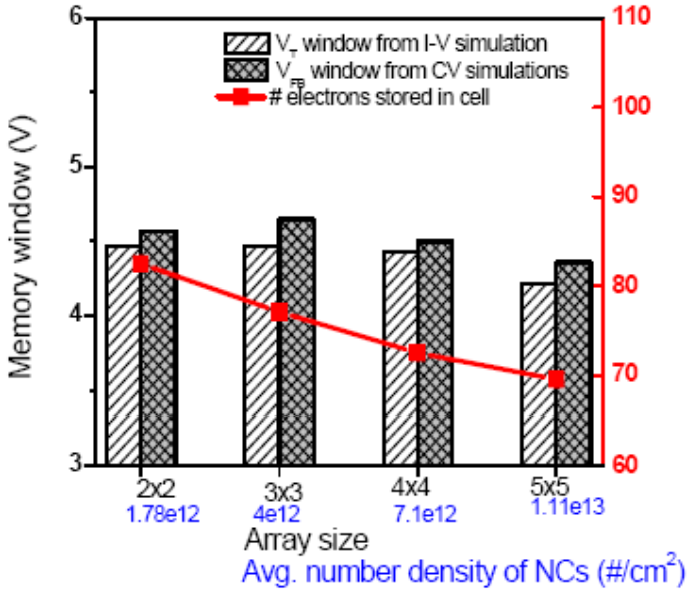


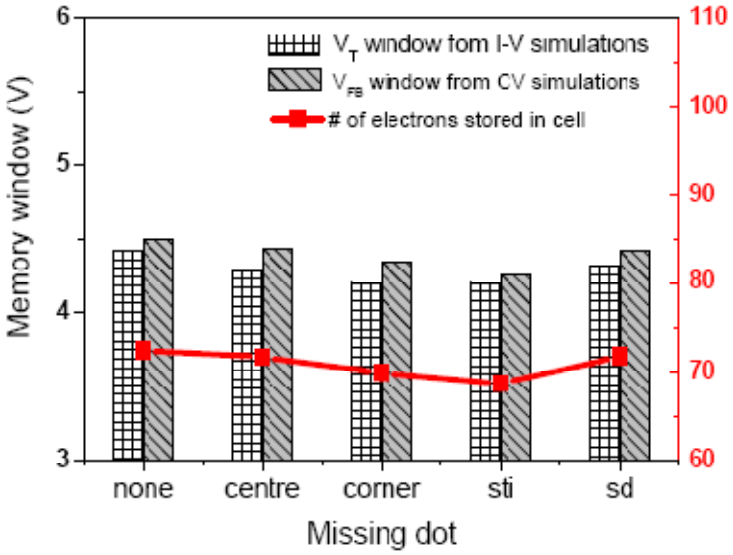
Prediction….

Area coverage, Channel length, No. density, Missing dots…









Summary

- **Full 3D electrostatics – tunneling framework to study m-ND Flash viability below 20nm node**
- **Immunity to fluctuations (good)**
- **Memory window reduction with L scaling (issue)**
- **Cells becomes edge critical (issue)**