Advanced NEMFET-based Power Management for deep-submicron Integrated Circuits

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Motivation

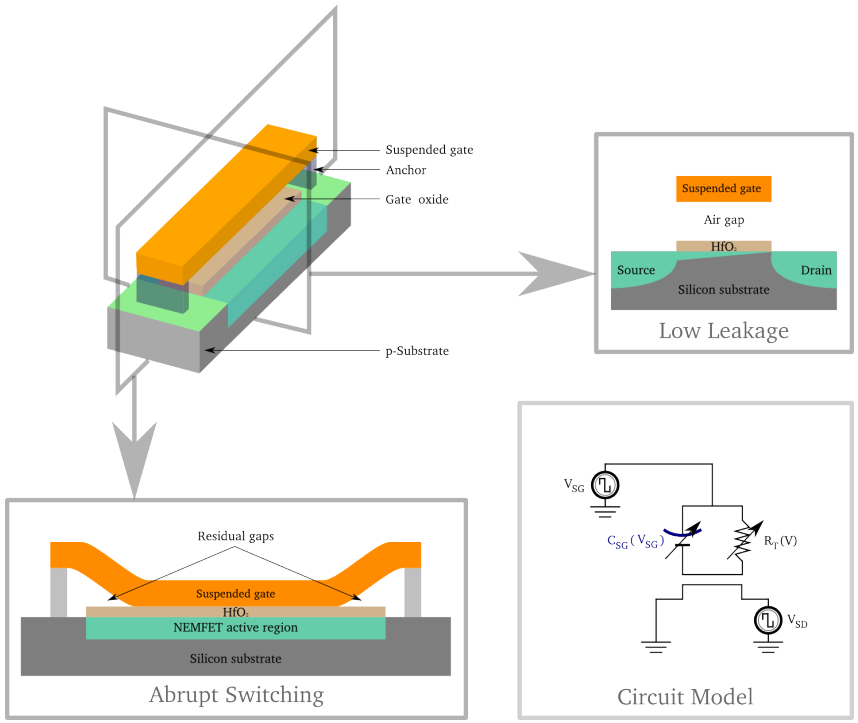
- CMOS technology is approaching its physical limits.
  - Emerging technologies have been investigated and proposed to supersede the MOSFET, e.g., Nano-Electro - Mechanical FETs (NEMFETs), carbon nanotubes, quantum dot cellular automata, single-electron devices.
  - Only low complexity circuits were successfully designed with the above technologies.
- 3D-Stacked IC (3D-SIC) may provide a smooth transition between CMOS and emerging devices.
  - It is a technology that potentially provides heterogeneous integration, higher performance, and lower power consumption, when compared to planar ICs.
- Scaling CMOS technology could still provide 30% improvement in performance at the 28 nm node with respect to the 40 nm node.
  - Tremendous increase of power dissipation of digital CMOS.
  - The life of the battery operated embedded systems with low activity, which is mostly determined by the standby leakage power dissipated by the circuit in sleep mode, is directly affected.

We address

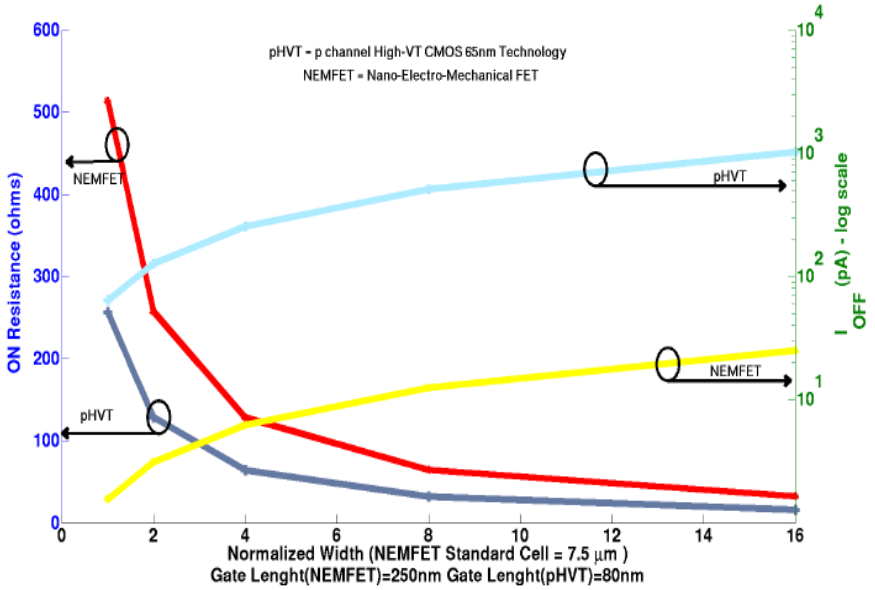
A Hybrid CMOS-NEMS 3D Stacked Chip Power Management Architecture.

NEMFET Background

NEMFET Geometry / Equivalent circuit

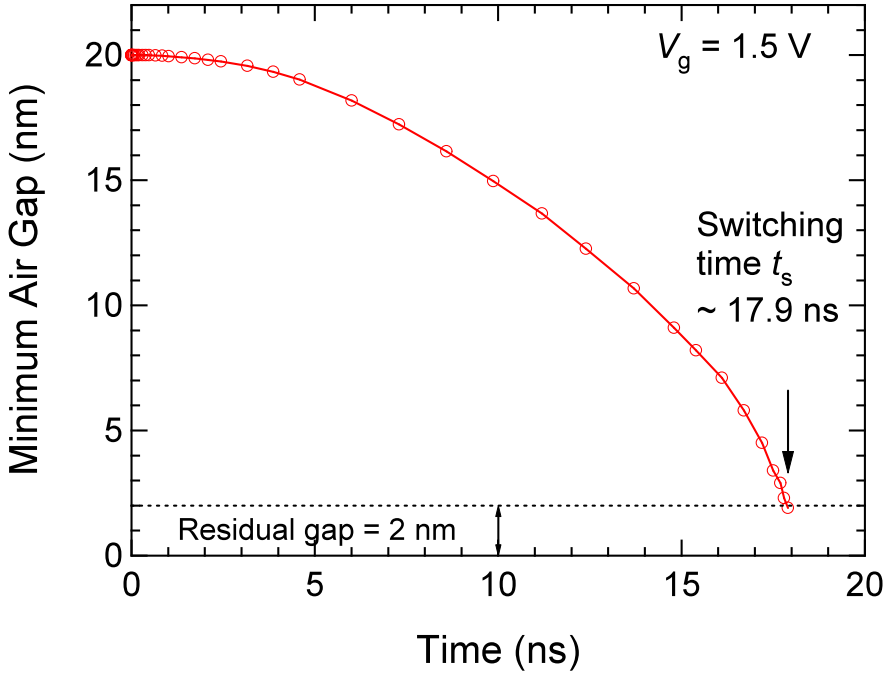


Static Analysis 65nm CMOS High-VT vs. NEMFET



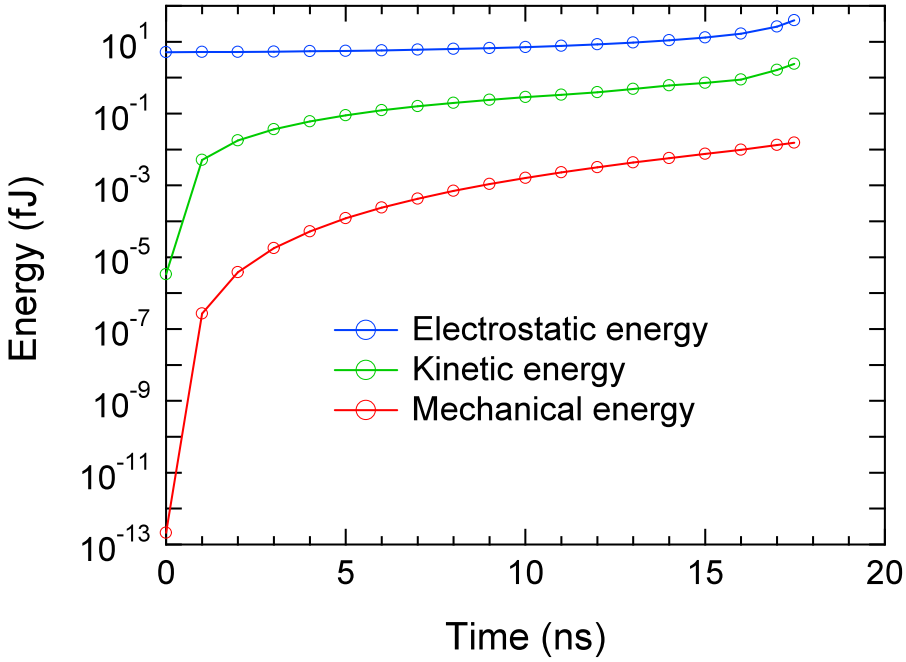
NEMFET Dynamic Behavior

Transient calculation (Pull-in)



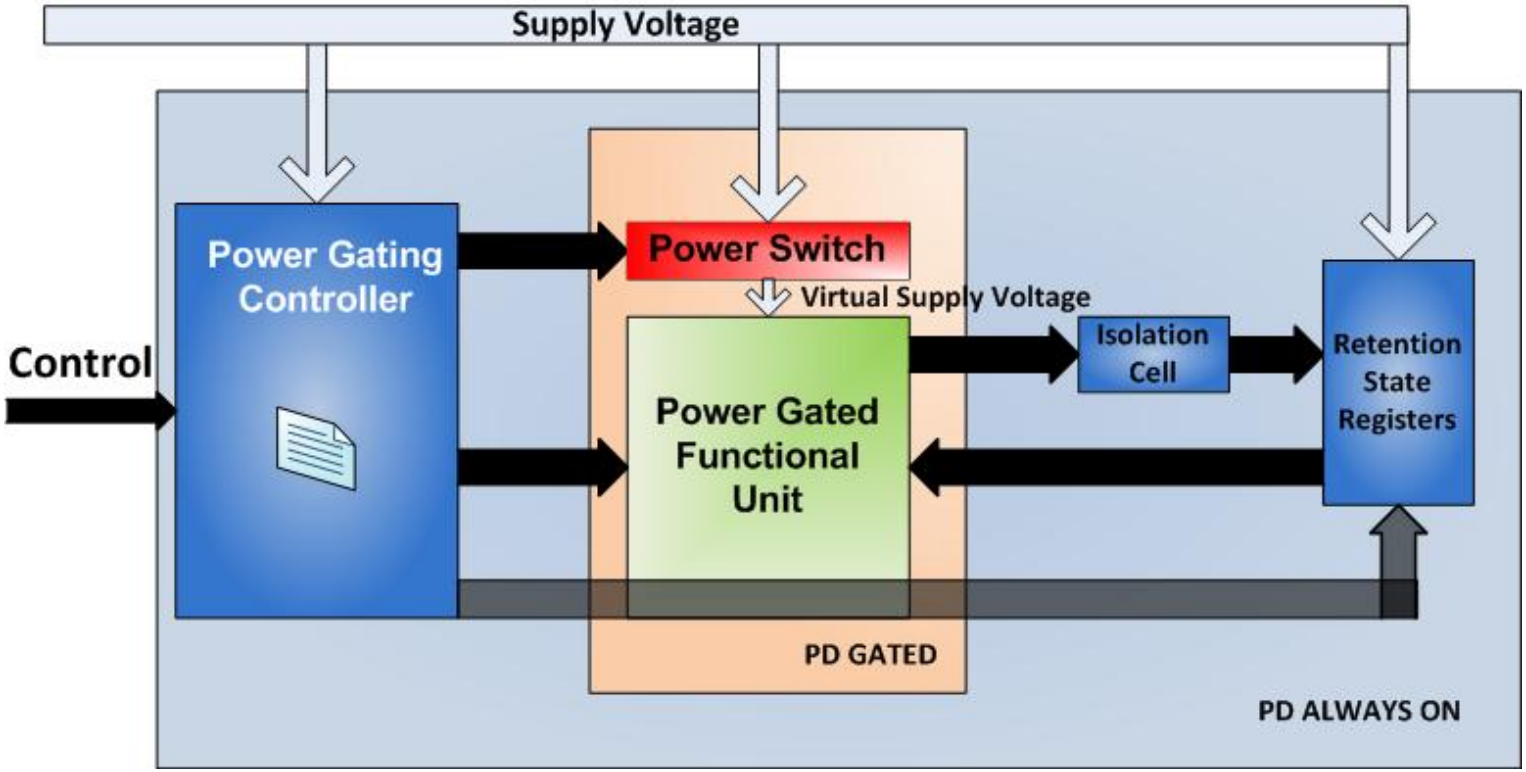
Switching time ~ 17.9 ns

Energy consumption (Pull-in)



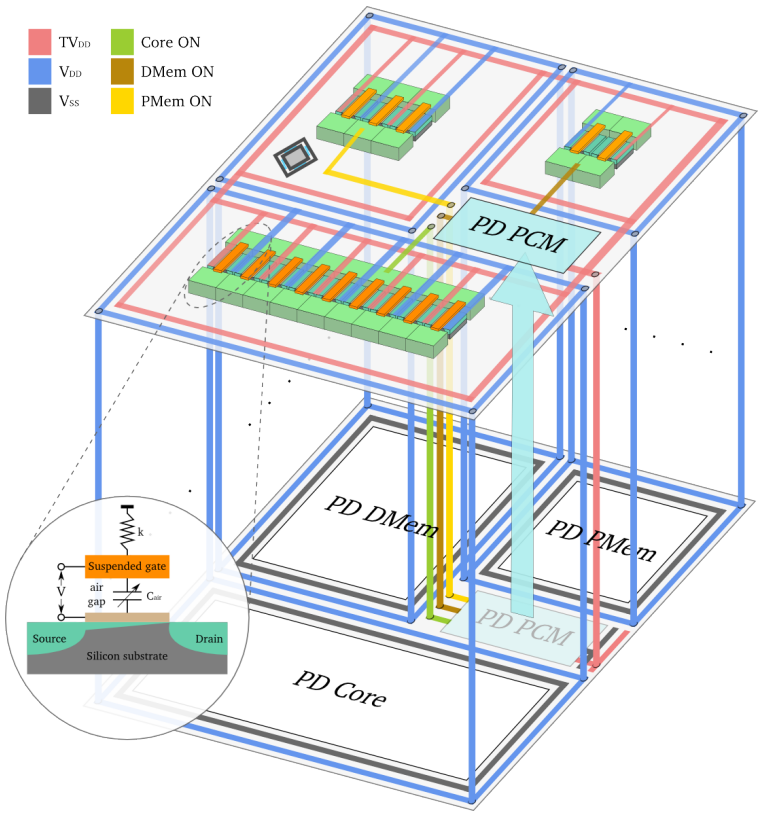
Energy consumption ~ 39.7 fJ

Power Management



3D Power Management

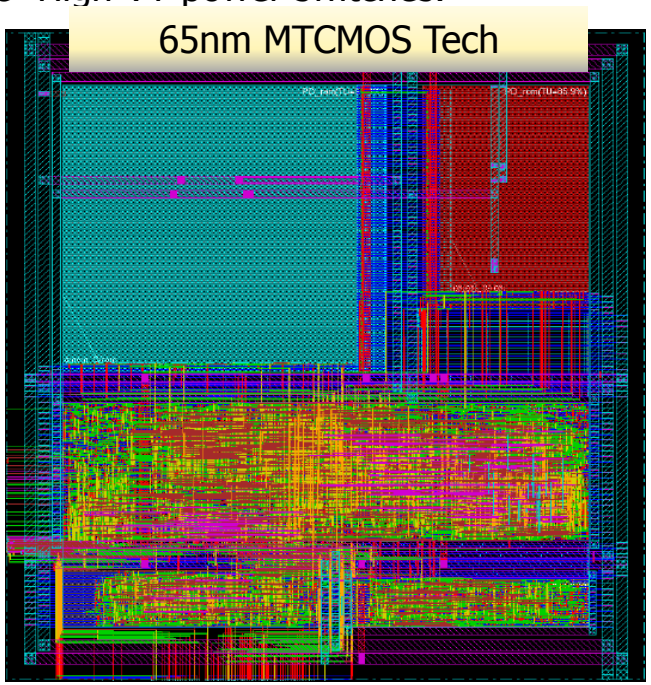
Towards "Zero-Energy"



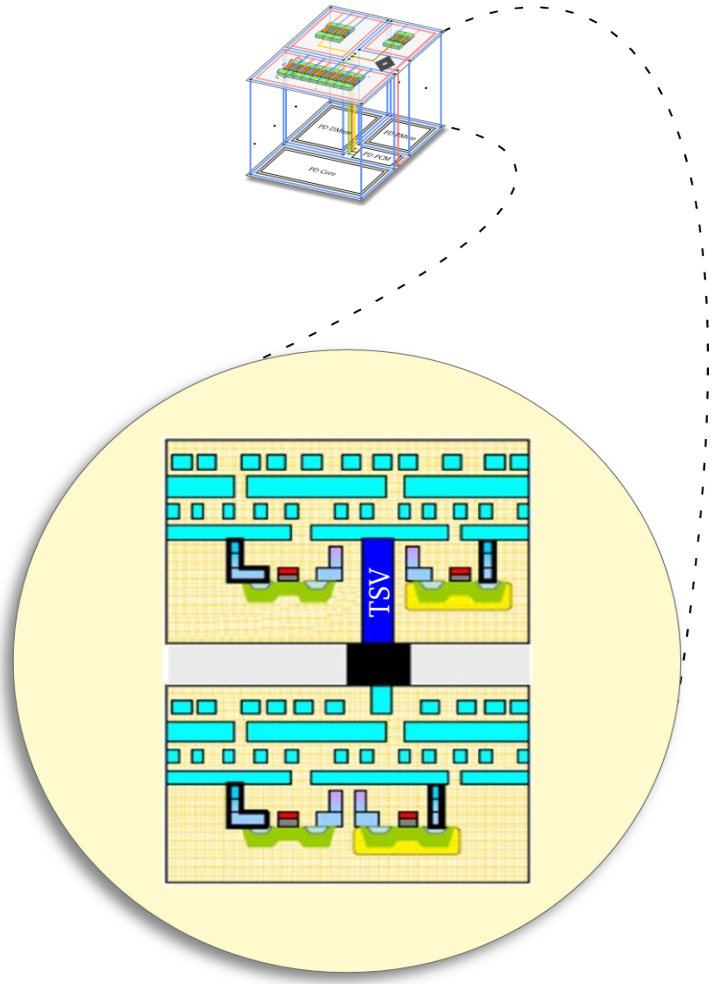
- Area reclaimed on the CMOS Tier
  - Signal interconnect length inside/ between gated components,
  - "True" VDD (TVDD) supply rings surrounding gated blocks are translated to the NEMS tier.
- Easy to integrate hybrid devices technologies
  - Low-leakage NEMFET device,
  - Energy scavengers,
  - Temperature sensors, etc.
- IP Reuse
- Power management controller and always-on cells placed on:
  - CMOS tier or NEMS tier.

A Case Study

- Heart beat rate monitor - Detects QRS complex in an Digitized Electrocardiogram (ECG).
  - Step 1. Identifies the R peaks in the ECG signal.
  - Step 2. Measures the interval between two consecutive R peaks.
- Four Designs
  - *Reference* Design – 1 TIER design with "classic" High-VT power switches.
    - **16-bit openMSP 430**
    - DMEM - 2kB SRAM
    - PMEM - 4kB ROM
    - Peripherals
  - *Stacked* Design – 2 TIER design
    - Bottom TIER – openMSP430 based SoC
  - *Hybrid* Design – 2 TIER design
    - Bottom TIER – openMSP430 based SoC
    - Top TIER – **PSO devices**: NEMFETs
  - *Leakage Enhanced* Design – 2 TIER design
    - Top TIER – **PSO devices**: NEMFETs
    - Top TIER – PSO and **PM Cells**: NEMFETs



A Case Study (2)



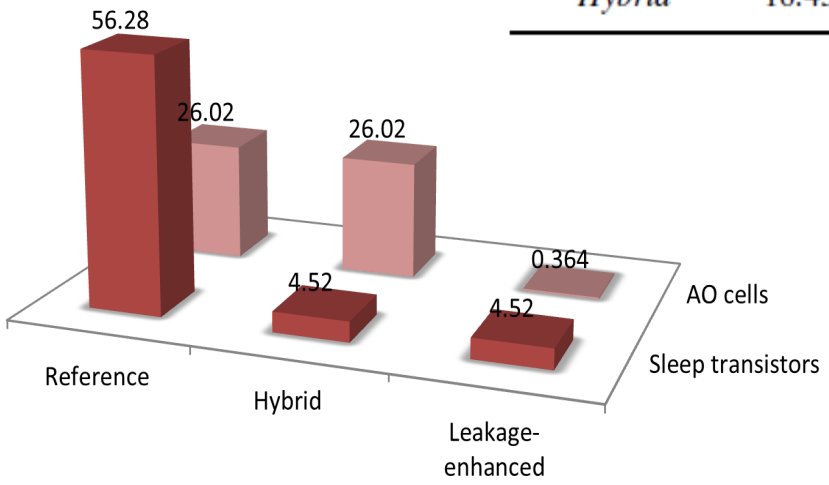
- Large metal vias connecting adjacent dies
- 5 μm diameter
- 20 μm length
- 10 μm pitch
- R ≈ 0.2 Ω / entire TSV ➔ low IR-drop in ON state
- C ≈ 40 fF ➔ limits the granularity of the power gating

TSV model based on Katti et. al. (IEDM, 2010)

Delay and Leakage Analysis

- Delay degradation
  - "interruption" of the power/ground (P/G) rails by the power switch
  - IR Drop on the power supply net

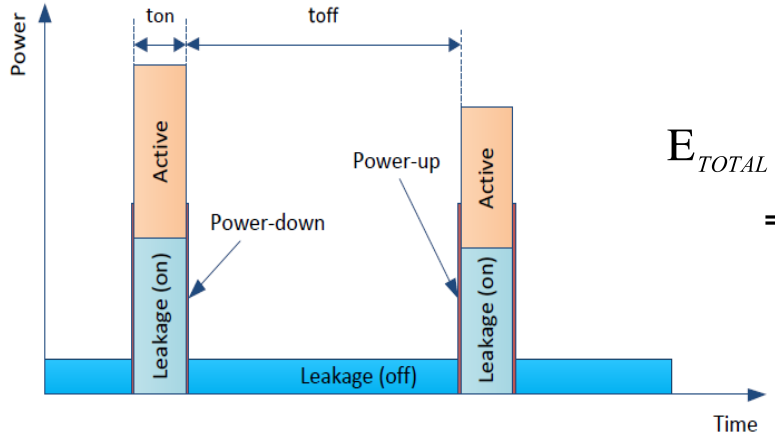
Implementation type	Average IR-Drop [mV] on STs	on V_{DD} Rail	Total	Clock period [ns]	IR Drop aware clock period [ns]
Reference	71.40	35.73	107.13	6.577	6.855
Stacked	4.46	35.55	40.01	6.426	6.525
Hybrid	18.43	35.55	53.98	6.426	6.561



Leakage Roadmap

Energy Analysis

Power Execution Trace



Energy Analysis

$$\mathrm{E}_{TOTAL} = T_{ON} \cdot P_{ON} + T_{OFF} \cdot P_{OFF} + \mathrm{E}_{TRANS}$$
$$= T_{ON}(P_{ACTIVE} + P_{LEAK,ON}) + T_{OFF} \cdot P_{LEAK,OFF} + T_{TRANS} \cdot P_{TRANS}$$

1292 cycles
sampling data analysis

2036 cycles
heart beat detection

Cycles = 198.5 *1292 + 1.5 *2036 = 259516

Energy Analysis (2)

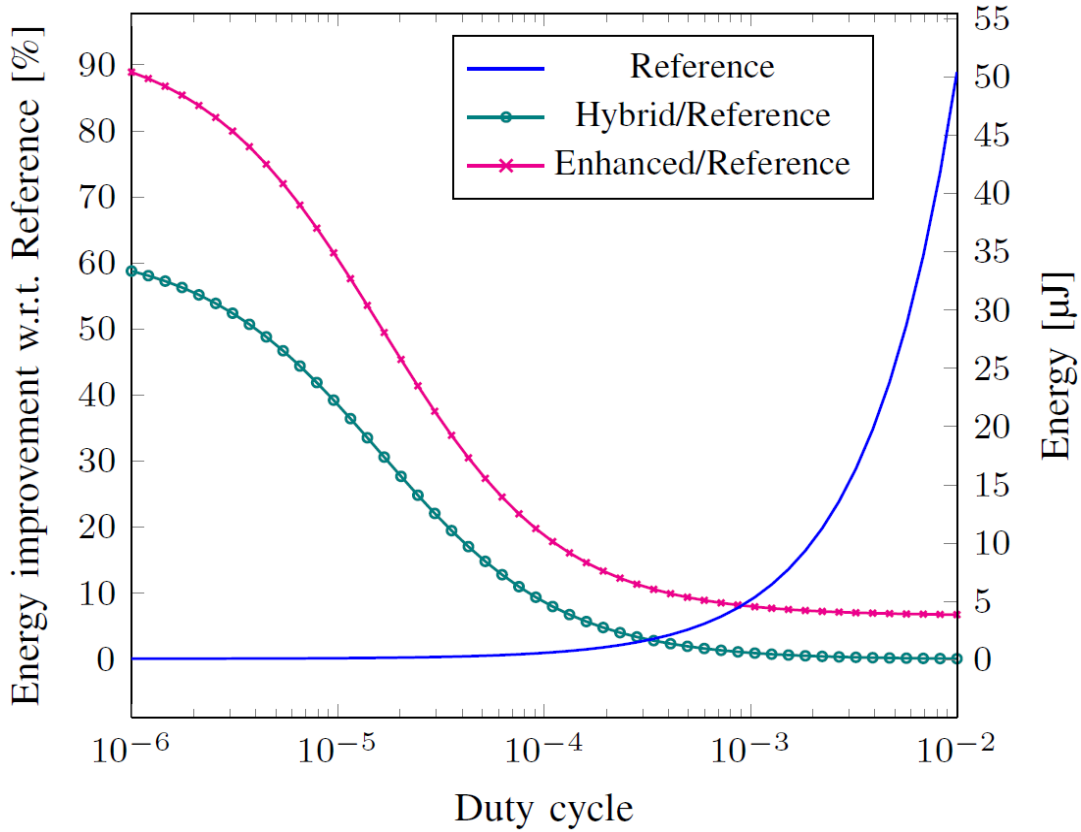
Implementation type	ON power [mW]	OFF power [nW]			Power-up energy [pJ]	Total energy [µJ]	Energy-Delay Product [µJ·ns]
		STs	Always-on cells	Total			
Reference	5.0340	56.28	26.02	81.28	48.04	9.05	62.01
Hybrid	5.0339	4.52	26.02	29.52	37	8.61	56.47
Leakage-Enhanced	4.7	4.52	0.364	4.884	37	8	51.48

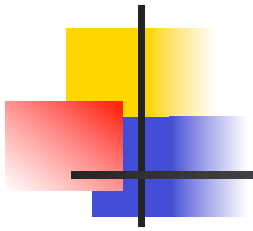
Active time = 1.73 ms, Idle time = 993.35 ms, Transition time = 5.32 ms @ 150 MHz

Improvements	16.64X	17%

- State-of-the-art piezoelectric vibration scavengers from Aktakka et. al.:
  - power density of 6.45 µW/mm^3/g^2
- Our assumptions:1g constant acceleration
  => for 8µJ, 1,24mm^3

Duty Cycle vs. Energy Improvement





Conclusions

- The proposed architecture can help ubiquitous embedded nano-systems cope with very tight energy budgets.
- Promising candidate in reaching truly "zero-energy" ubiquitous nano-systems.
- Specifically effective for low activity applications.
- Energy evaluation of the Enhanced design indicated a reduction of 7% over the 3D Hybrid architecture and of about 15% with respect to the 2D CMOS counterpart.
- For applications with lower activity, the potential energy improvement can reach up to 90%, with respect to the 2D CMOS Reference design.