Designing CMOS Wireless System-on-a-chip – analog/RF perspective

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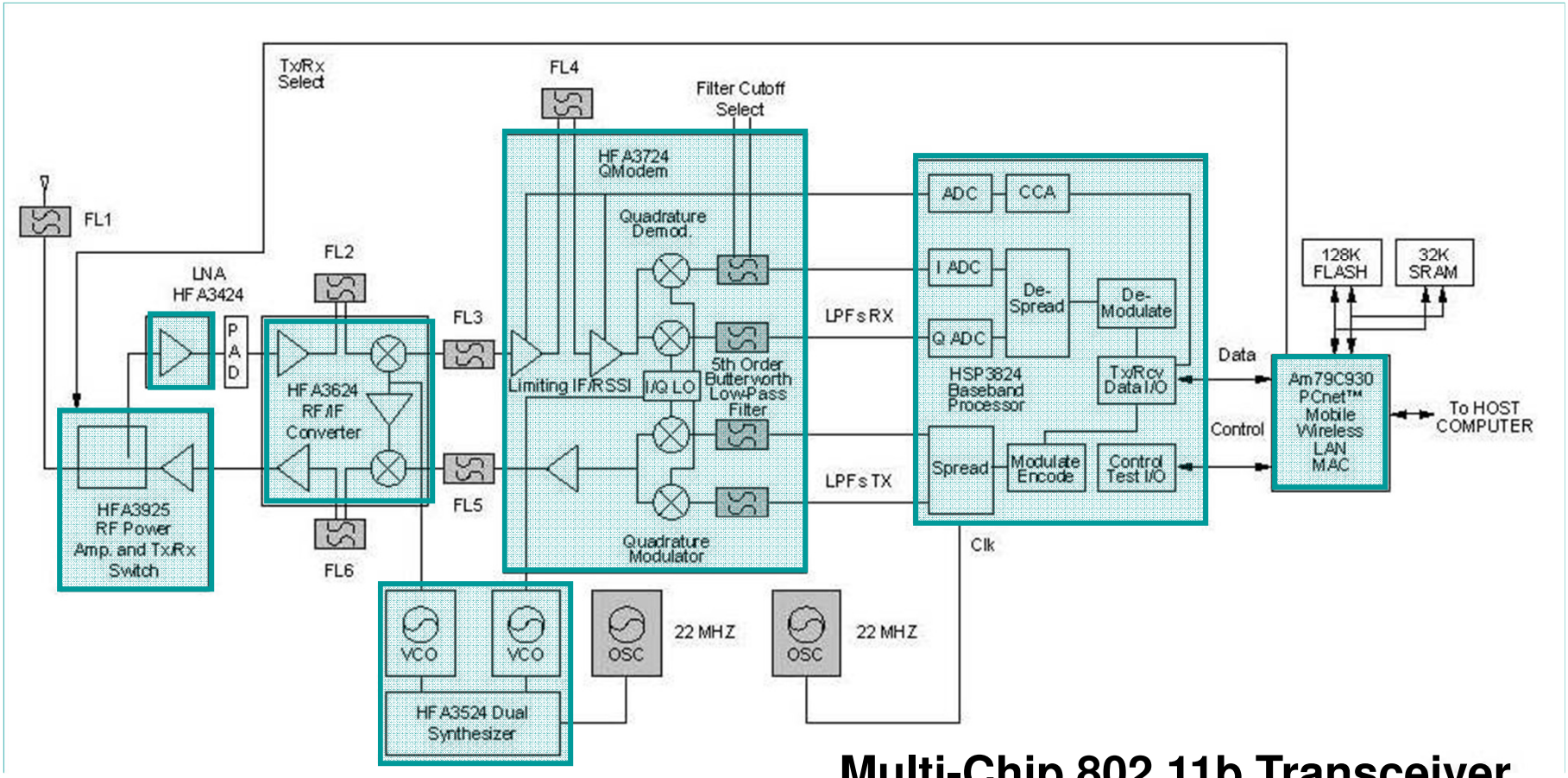
Japan, Nov 2011

Outline

- System-on-a-Chip Overview
  - Transceiver Building Blocks
  - Integration issues
- System-on-a-Chip Example:
  - A 1x1 802.11n WLAN SoC
    - Terrovitis et al, 2009 ESSCirC
- Conclusion

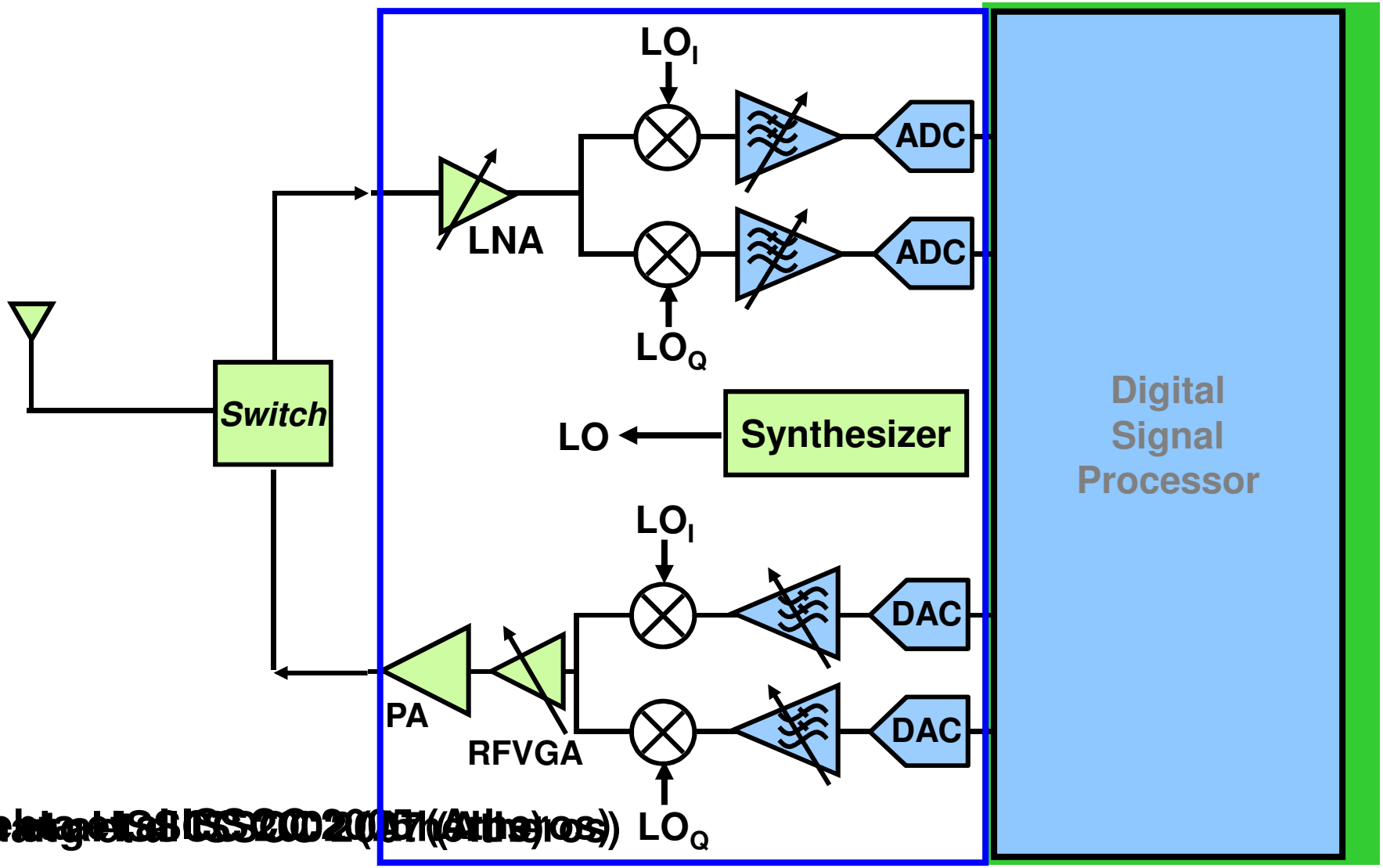
SoC Trends: WLAN (1996)



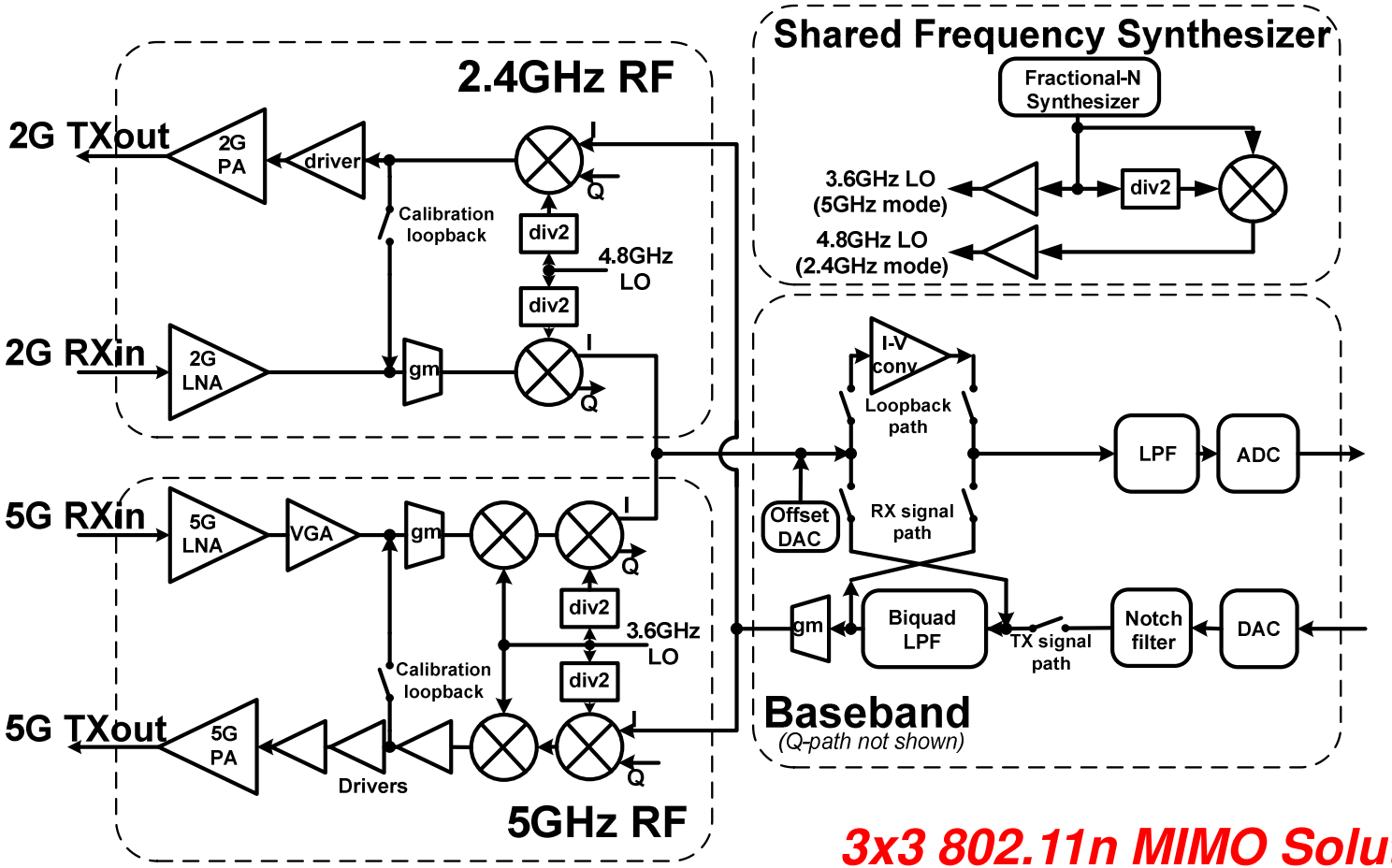
Multi-Chip 802.11b Transceiver

Prism WLAN chipset (Harris Semi) AMD App Note (www.amd.com)

WLAN Integration Story



Soc Trends: WLAN (2011)



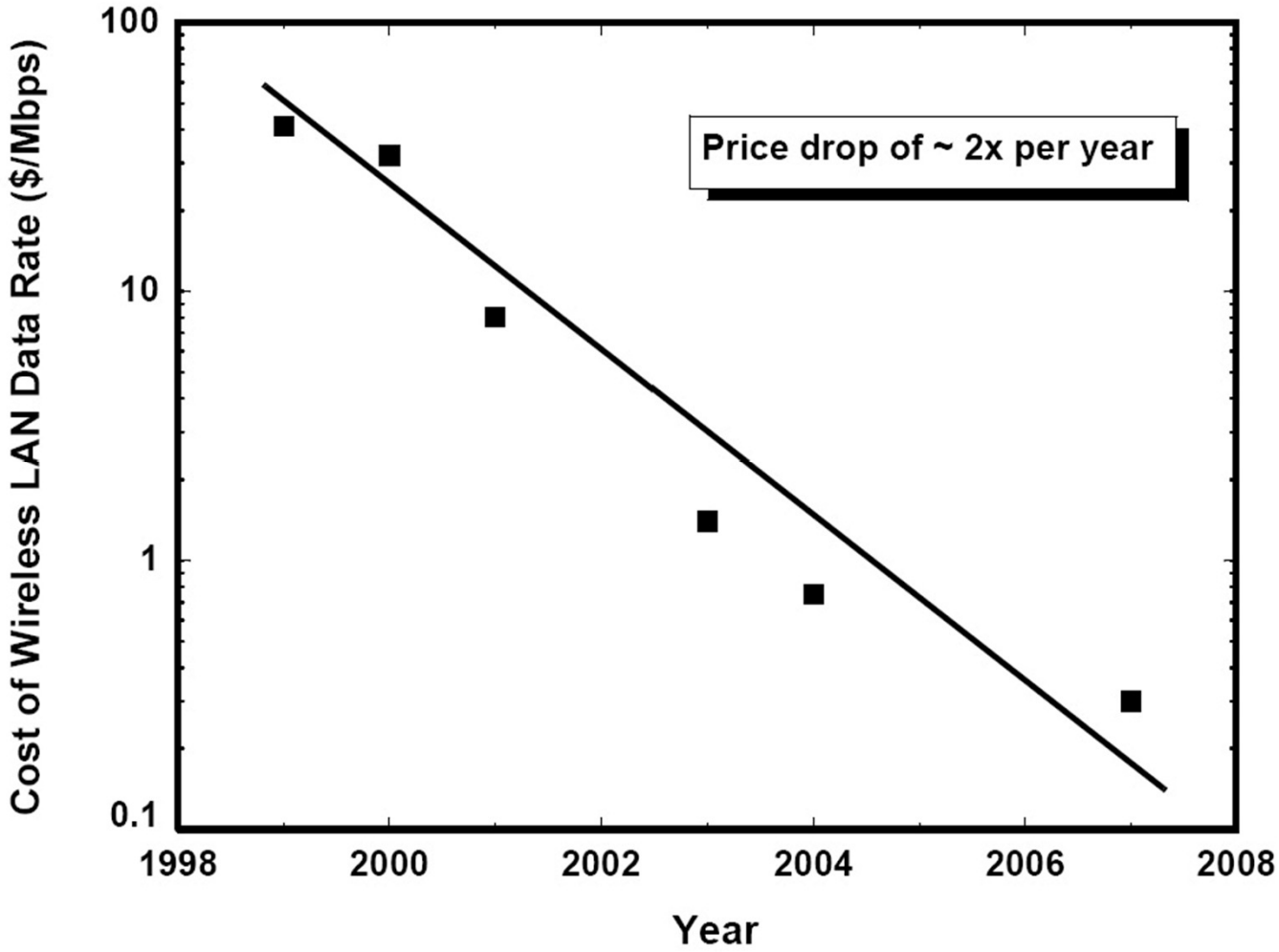
3x3 802.11n MIMO Solution
(1 of 3 chains shown)

Abdollahi-Alibeik et al, ISSCC 2011 (Atheros)

Advantages of SoC Integration

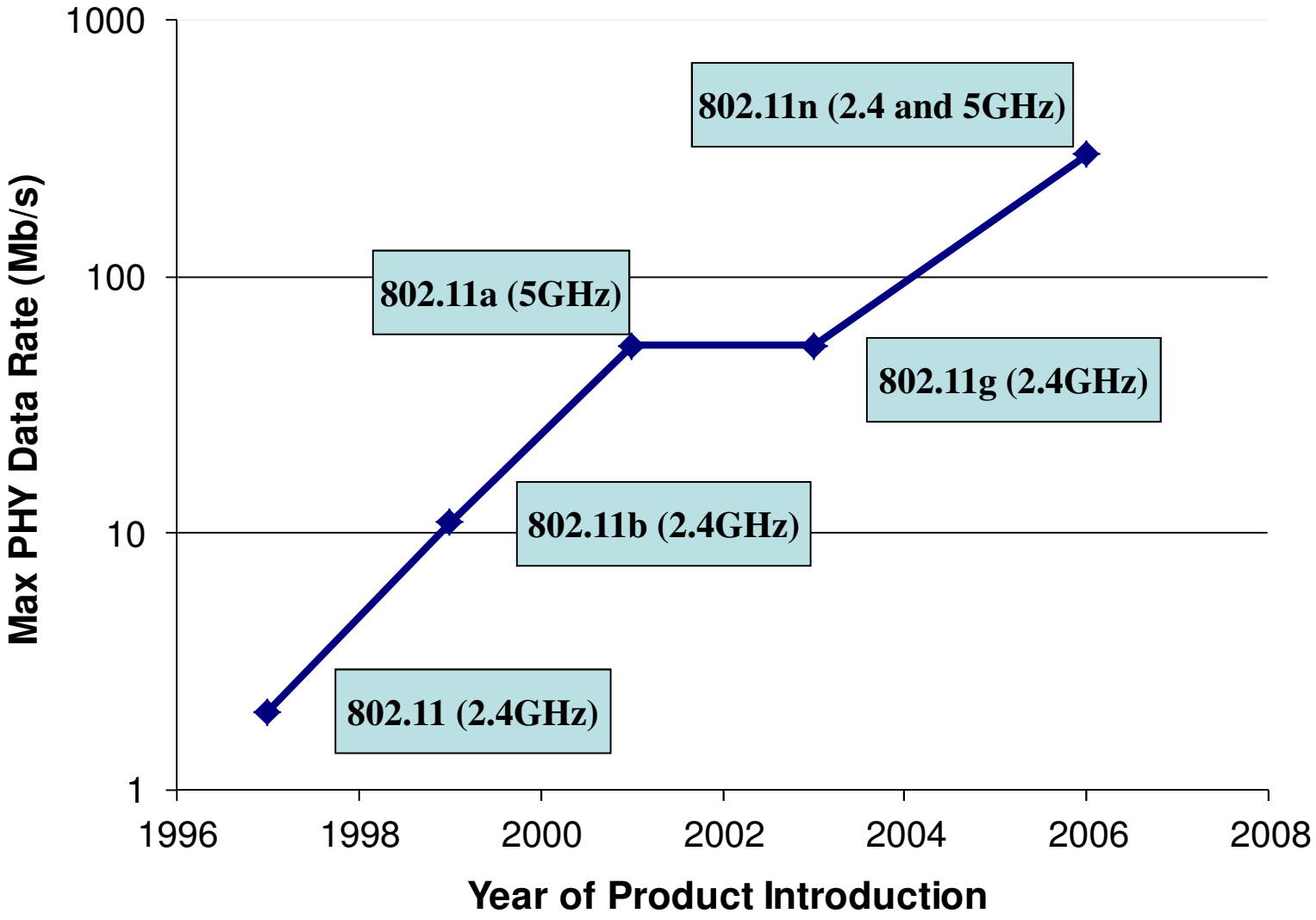
- Increased functionality
- Smaller Size / Form Factor
- Lower Power
  - On-chip interface
- Lower Cost
  - Single package
  - Ease of manufacture
    - Minimum RF board tuning
    - Reduced component count
      → Improved reliability

Cost of WLAN Throughput

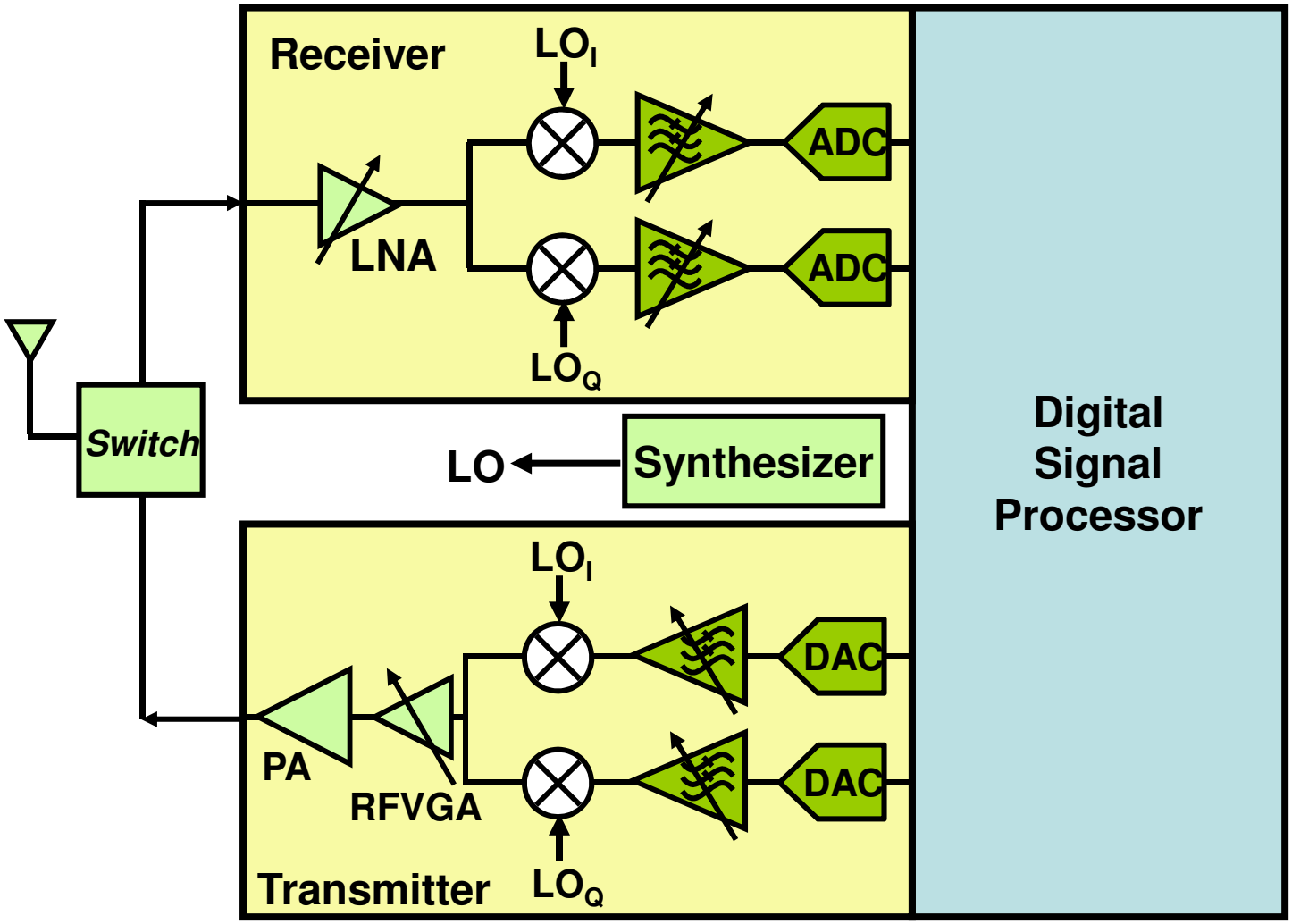


Zargari, 2007 VLSI Symposium Short Course

Evolution of 802.11 WLAN PHY Rates



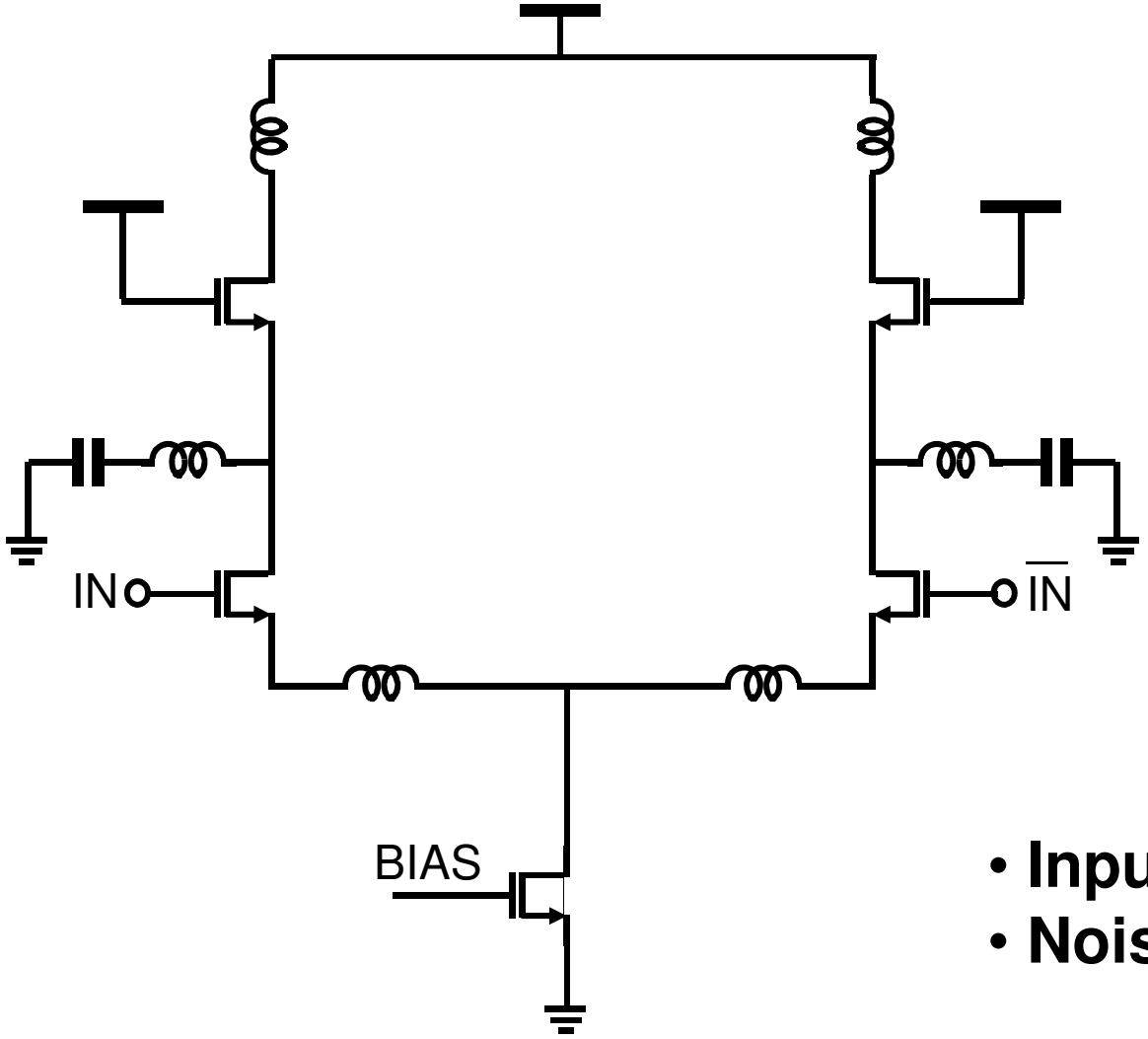
Wireless SoC Block Diagram



Low Noise Amplifier

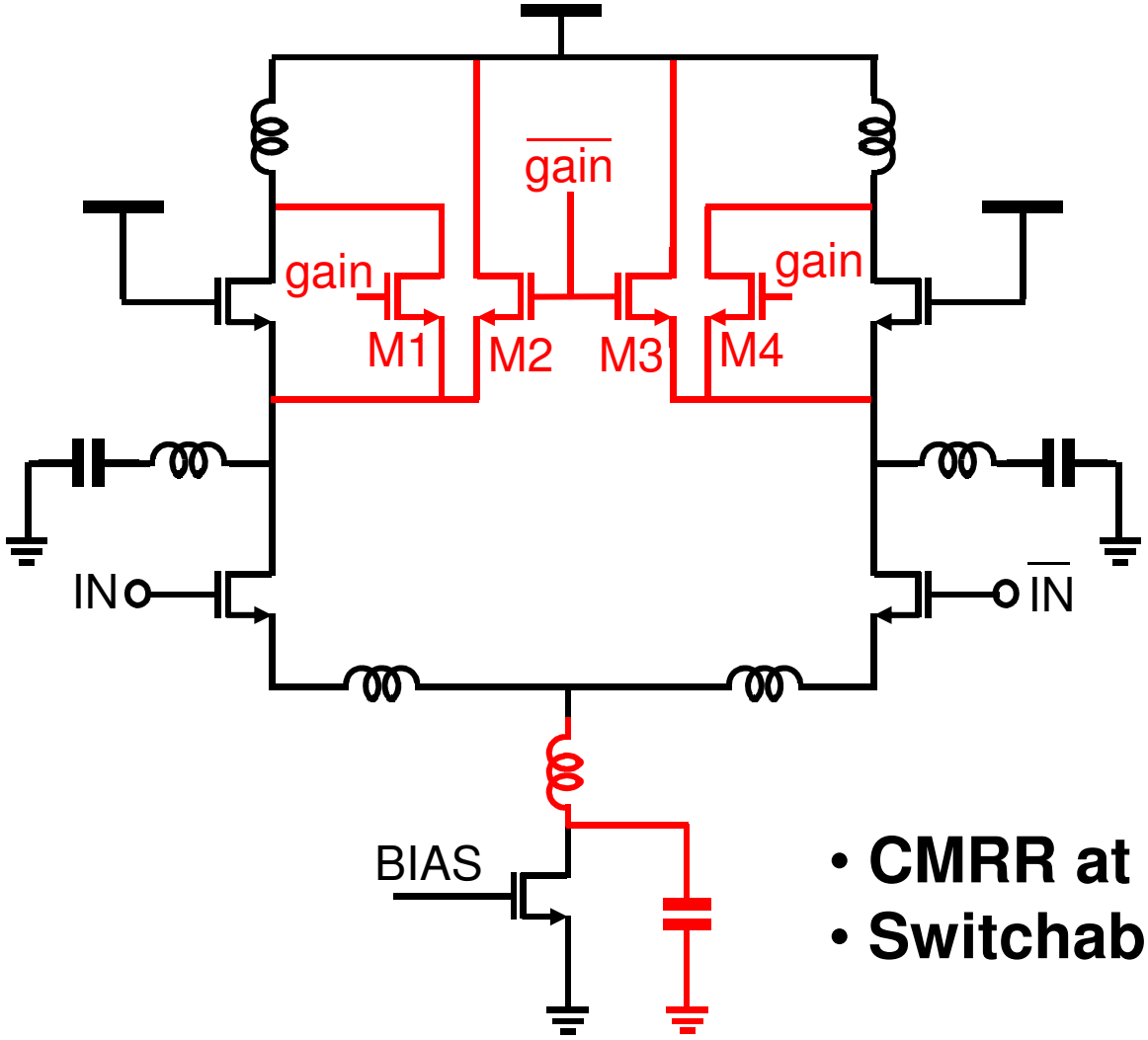
- **Low Noise Figure**
  - **Sufficient gain**
- **Able to accommodate large blockers**
  - **Large Dynamic Range**
  - **Large Common-mode Rejection**
  - **High Linearity**

LNA with Cascoded Diff Pair



- **Input match**
- **Noise Figure**

LNA with Switchable Gain



- **CMRR at RF**
- **Switchable gain for high DR**

Zargari et al, JSSC Dec 2004 (Atheros)

Power Amplifier

General Specifications

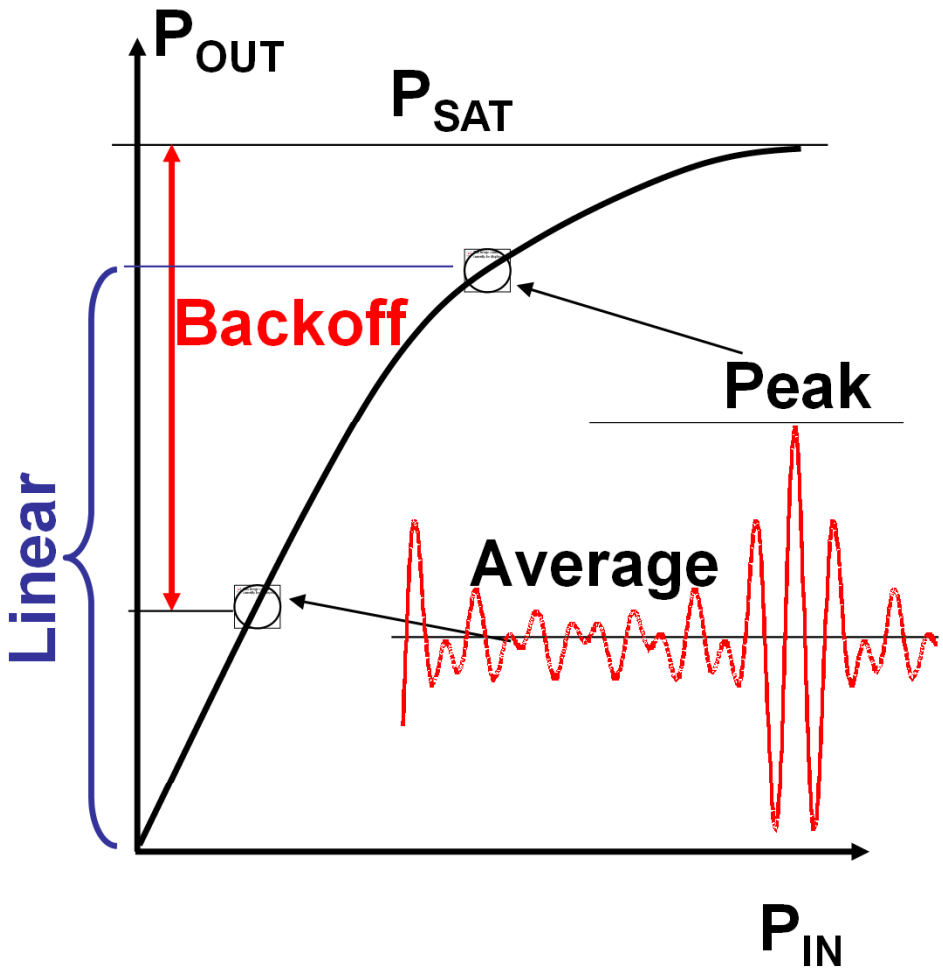
- Output power: Saturated power, P1dB
- Efficiency
- Linearity: OIP3/IM3, Harmonics
- Stability/Robustness: VSWR

Digital Communications

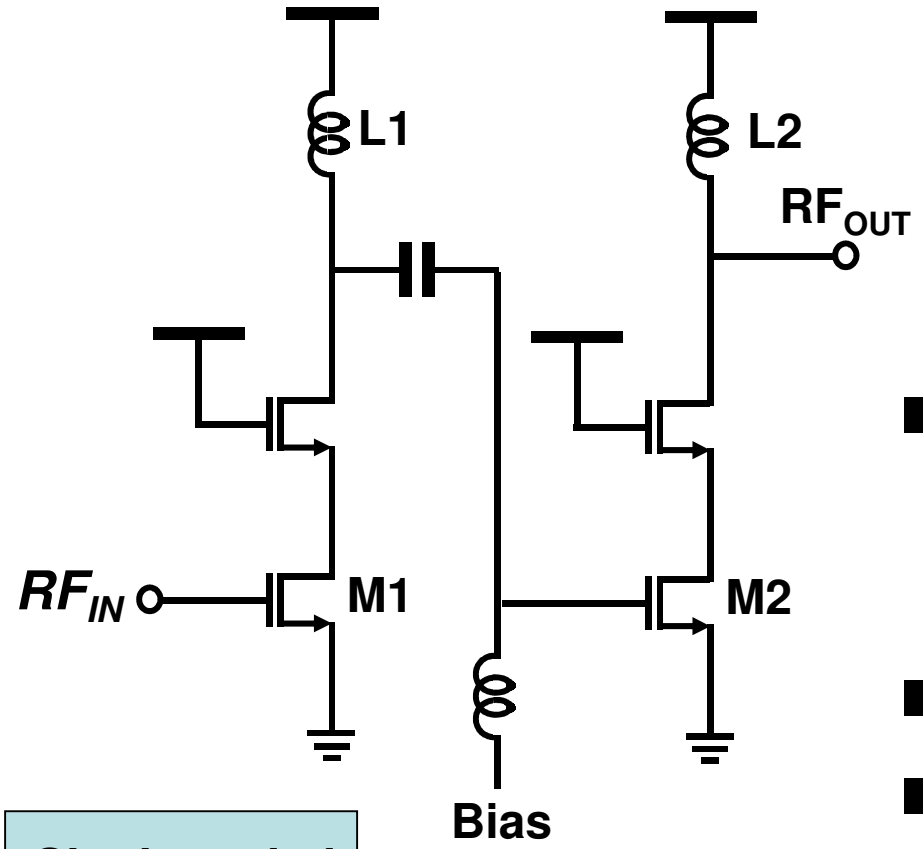
- Large Peak to Average Ratio → linearity
  - Transmit Spectral Mask – modest linearity
  - Error Vector Magnitude (EVM) – high linearity

Peak to Average Ratio

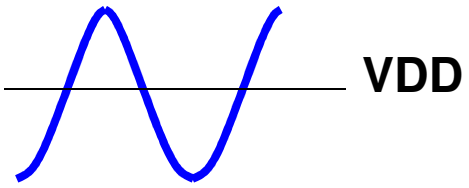
- Information encoded in both amplitude and phase
- Spectral efficient but power inefficient because average output power is much less than maximum output power



Cascoded Power Amplifier



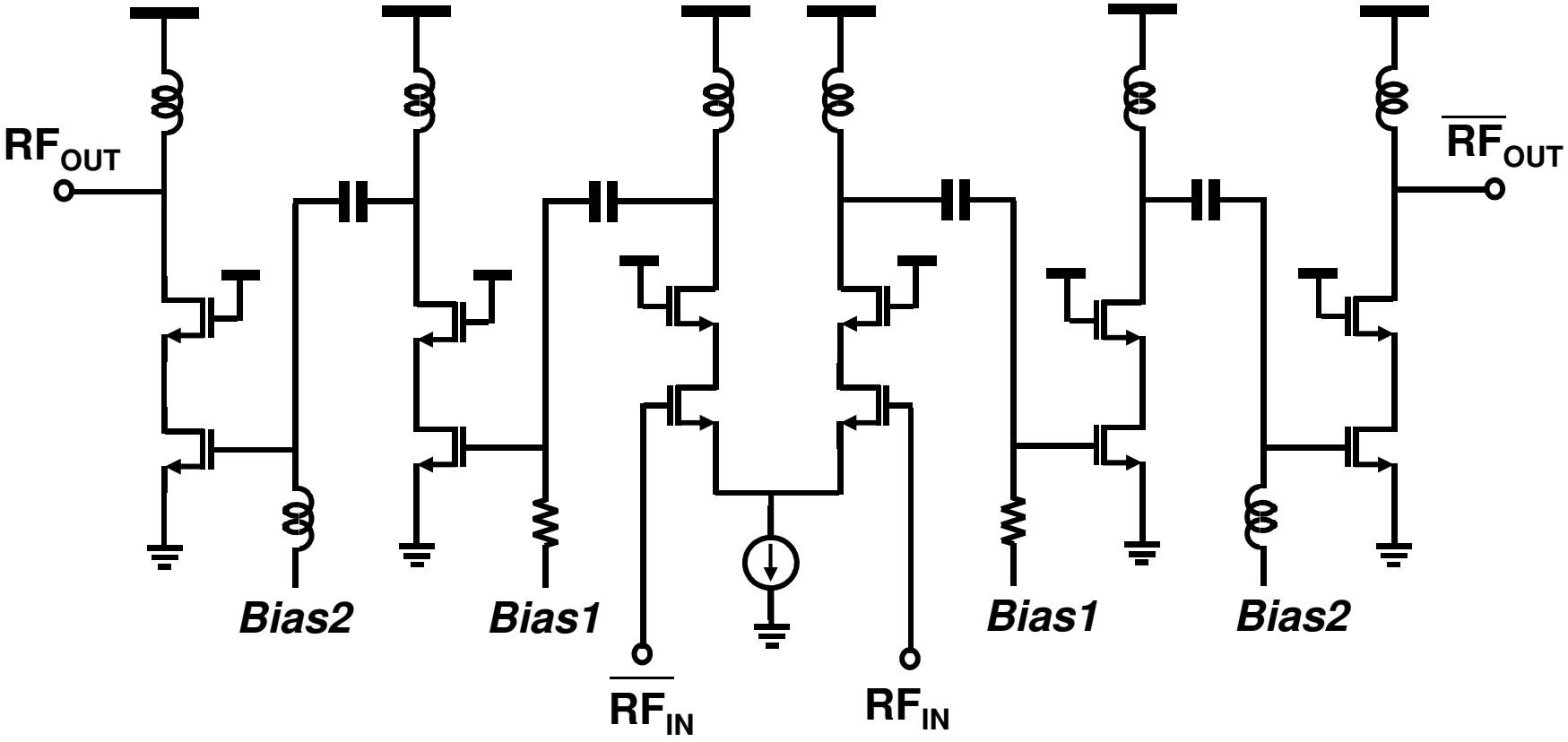
Single-ended equivalent



- Cascoding advantages
  - 3.3V supply voltage
  - Stability
- Capacitive Level-shift
- Differential
  - Off-chip balun

Su et al, ISSCC 2002 (Atheros)

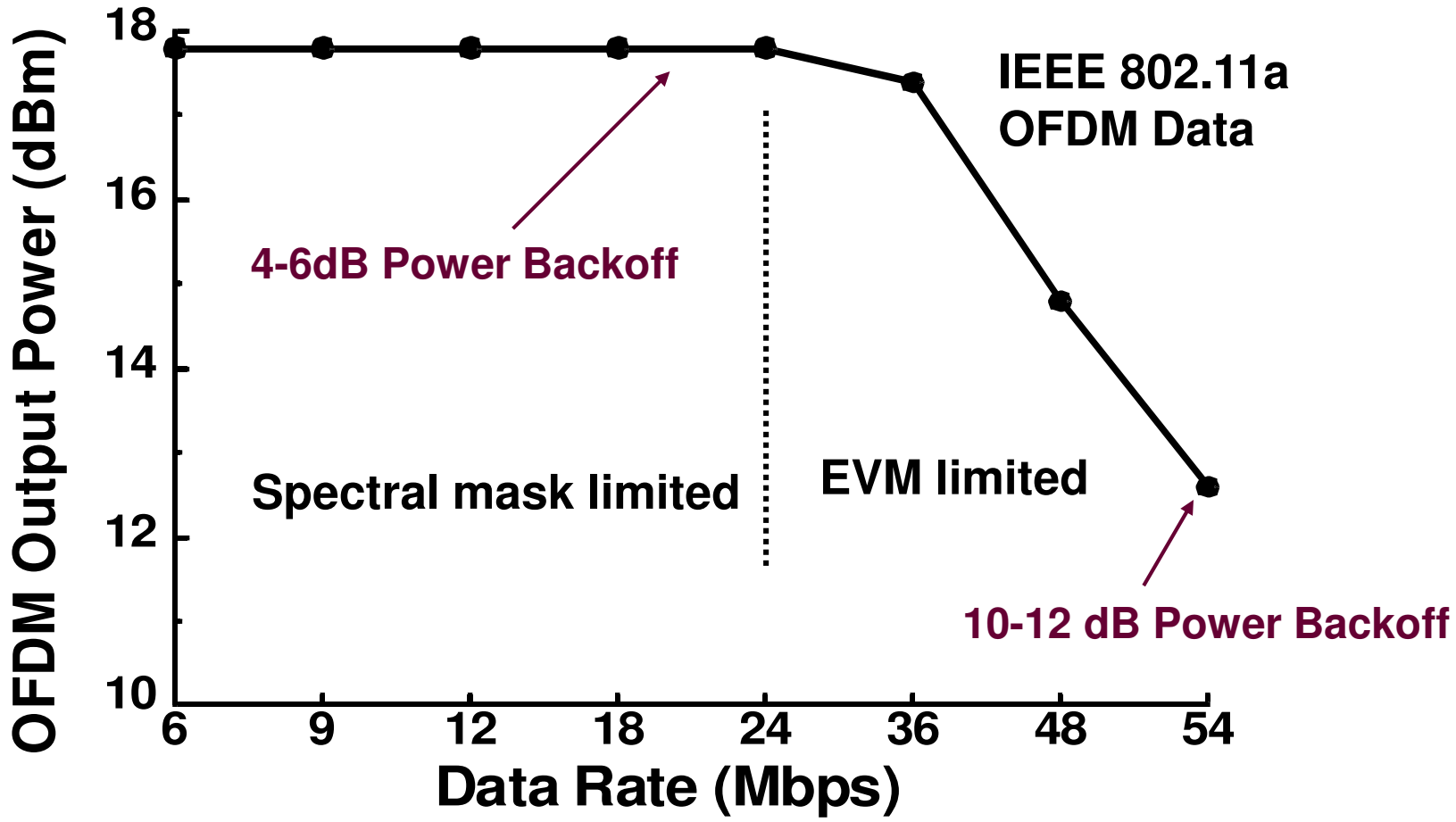
Cascoded Power Amplifiers



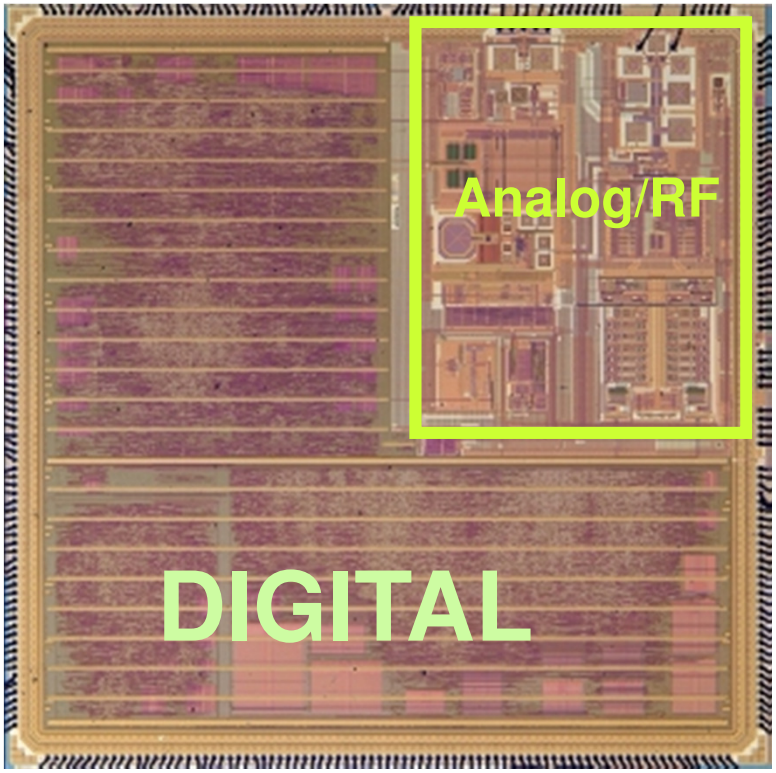
P_{MAX} = 22 dBm **P_{OFDM} = 17.8 dBm (BPSK)**

Zargari et al, JSSC Dec 2002 (Atheros)

Measured Power vs Data Rate

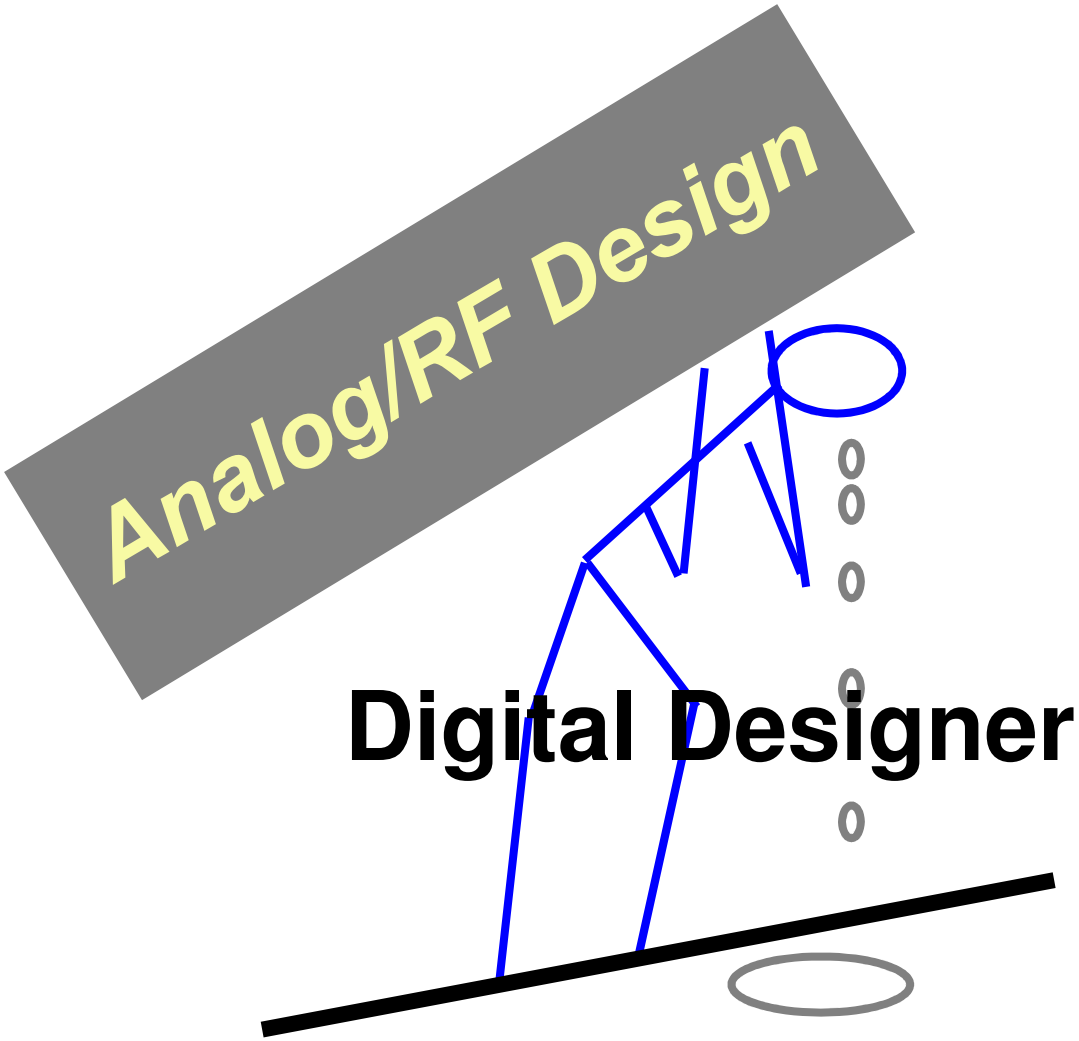


System-on-a-Chip Integration



- ✓ **Digital Assistance: Calibration Techniques**
- **Digital Interference: Noise Coupling**

Digital Assisted Analog/RF Design



Digital Assisted Analog/RF Design

- **Using digital logic to compensate/correct for imperfections of analog and RF circuits to enable:**
  - **Lower power,**
  - **smaller area,**
  - **improved reliability of analog/RF**

  ➔ resulting in lower cost and improved performance

Digital Assistance: Calibration Issues

- **Desired properties of calibration:**
  - **Independent of temperature, aging, frequency**
  - **Inexpensive (in time, area and power) to implement**
  - **Do not interfere with system performance**

- **Wireless System-on-a-Chip advantage:**
  - **Calibration building blocks already exist on-chip: transmitter and receiver, data converters, and CPU**
  - **No package pin limitation**

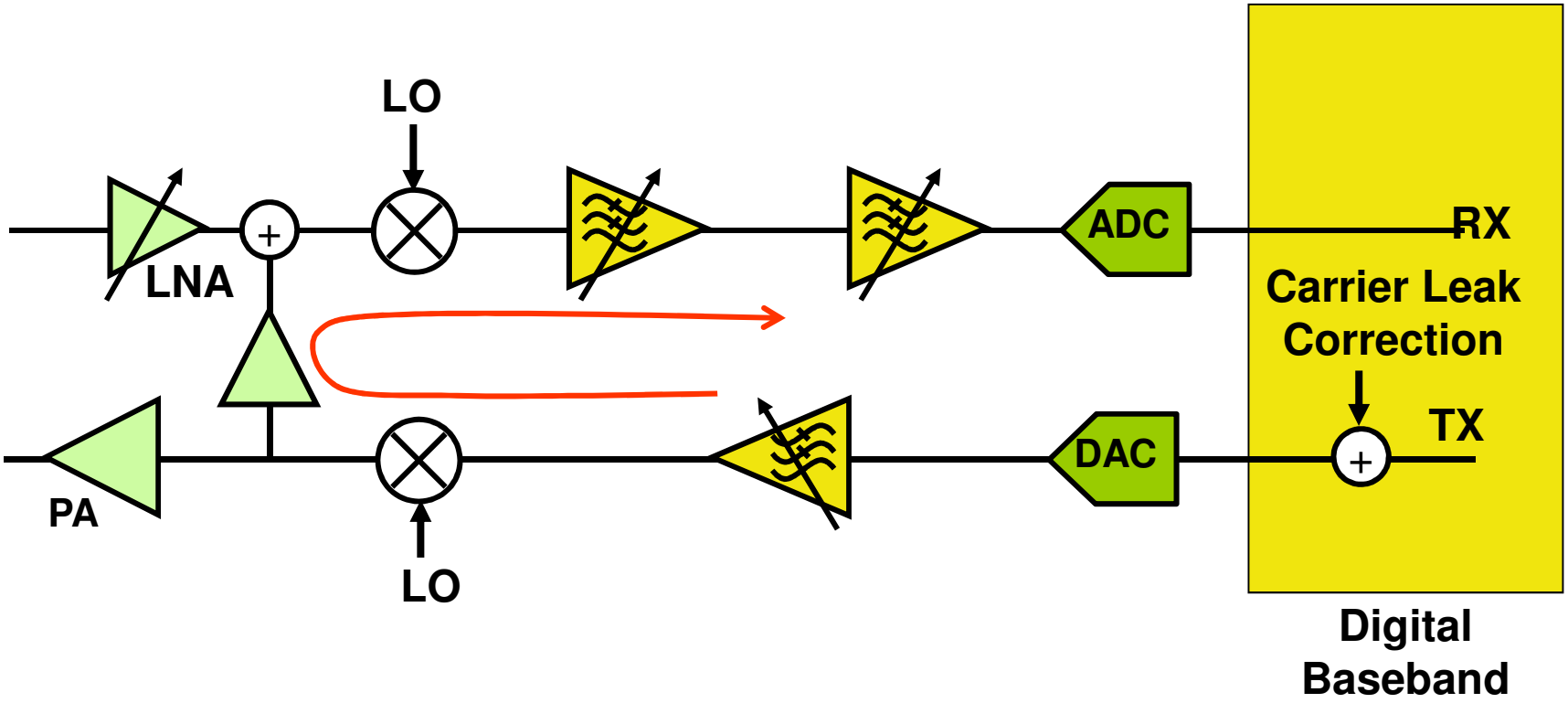
Calibration Techniques

- **Test Signal**
  - **Dedicated test signals from DAC: Tx carrier leak**
  - **RF loop back: Receive filter bandwidth**
  - **Thermal noise: Rx Gain**
  - **Live Rx (signal) traffic: Rx I/Q mismatch**

- **Observation Signal**
  - **Dedicated ADC**
  - **Implicit ADC: Comparator**

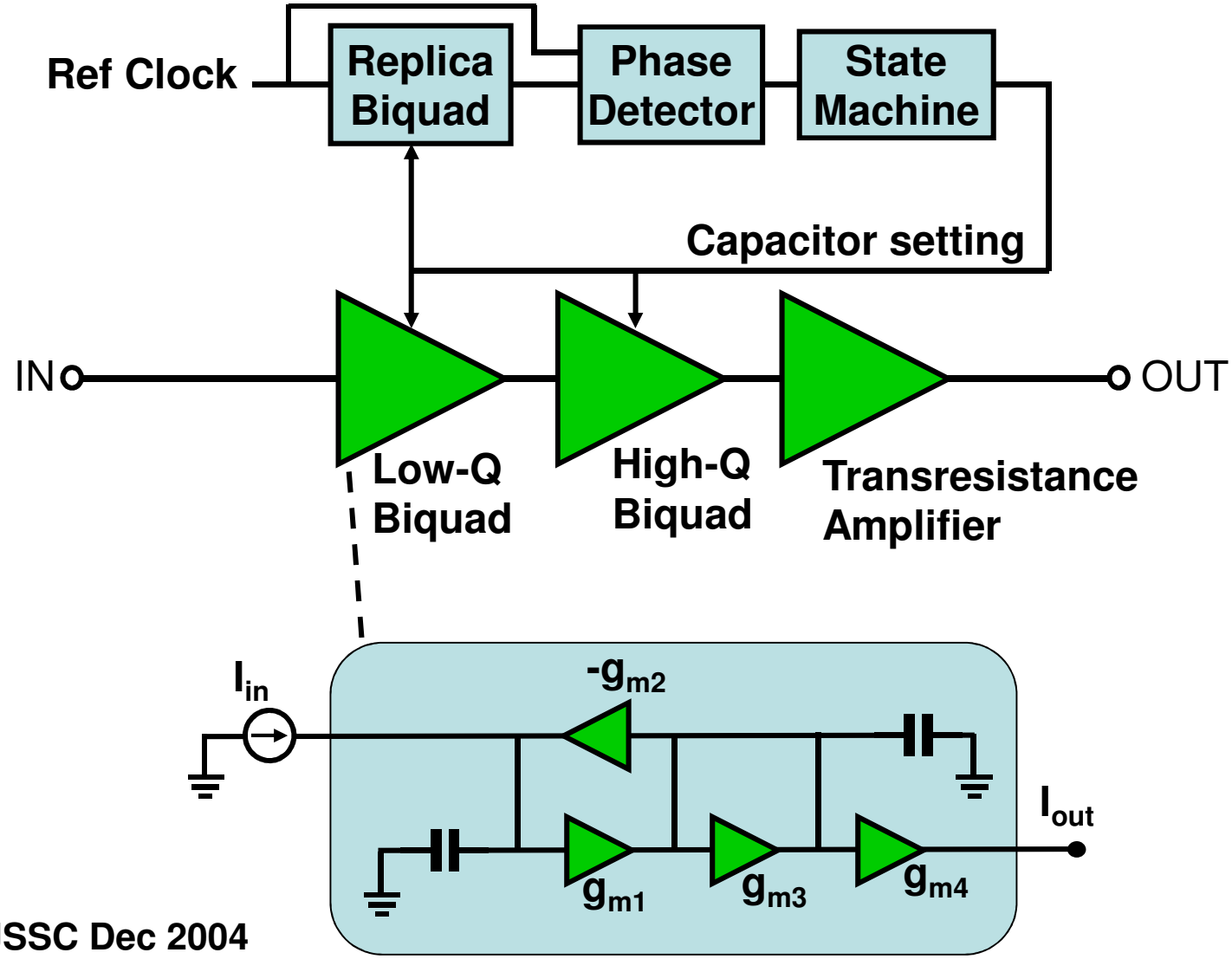
- **Tuning Mechanism**
  - **Dedicated DAC**
  - **Implicit DAC:**
    Selectable capacitors, resistors, transistors
  - **Digital tuning (if signal is already digital)**

RF loop back: Tx Carrier Leak



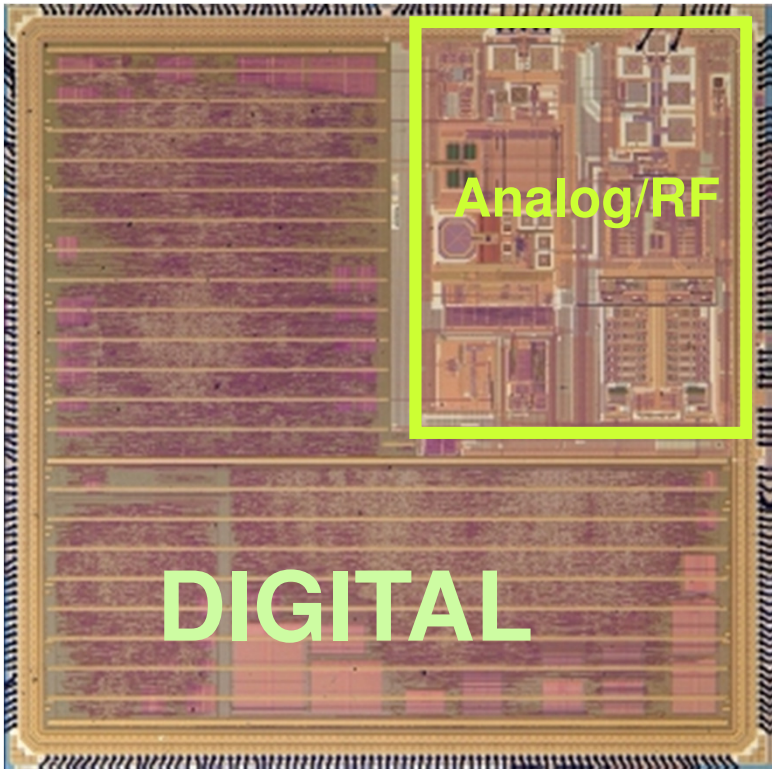
- Test signal: Tx DAC
- Observation signal: RF loop back to Rx ADC
- Tuning: Carrier Leak Correction at Tx DAC input

Calibrating Low-pass gm-C Filter



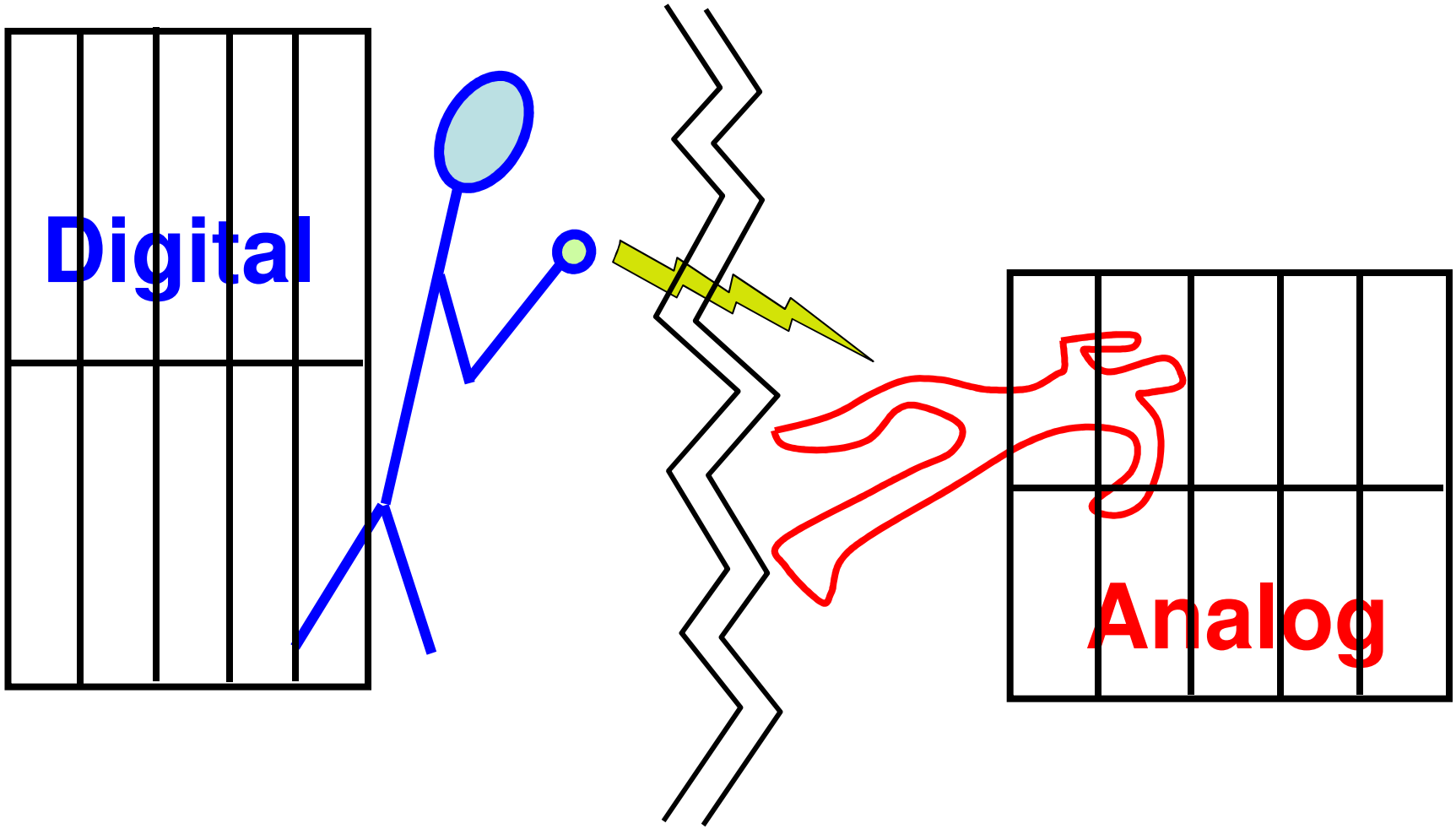
Zargari et al, JSSC Dec 2004

System-on-a-Chip Integration

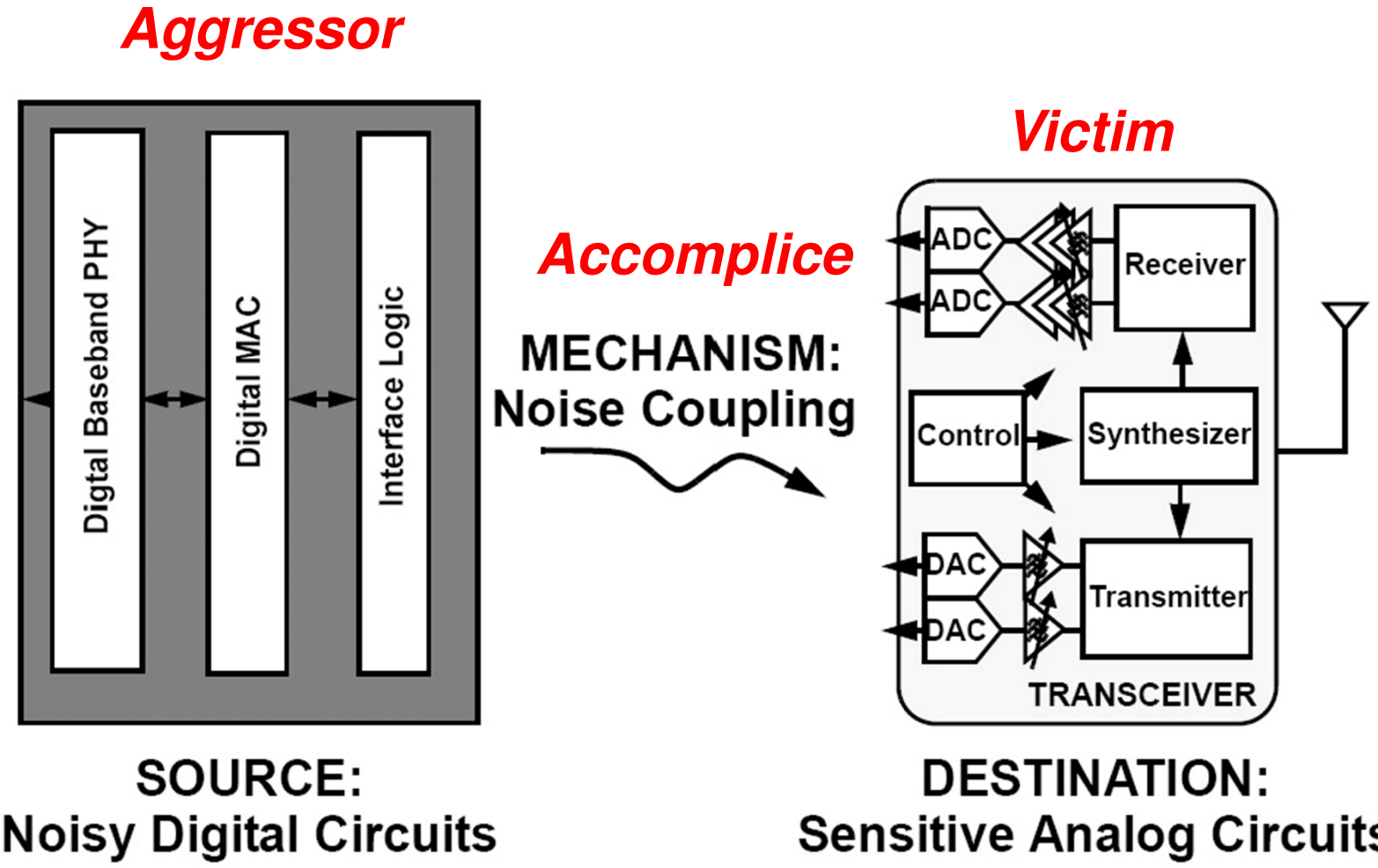


- **Digital Assistance: Calibration Techniques**
- ✓ **Digital Interference: Noise Coupling**

Digital Interference



Digital Interference: Noise Coupling



Noise Source

Pacify the aggressor

- **Reduce noise by turning off unused digital**
  - **Clock gating**
  - **Avoid oversized digital buffers**
- **Stagger digital switching**
  - **Avoid large number of digital pads switching simultaneously**
  - **Avoid switching digital logic at the same sampling instance of sensitive analog**

Noise Destination

Strengthen the victim

- **Increase immunity of sensitive analog and RF circuits**
  - **Common-mode noise rejection**
    → Fully differential topology
  - **Power Supply noise rejection**
    → Good PSRR
    → Dedicated on-chip voltage regulators

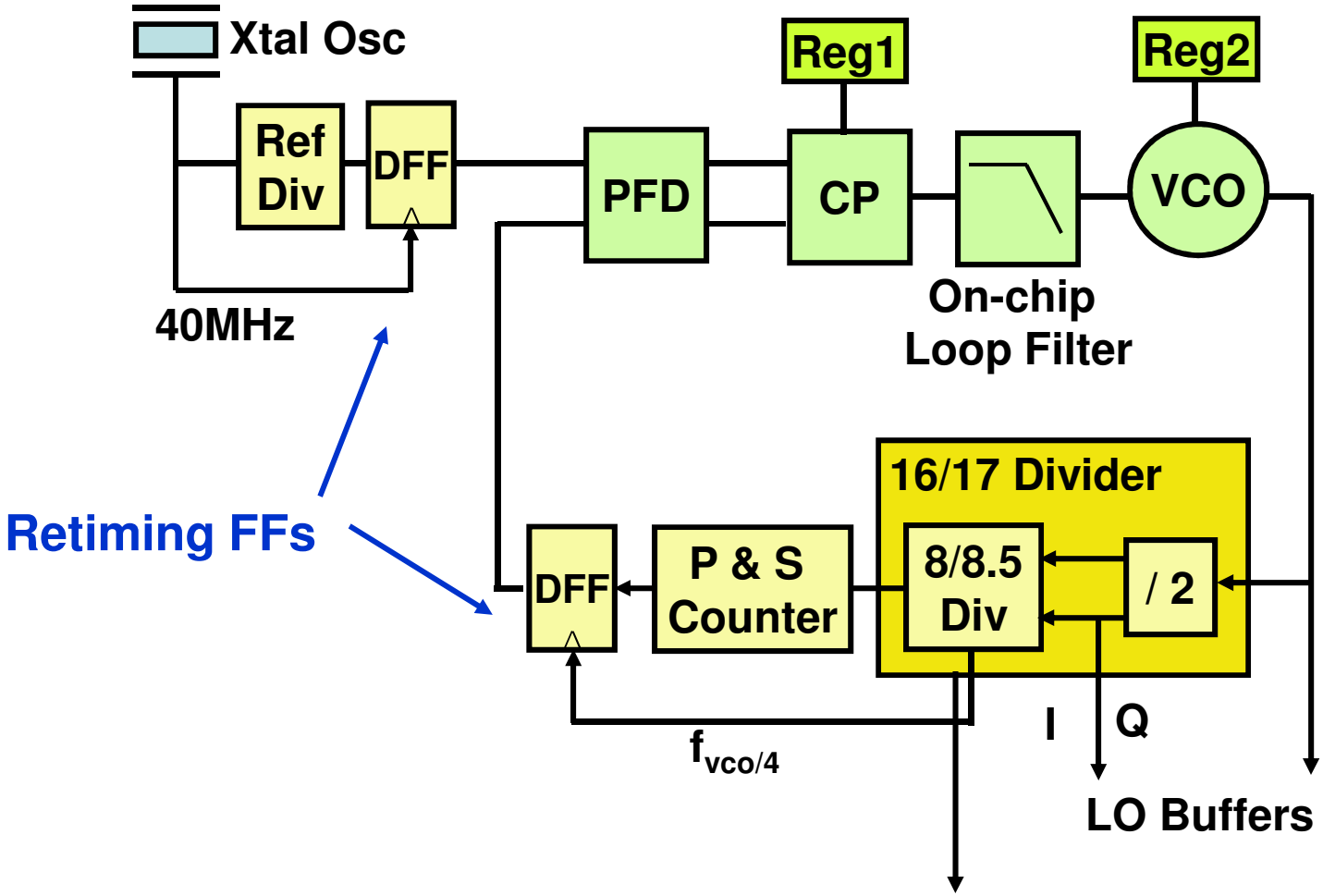
- **Avoid package coupling by keeping sensitive nodes on chip**
  (Example: VCO control voltage)

Coupling Mechanism

Deter the accomplice

- **Power Supply noise coupling**
  - **Separate or star-connected power supplies**
- **Capacitive or inductive coupling to sensitive signals and bias voltages**
  - **Careful routing of signal traces to reduce parasitic capacitive/inductive coupling**
  - **Use ground return-path shields**
- **Substrate coupling induced V_{TH} modulation**
  - **Low-impedance substrate connection**
  - **Guard rings**
  - **Physical separation**
  - **Deep Nwell**

Frequency Synthesizer



Terrovitis et al, ISSCC 2004 (Atheros)

A 1x1 802.11n WLAN SoC with fully integrated RF Front-end Utilizing PA Linearization

Manolis Terrovitis, Michael Mack, Justin Hwang, Brian Kaczynski, Gabriel Tseng*, Bor-Chin Wang*, Srenik Mehta, David Su

Atheros Communications, Santa Clara, California

***Atheros Communications, Hsinchu, Taiwan**

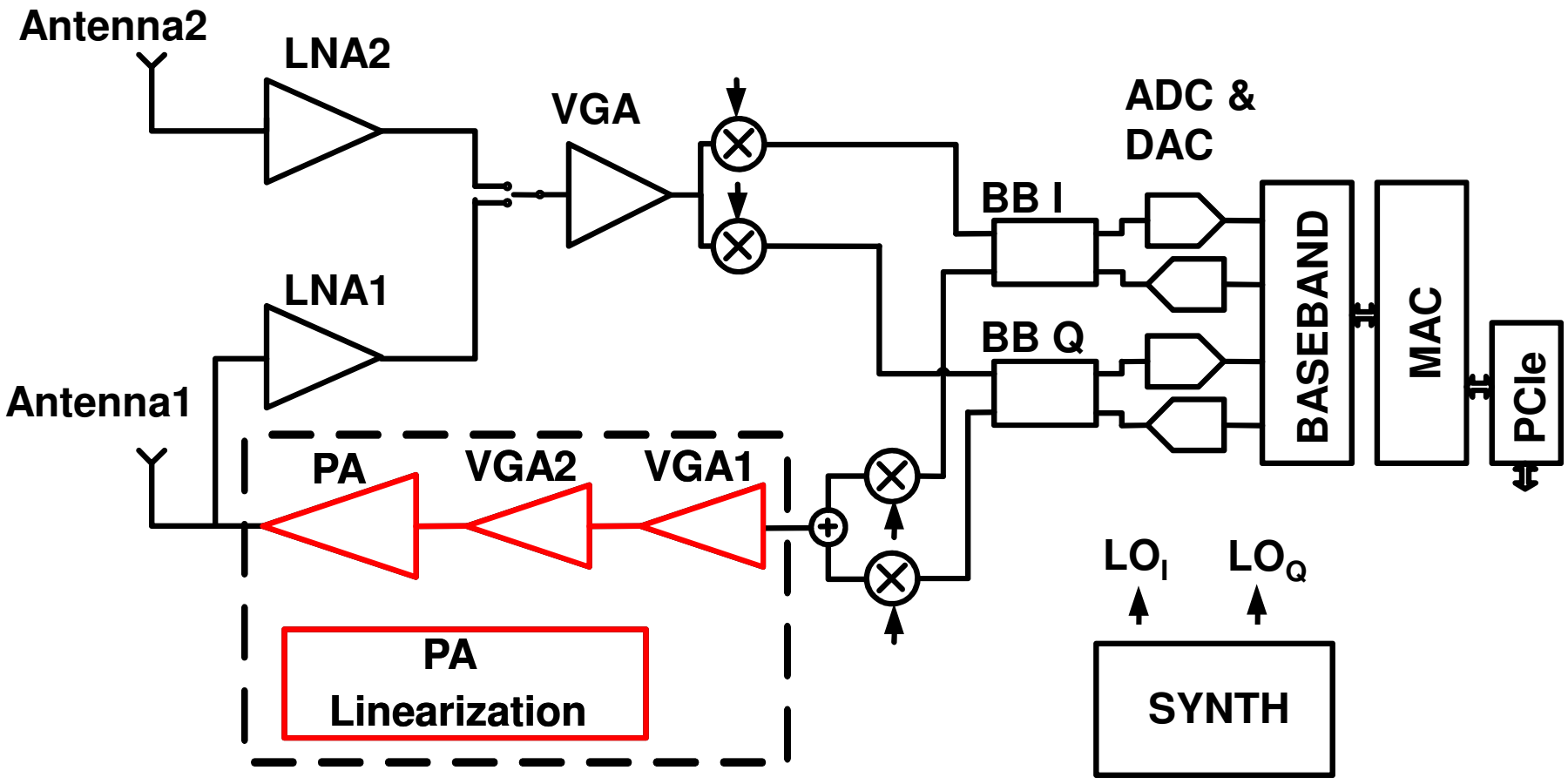
From presentation by Dr. Manolis Terrovitis at the 35th European Solid-State Circuits Conference in Athens on September 16, 2009

SoC Design Goals

- Design a low cost, small form factor, and high performance 802.11 system
- Eliminate external components (Power Amplifier, Low-Noise Amplifier, Transmit/Receive switch)
- Power Amp Linearization for maximum transmit linear output power and efficiency

Terrovitis et al, ESSCIRC 2009 (Atheros)

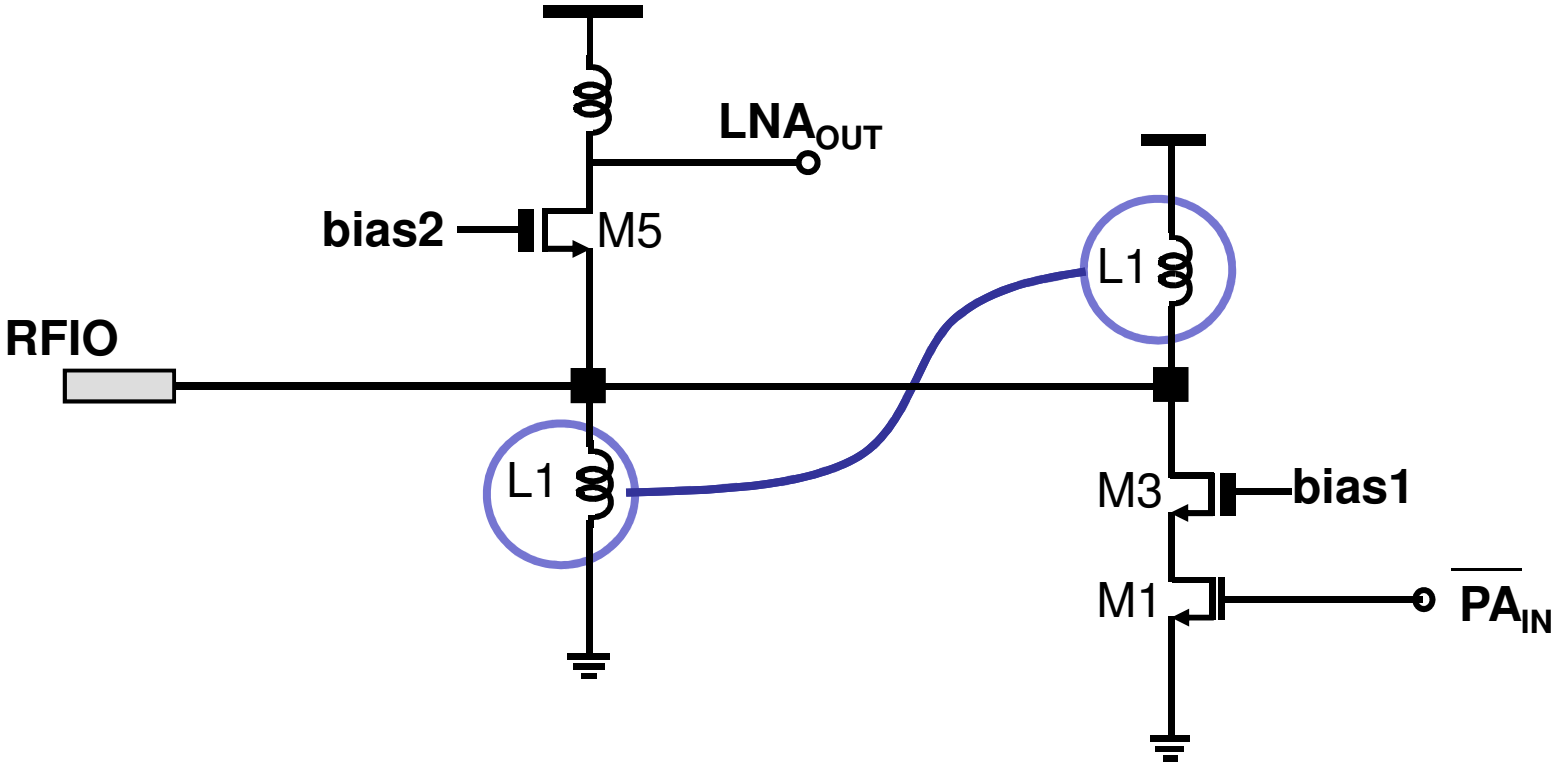
SoC Block Diagram



Ref: Zargari et al, Dec. 2008, JSSC.

Terrovitis et al, ESSCIRC 2009 (Atheros)

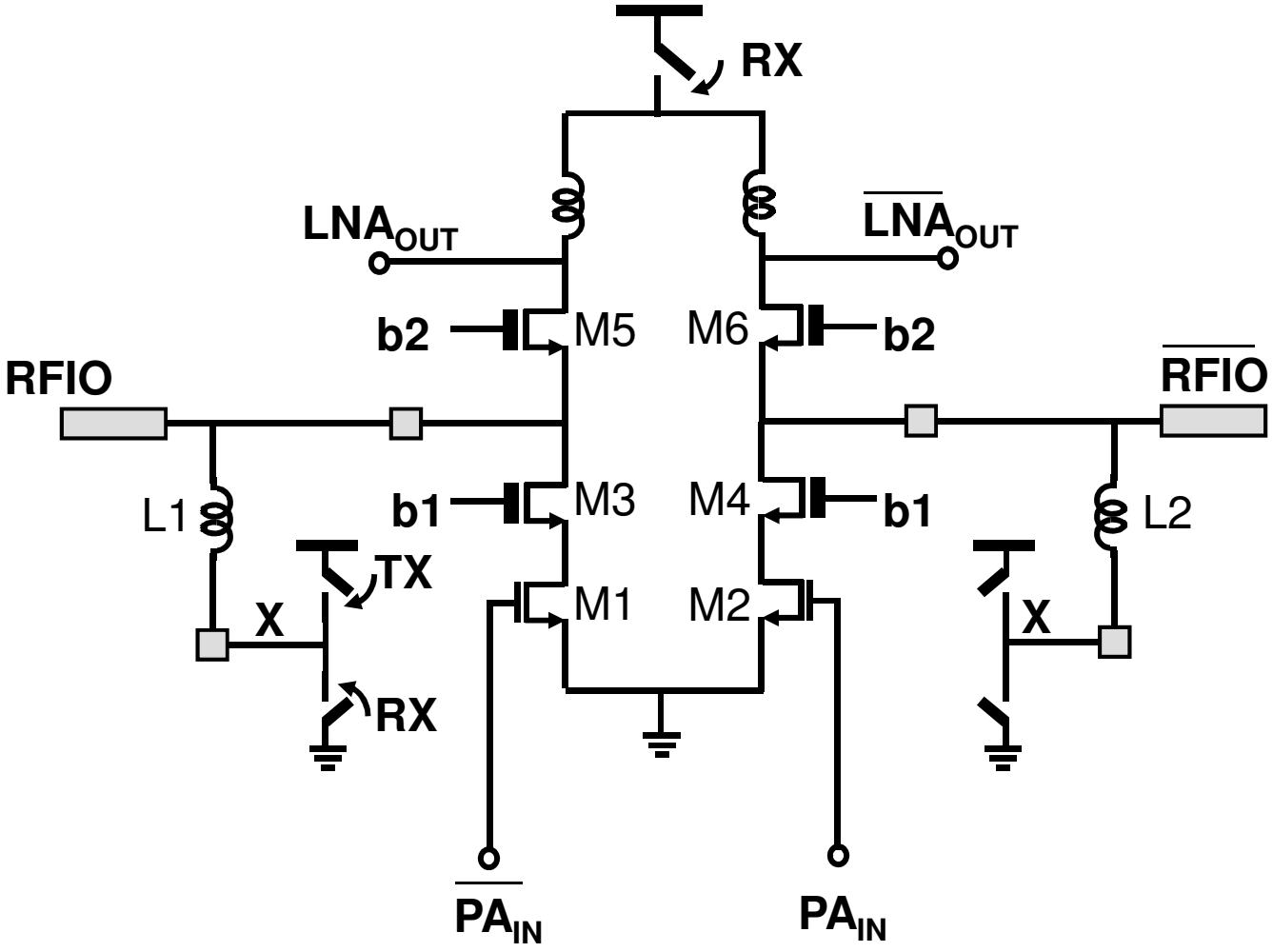
Combined RF Frontend



- PA, LNA, T/R Switch
- Large swing
- Low impedance

Terrovitis et al, ESSCIRC 2009 (Atheros)

Combined RF Frontend



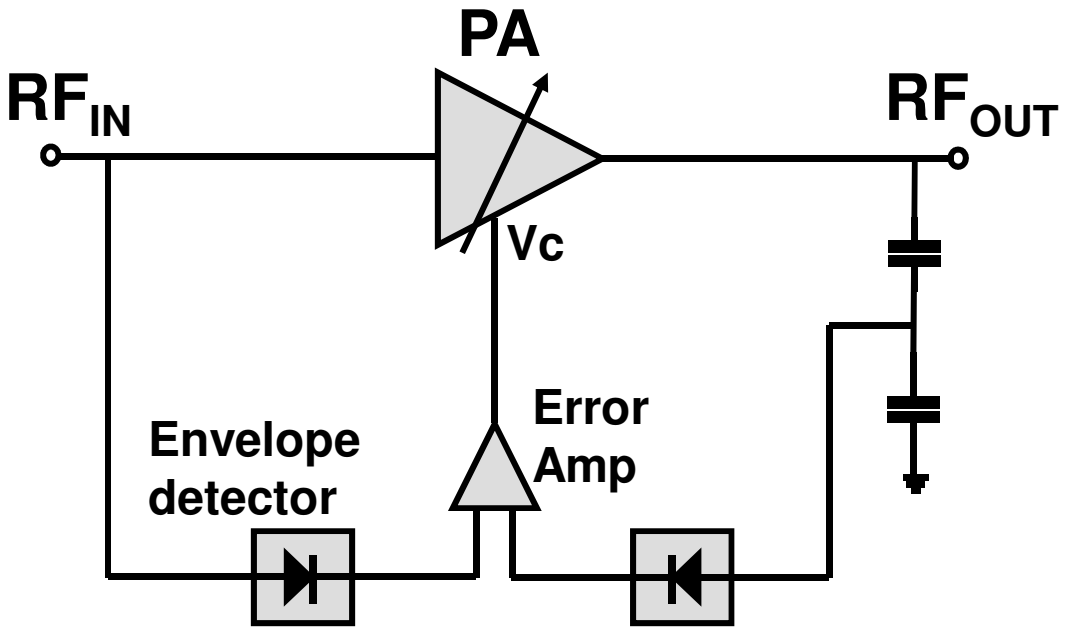
Terrovitis et al, ESSCIRC 2009 (Atheros)

Linearized RF Power Amp

Transistors are *cheap* on an System-on-a-Chip

- **Use linearization technique to improve linearity and efficiency of the Power Amplifier**

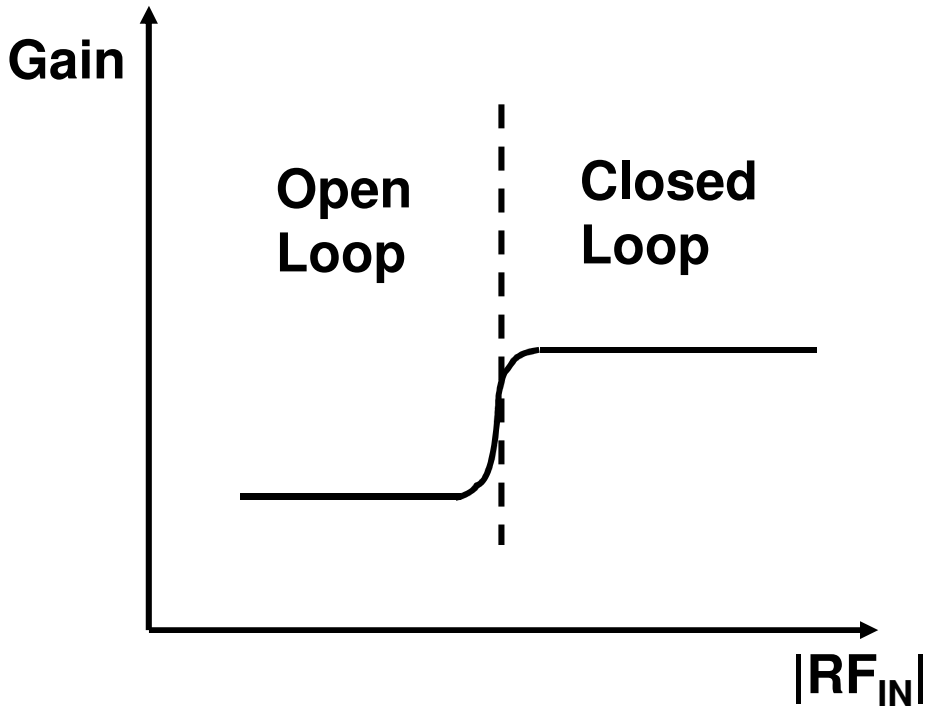
Envelope Feedback



- **Linearizes Gain**
- **Fixes Gain over process and temperature**

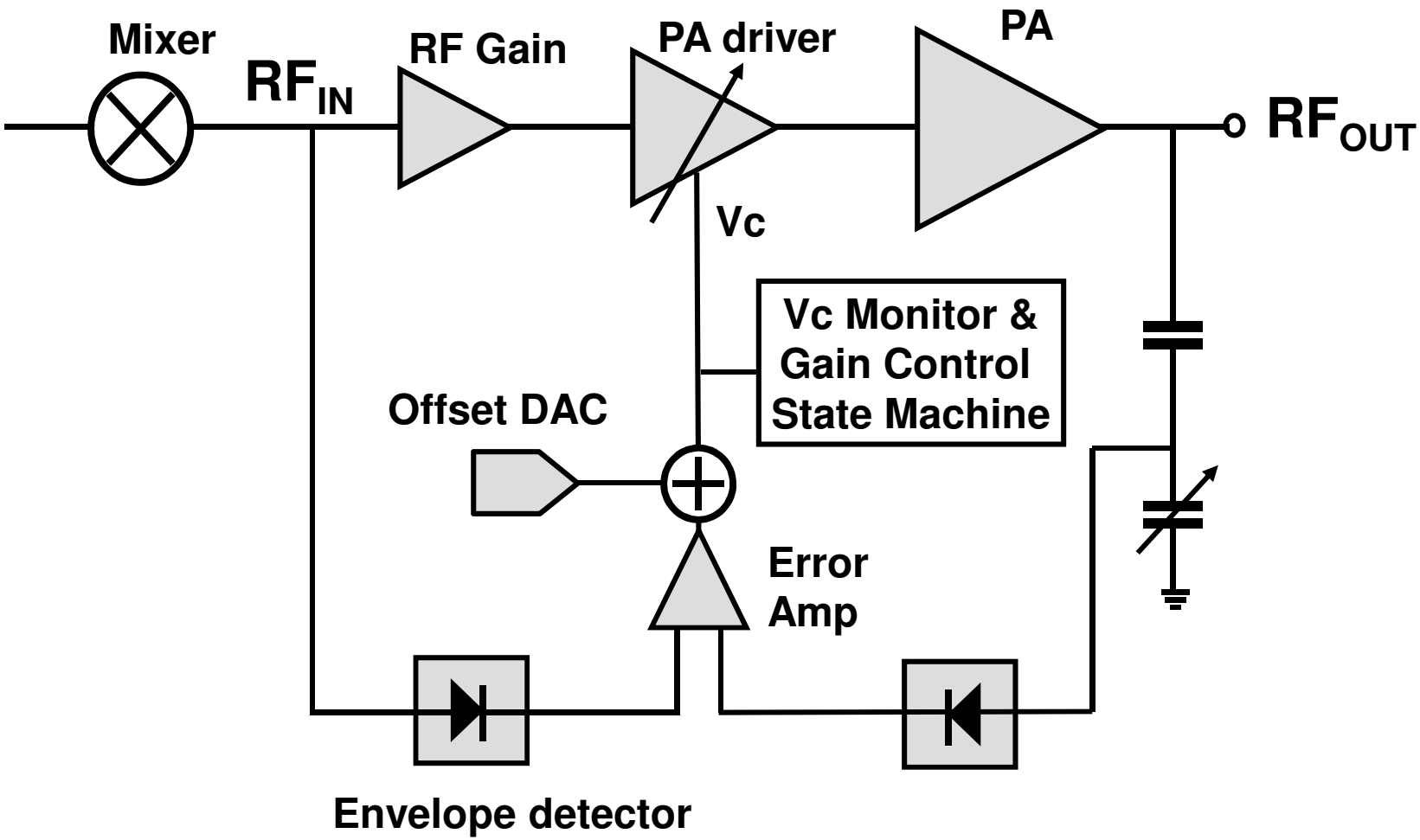
Envelope FB Linearization Issues

- Phase distortion is not corrected
- Envelope detectors do not respond for low signal
  - Loop opens at low amplitude
  - Offset Correction



Terrovitis et al, ESSCIRC 2009 (Atheros)

Implemented Feedback Loop



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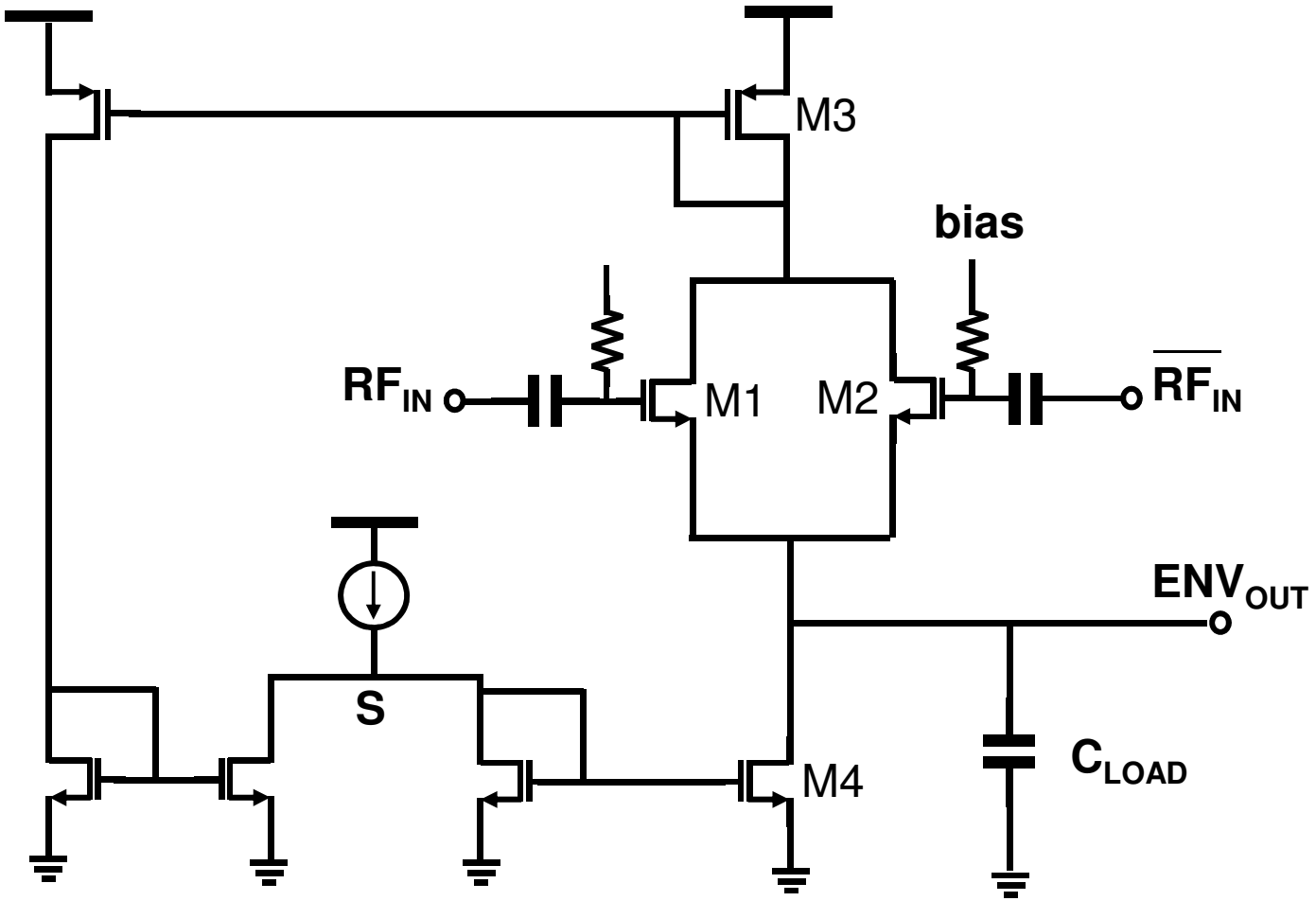
Fast Envelope Detector



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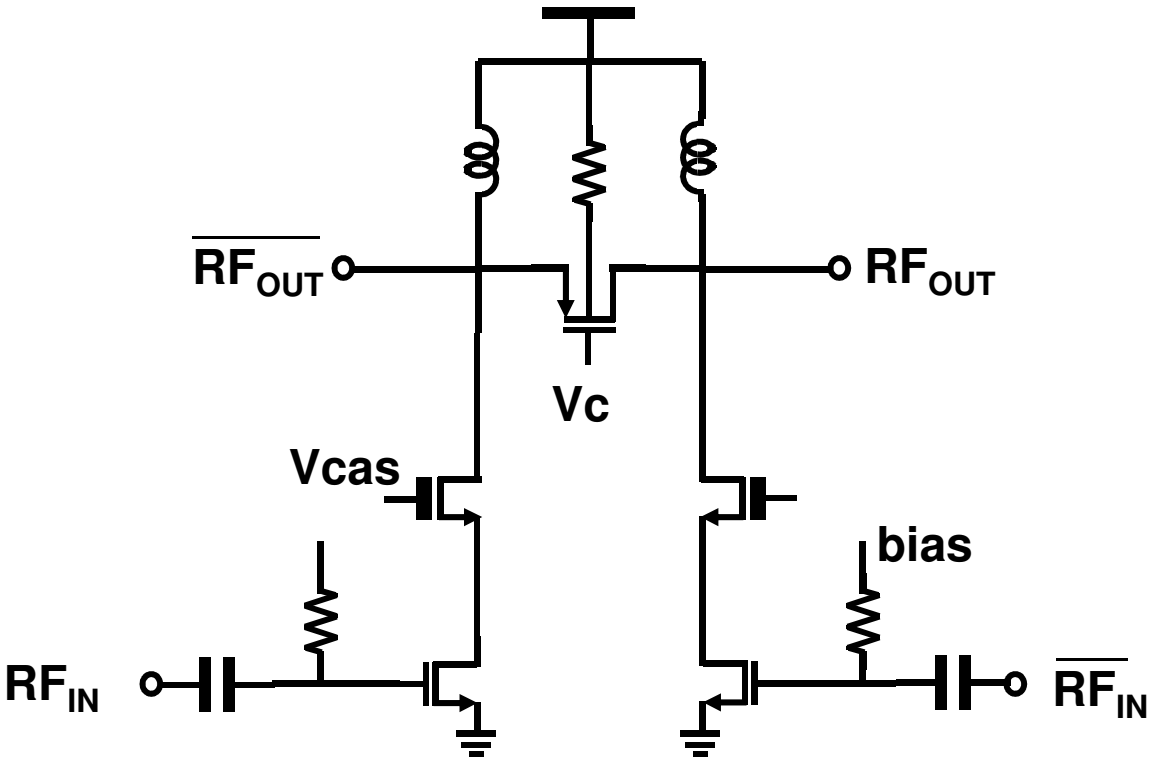
PA Driver with Variable Load

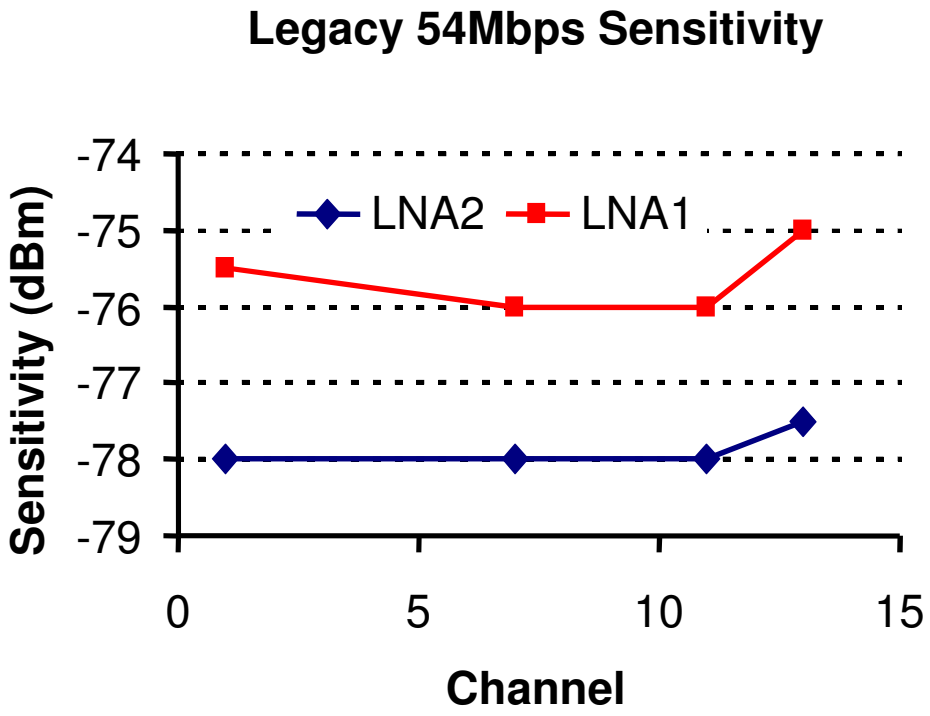


Terrovitis et al, ESSCIRC 2009 (Atheros)

Sensitivity Measurements

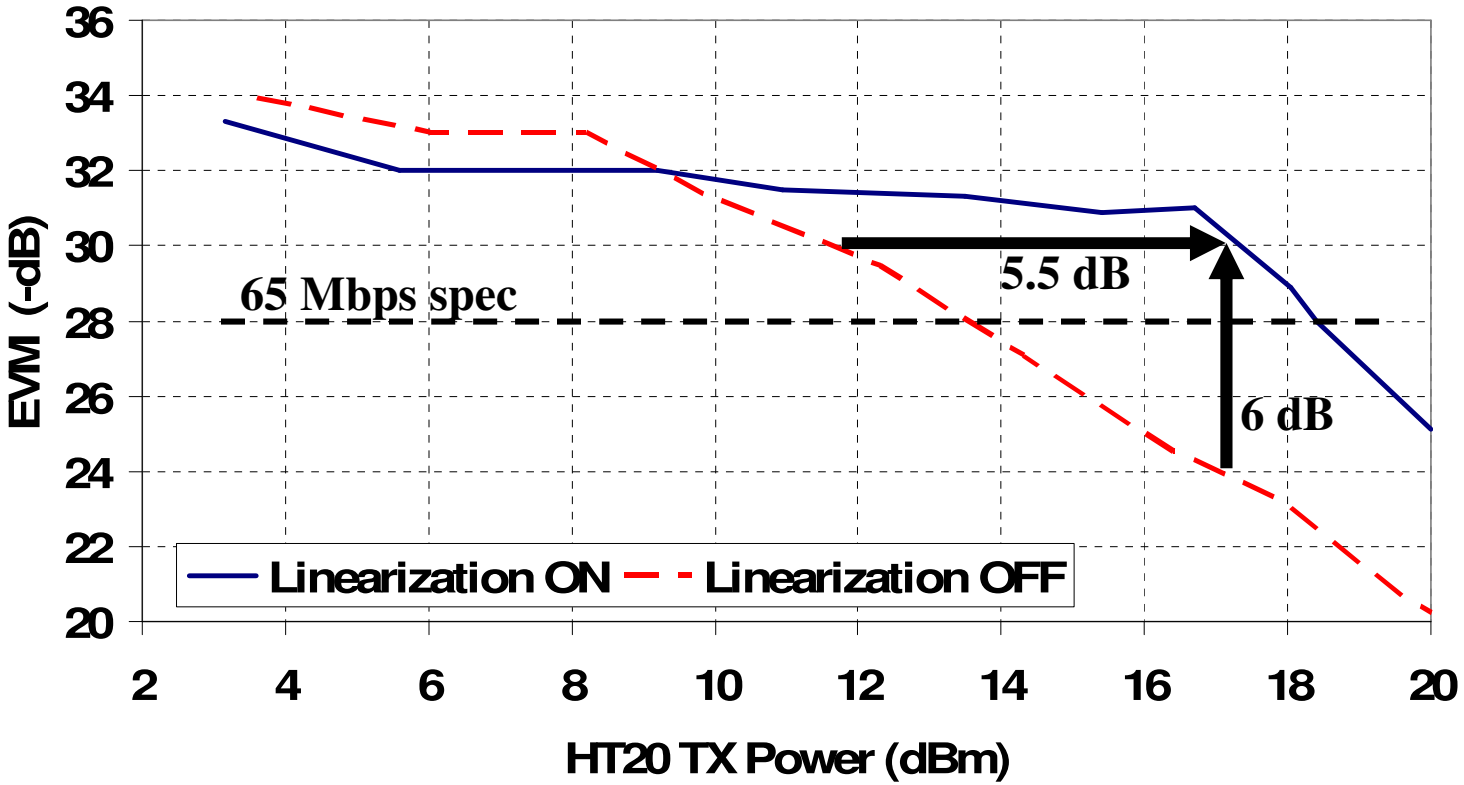
System NF (LNA1/LNA2) = 5.5dB / 3.5dB

Data Rate	Sensitivity LNA1/LNA2 (dBm)
CCK 1Mbps	-97/-99
11g 54Mbps	-76/-78
HT20 65Mbps	-73/-75
HT40 135Mbps	-69/-71.5



Terrovitis et al, ESSCIRC 2009 (Atheros)

Output Power Measurements



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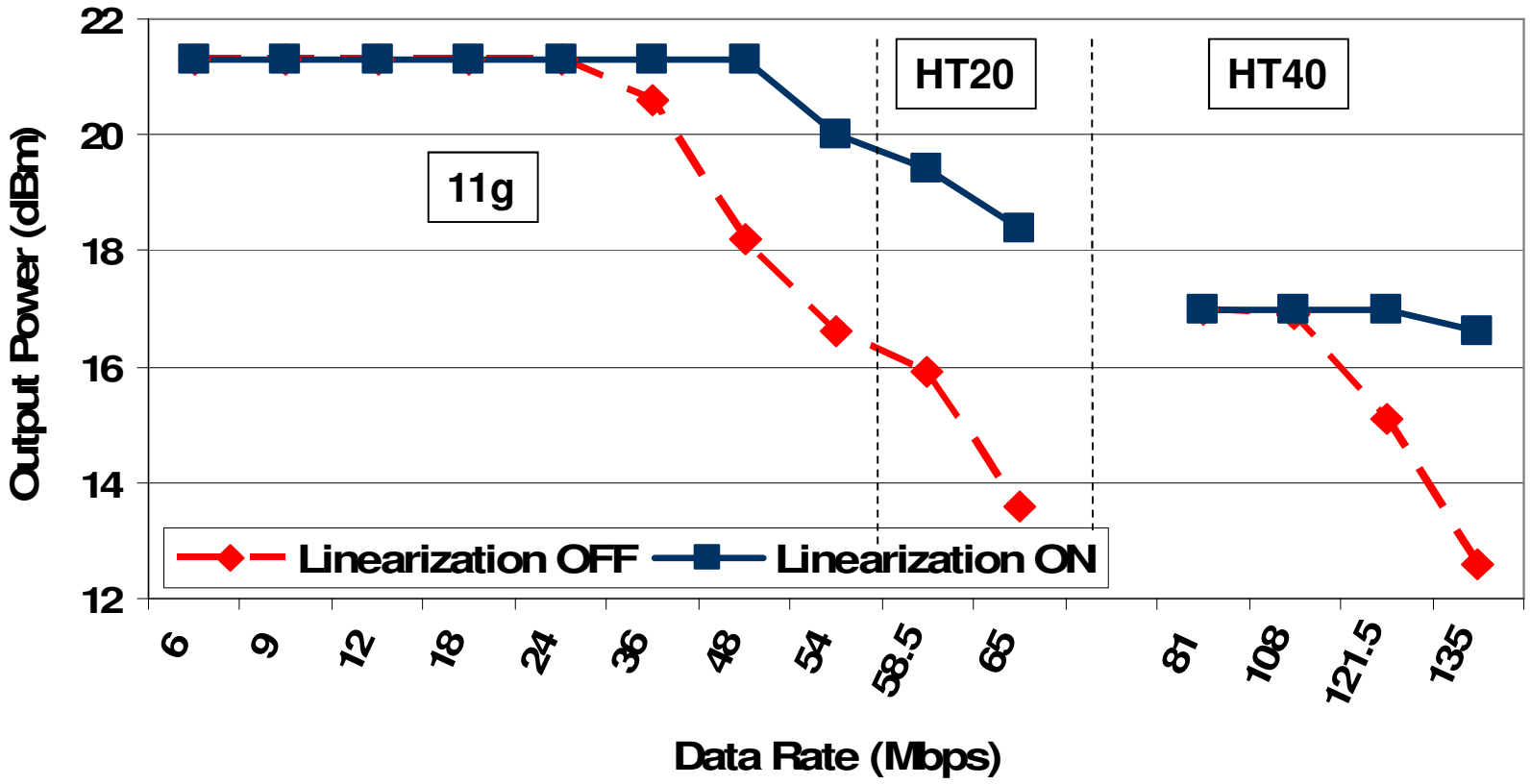
Max EVM and Mask Compliant Power vs Data Rate



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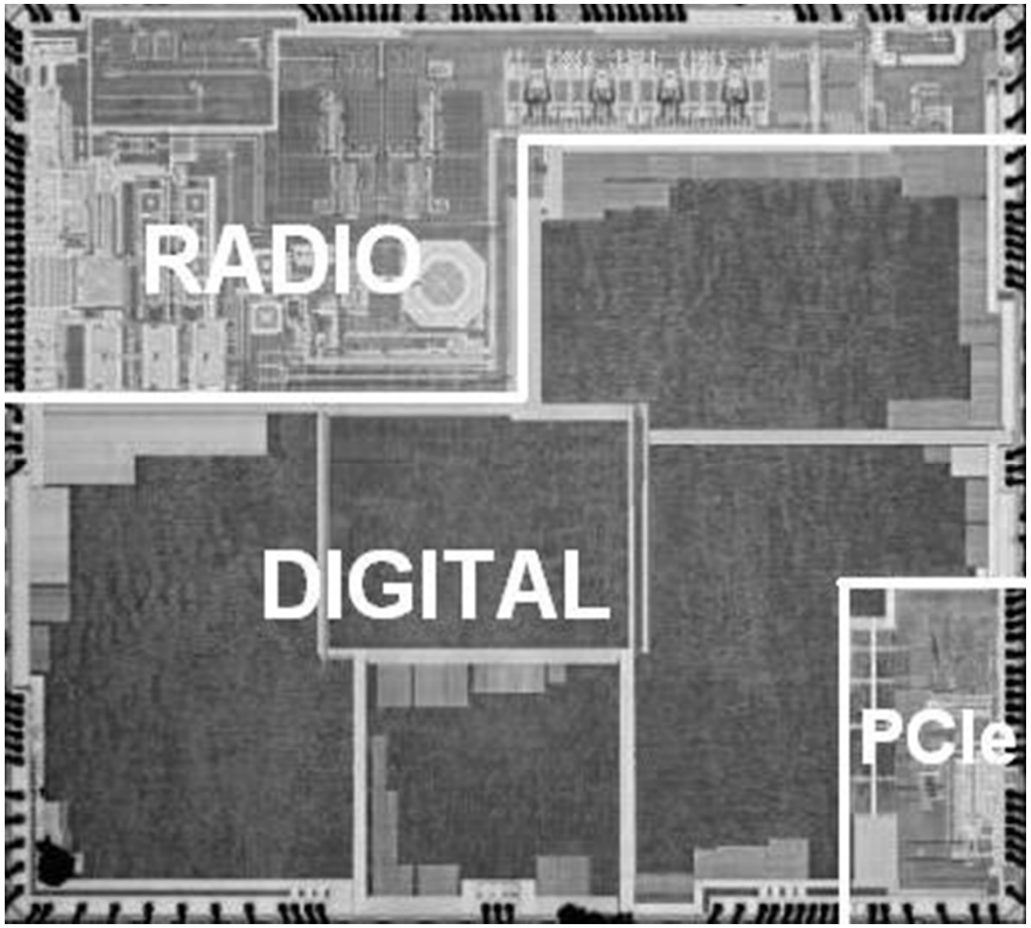
Chip Micrograph



- 0.13μm CMOS
- 68 pin QFN package
- 19mm^2 Silicon Area
- Current Consumption from 3.3V
  - RX: 210mA
  - TX: 455mA @ Pout=18.4dBm, HT20, EVM=-28dB

Terrovitis et al, ESSCIRC 2009 (Atheros)

Conclusions

- **CMOS has become the technology of choice for integrated radio systems**
- **Integrating a radio in mixed-Signal System-on-a-Chip is no longer a dream but a reality**
- **Wireless SoC can provide significant advantages in size, power, and cost**

Continuing Challenges

- Multi-mode radios to support several wireless standards
- RF design in scaled CMOS
  - Reduced supply voltage: voltage, current, time…
  - nanometer transistors: leaky, low gm.ro
  - How to reduce area and power
  - More “digital assistance”
- Challenges of radio designers have been, are, and will continue to be:
  - Power consumption / Battery life
  - Range
  - Data rate
  - Cost

Acknowledgments

- **Many of the slides are based on previous presentations from Qualcomm Atheros and Stanford University, especially those by:**

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