Analog and RF circuit techniques in nanometer CMOS

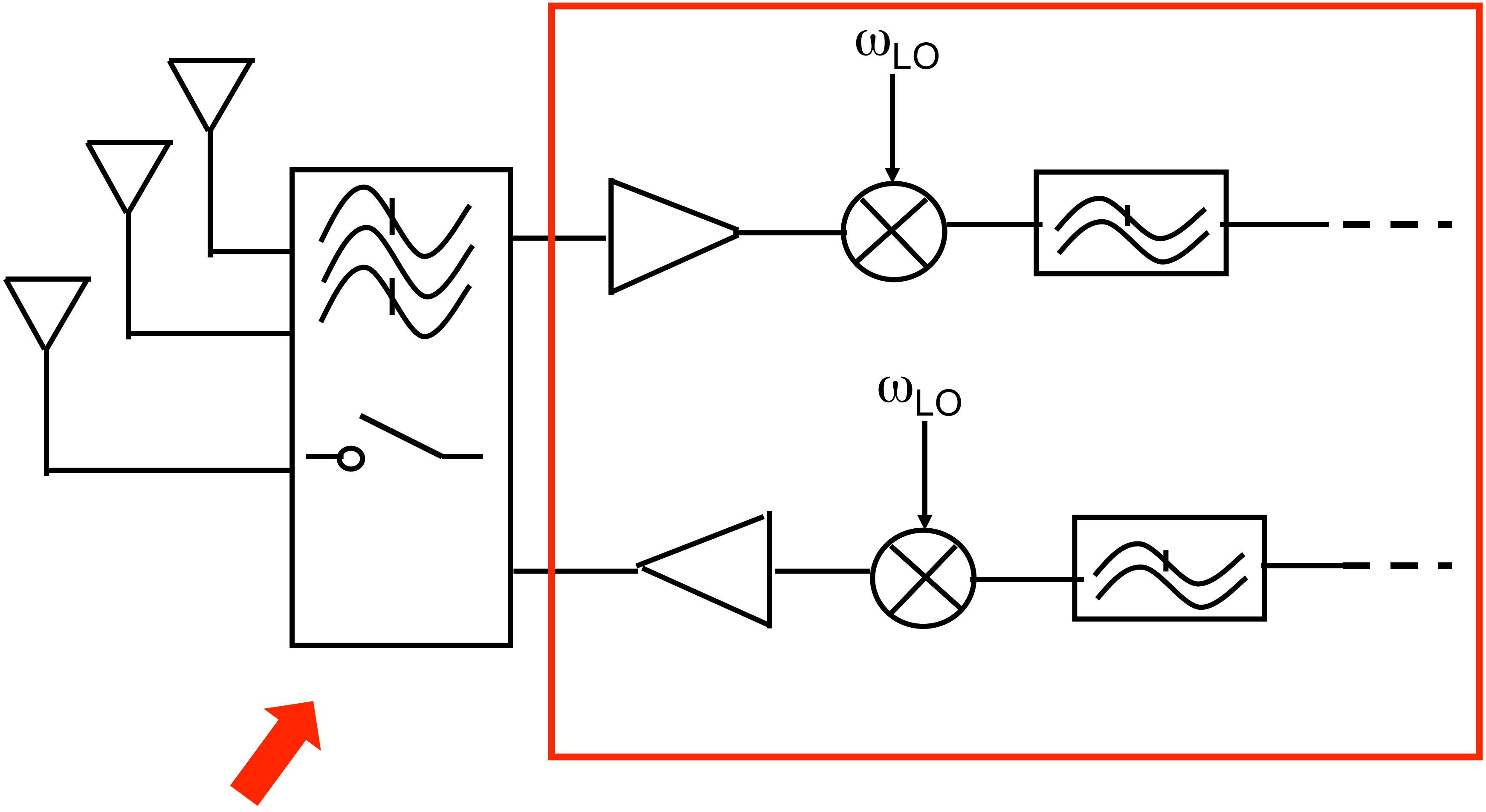
Bram Nauta
University of Twente
The Netherlands
http://icd.ewi.utwente.nl
b.nauta@utwente .nl

UNIVERSITY OF TWENTE.

Outline

- Introduction
- Balun-LNA-Mixer (BLIXER)
- Interferer robust SDR RX – analog part
- Interferer robust SDR RX – digital part
- Summary

Preferred: one wide band frontend IC:
Software Defined



Keep minimal

RF system trend (I)

- Challenges **wide band** circuits:

Minimal pre-filtering: → high linearity

No high Q tanks: → low noise

- Bandwidth will be ok for low GHz

- Towards Software Defined Radio

Outline

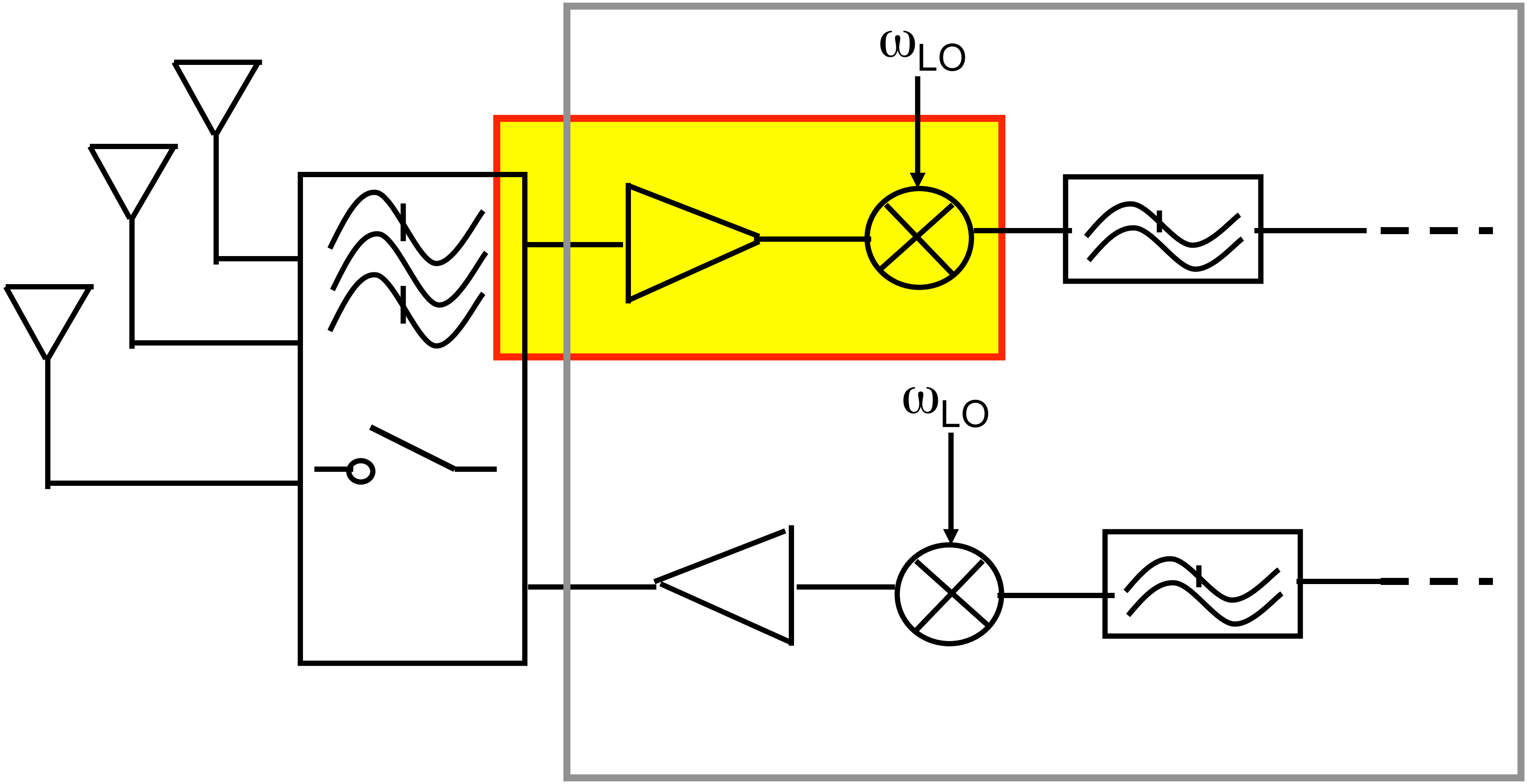
- Introduction
- **Balun-LNA-Mixer (BLIXER)**
- Interferer robust SDR RX – analog part
- Interferer robust SDR RX – digital part
- Summary

BLIXER

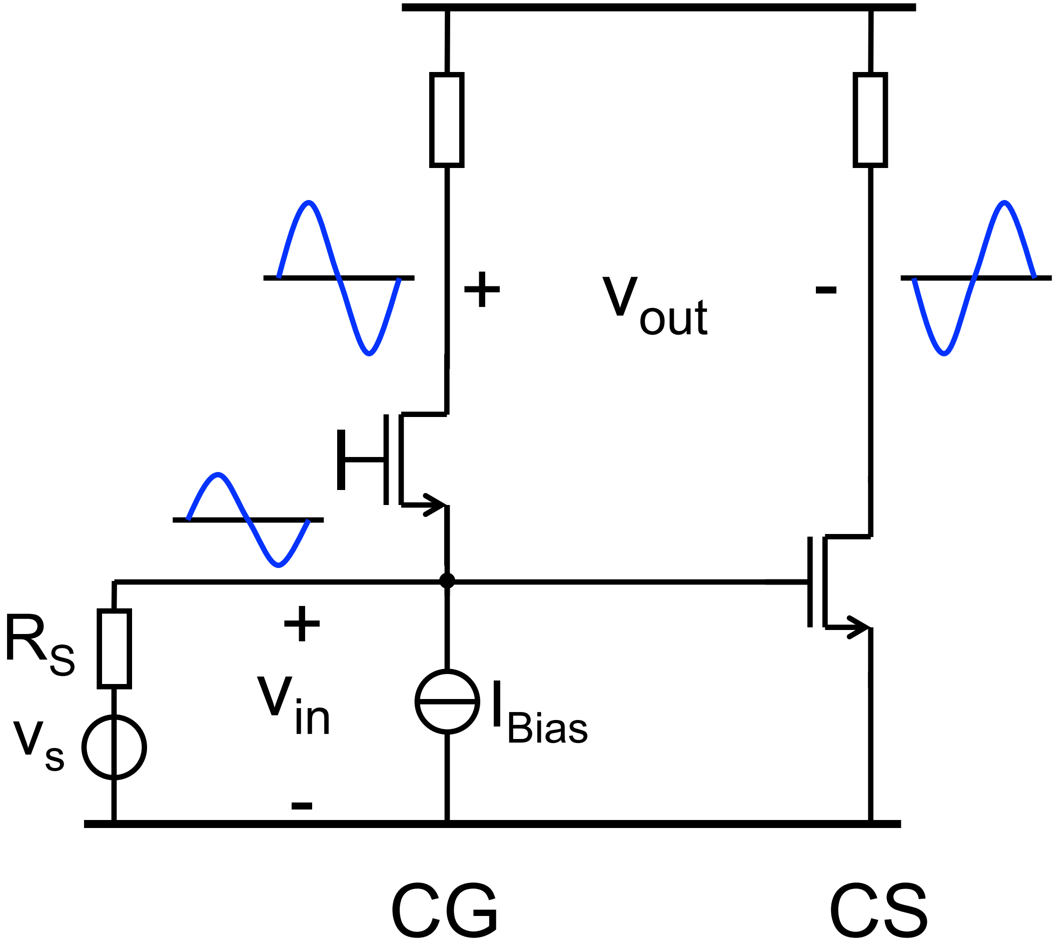
Balun + LNA + Mixer

[Blaakmeer, ISSCC2008]

BLIXER=Wide band receiver



Balun-LNA

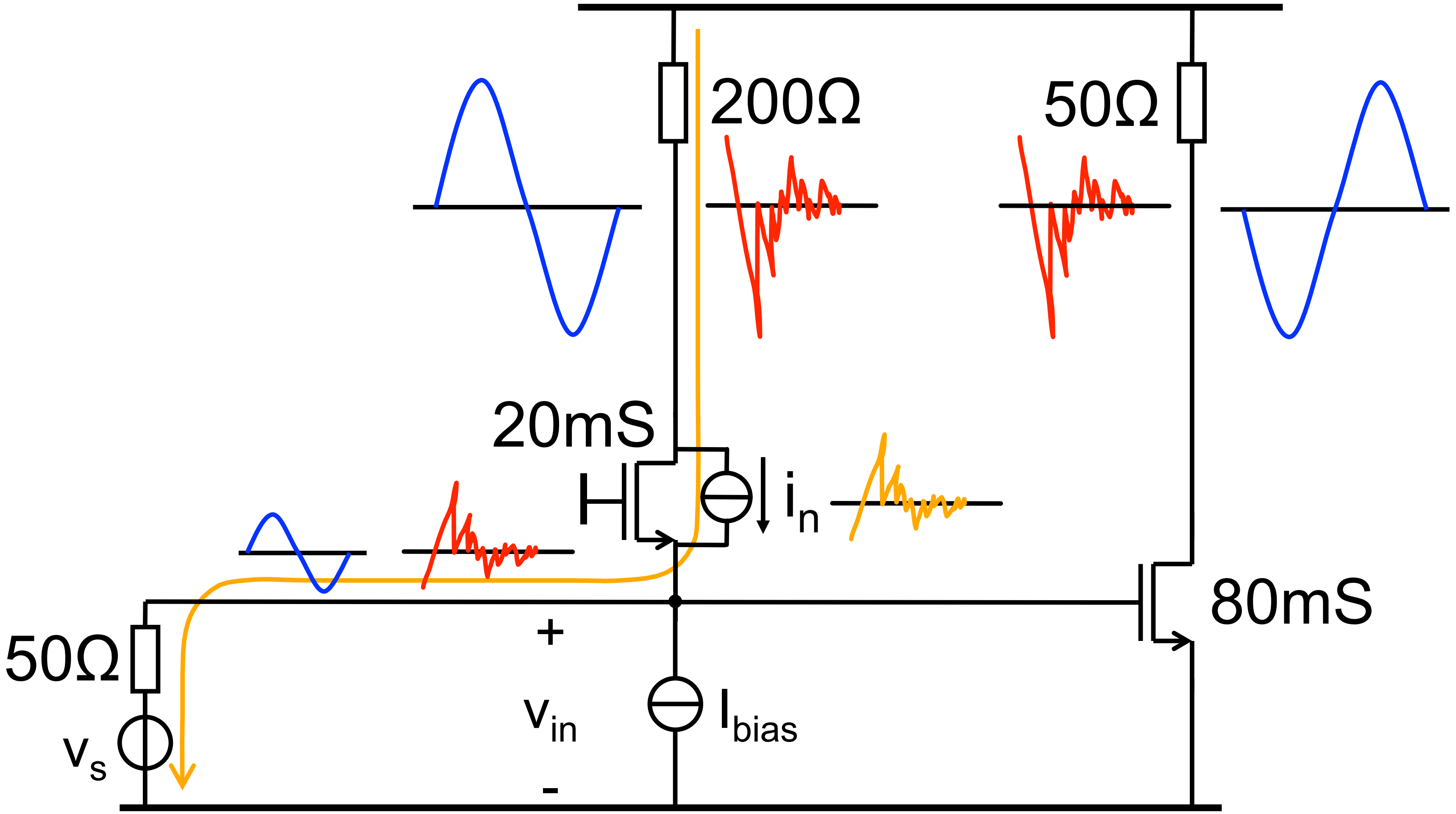


Simultaneous:

- Single-to-Differential
- Balanced Gain
- Broadband input match (~1/g_{mCG})
- Noise Canceling
- Distortion Canceling

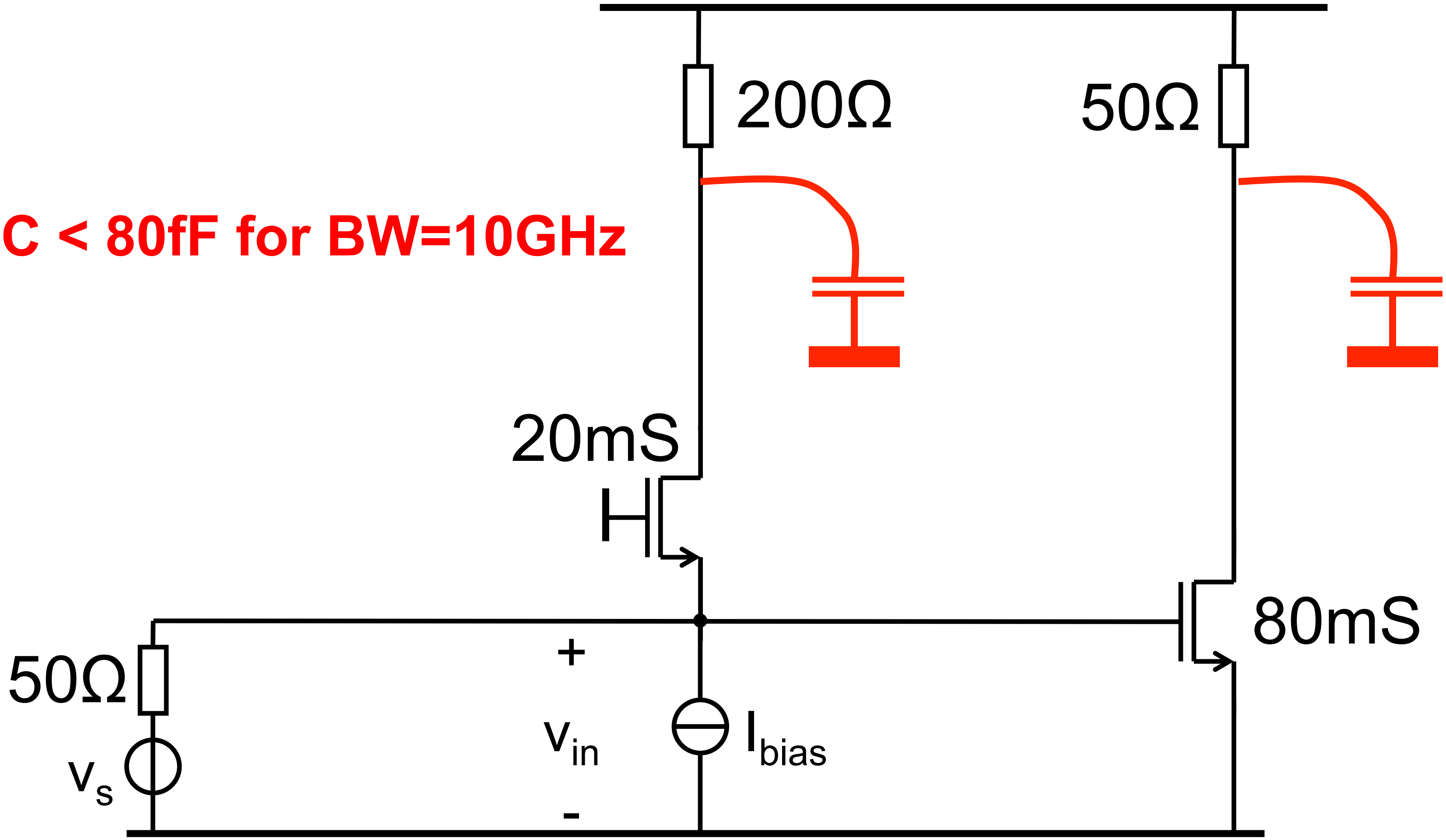
[Blaakmeer et al. ESSCIRC `07]

Noise Canceling

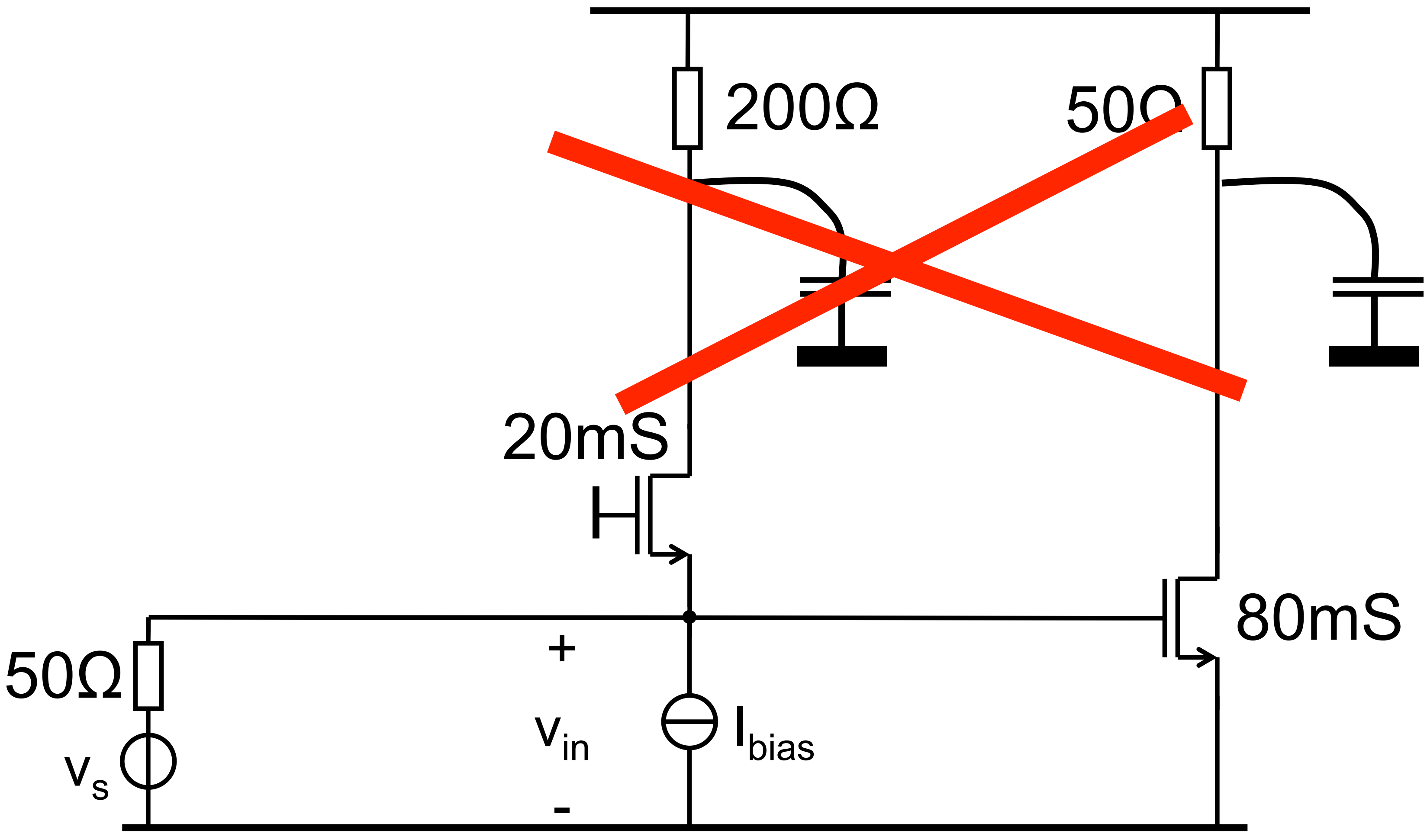


Bandwidth problem:

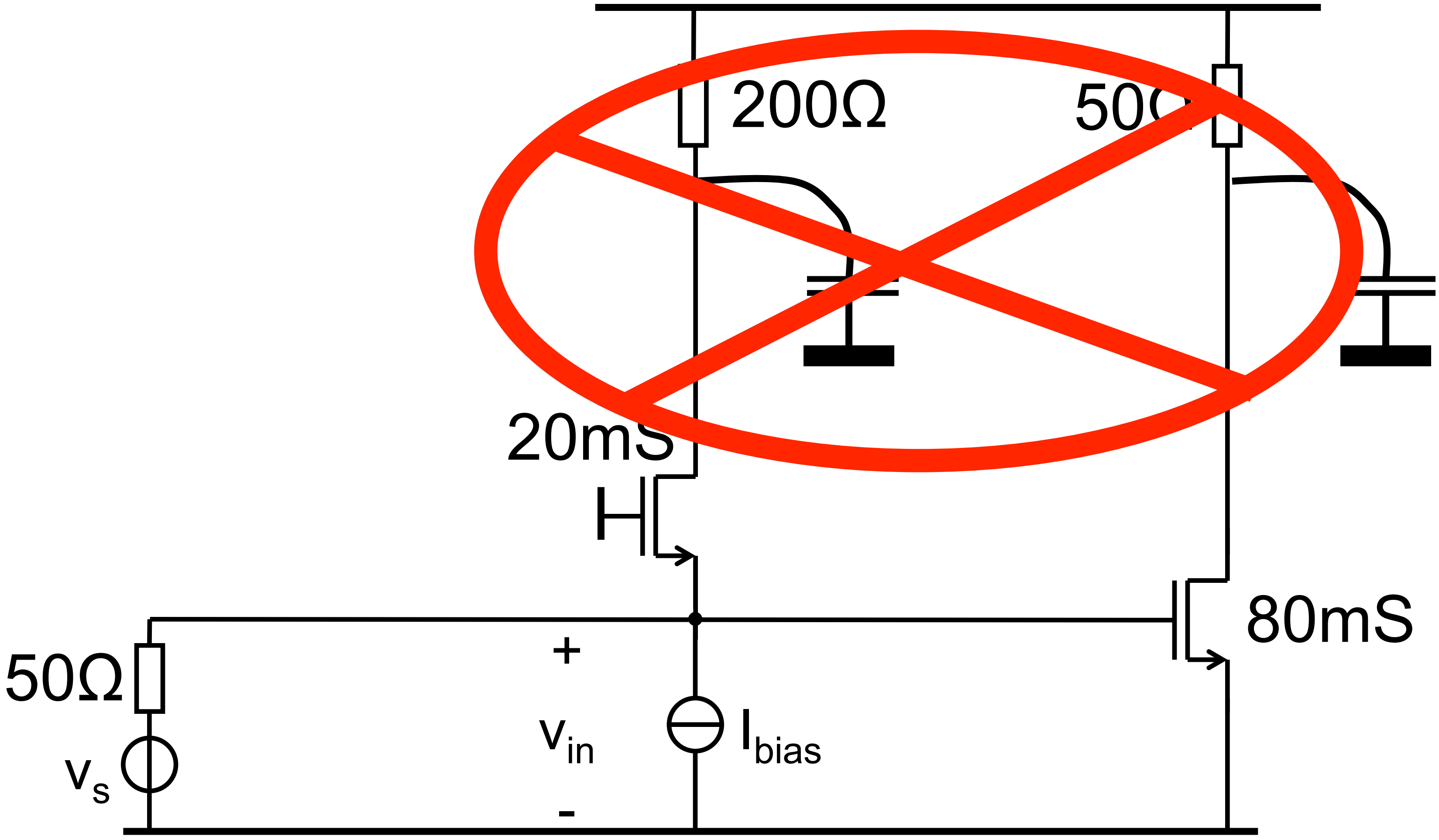
C < 80fF for BW=10GHz

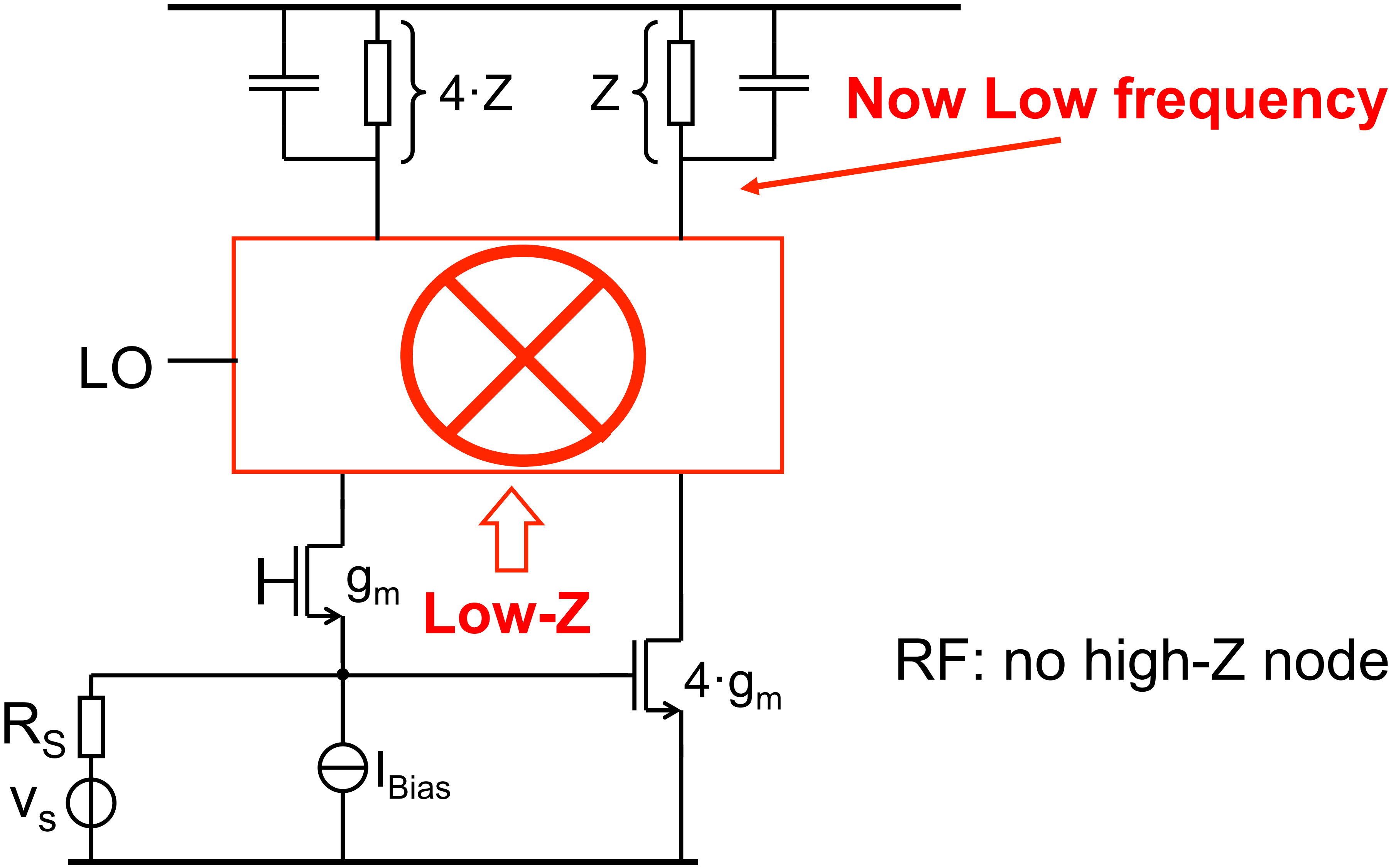


So, Don't make voltage gain @ RF



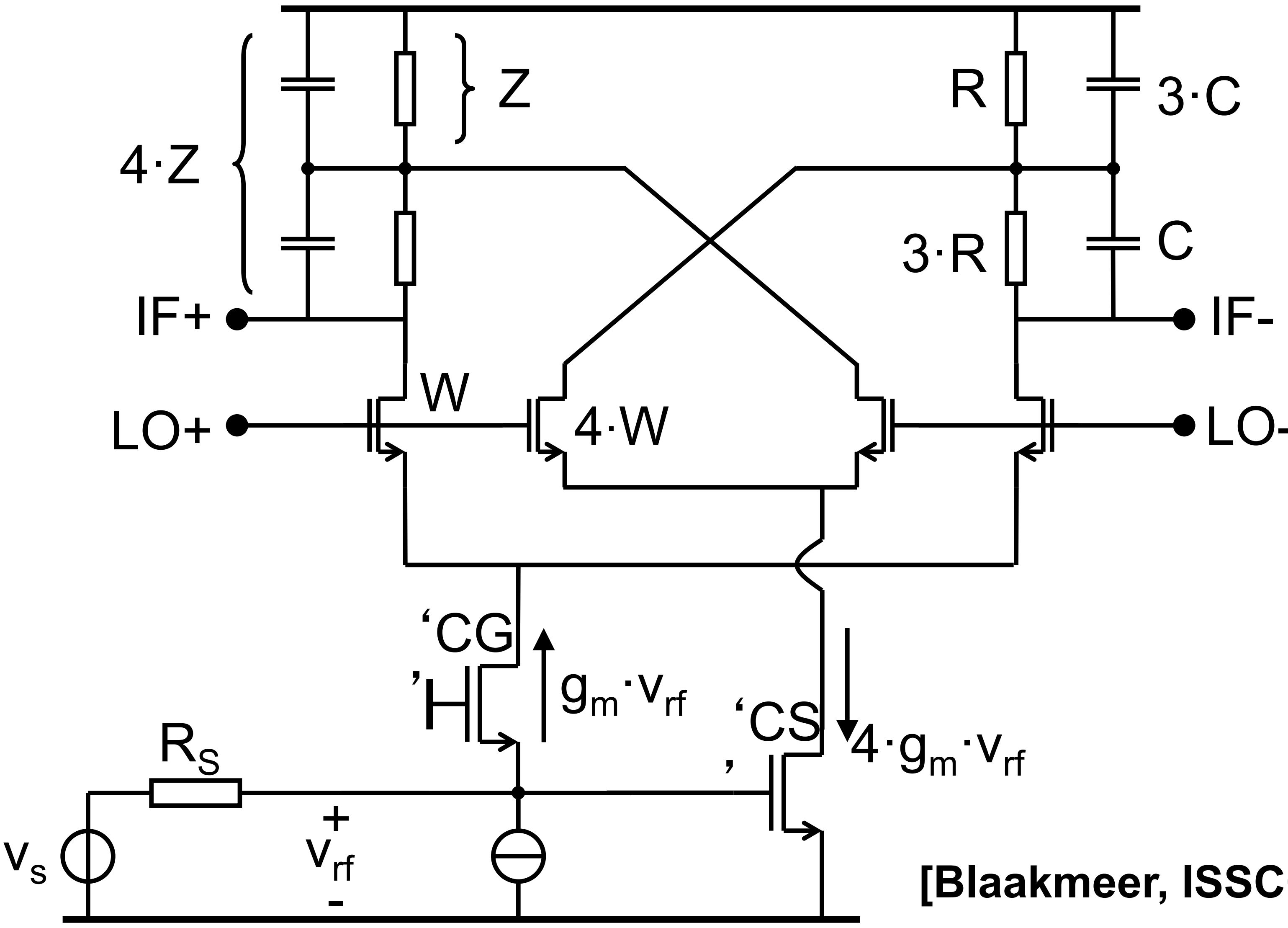
Use a MIXER





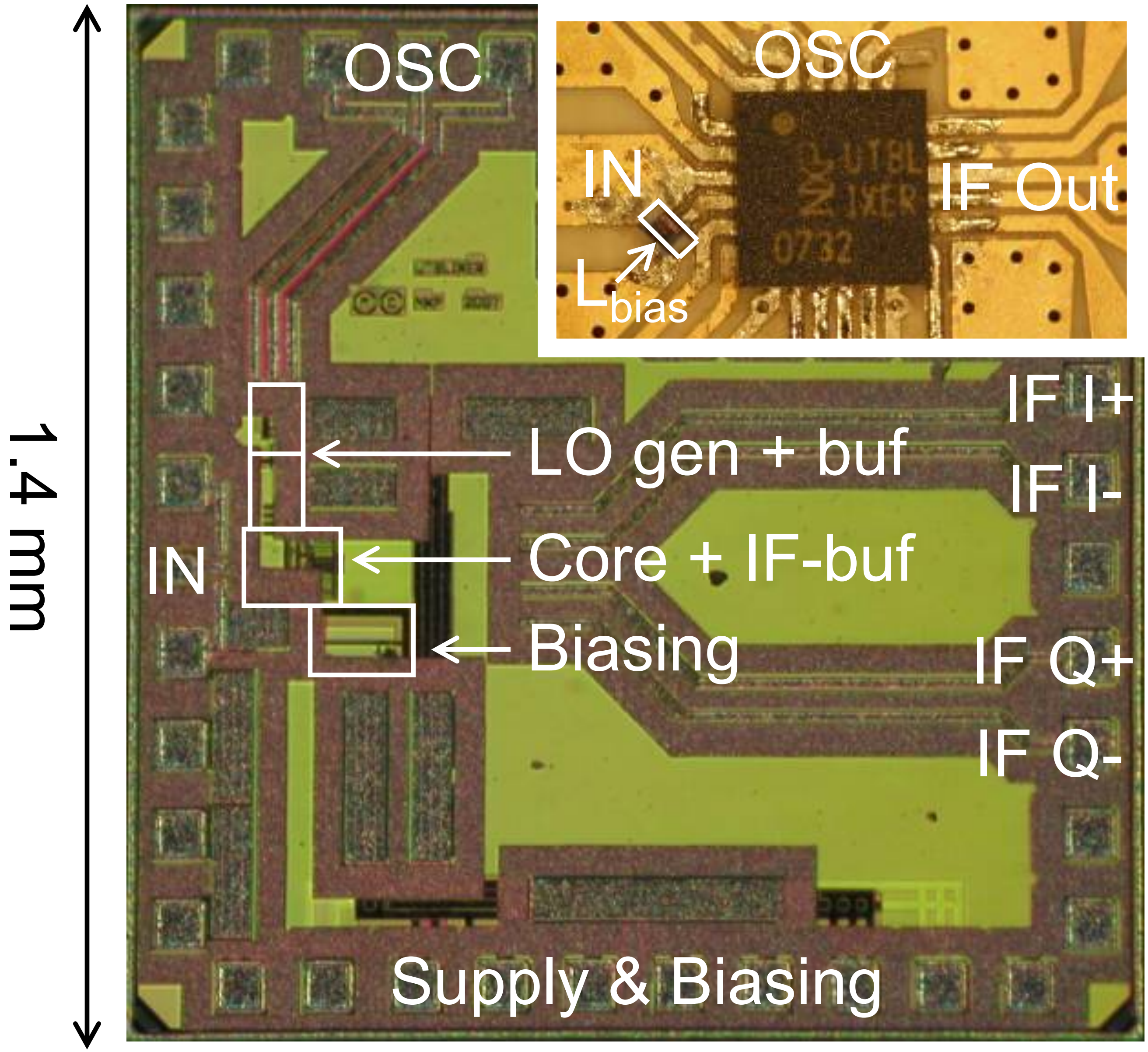
RF: no high-Z nodes

Mixer stacked on CG-CS stage



[Blaakmeer, ISSCC'08]

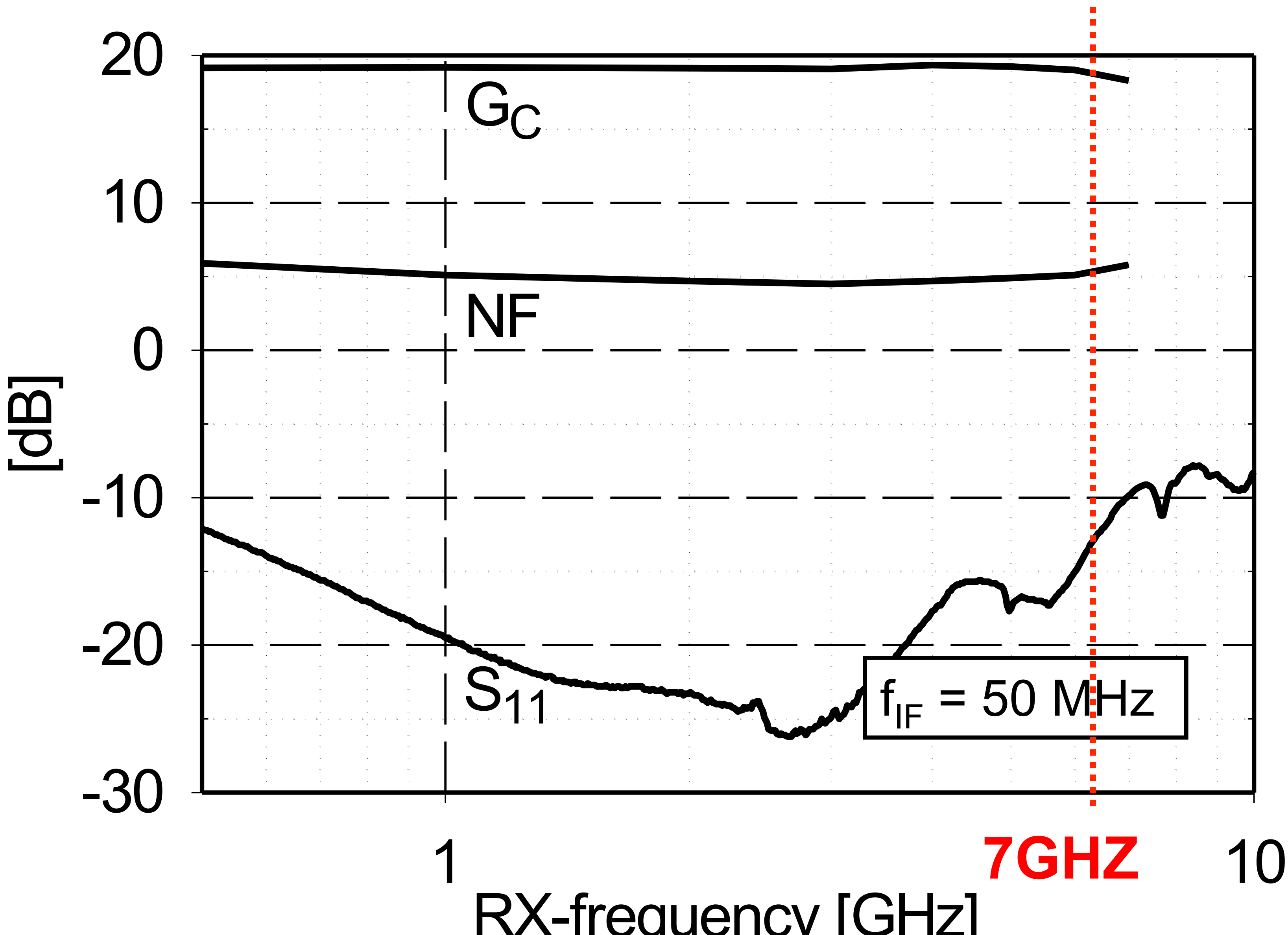
Chip Micrograph and PCB detail



Baseline
65nm CMOS
1.2V supply

Active area
< 0.02 mm^2

Conversion Gain, NF and S_{11}



Other BLIXER Performance

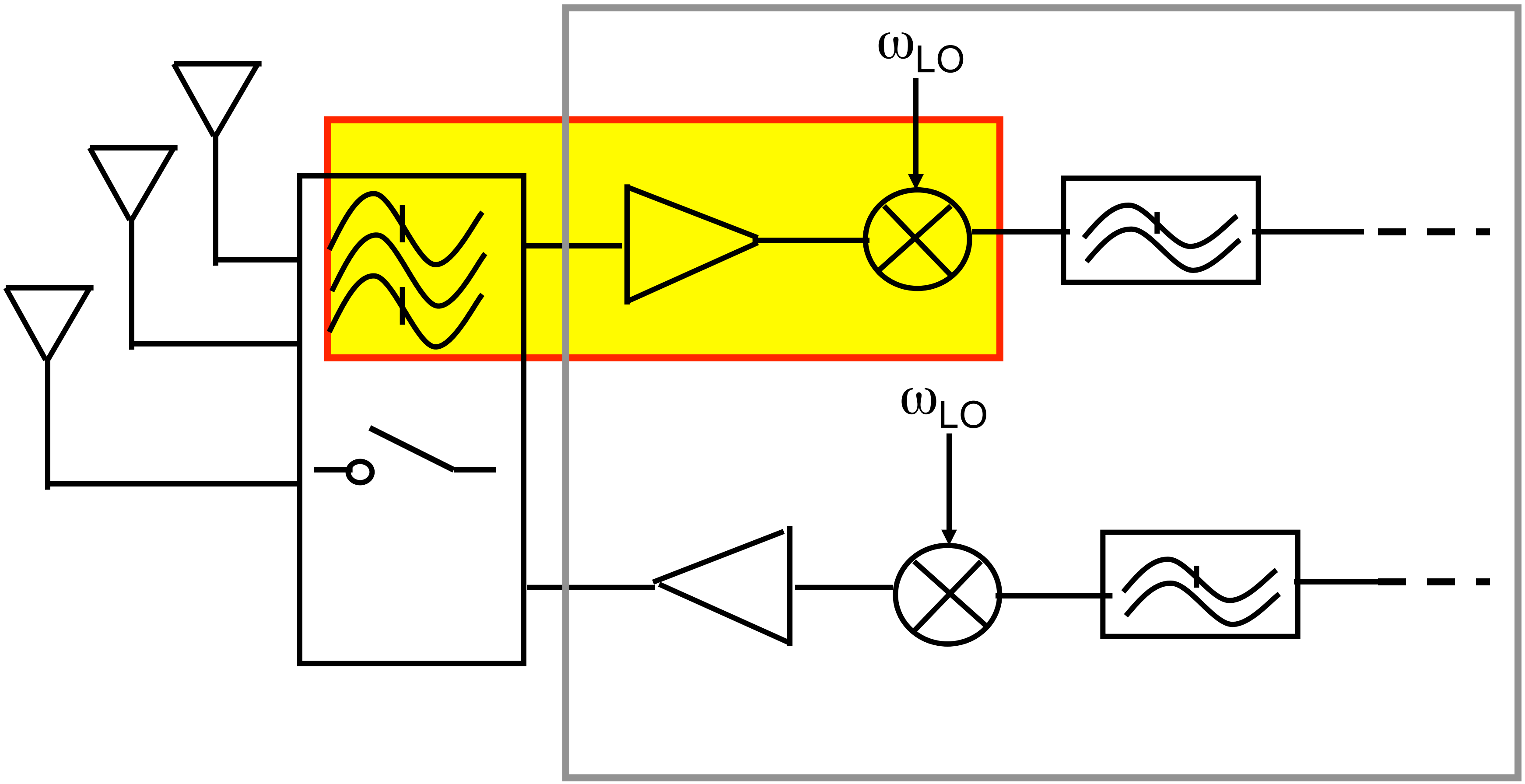
- Linearity:
  - IIP3 @ RF: -3 dBm
  - IIP2 @ RF: +20 dBm
- Quadrature accuracy:
  - Phase error < 3°
  - Gain error < 1dB
- LO leakage < -50 dBm
- Dissipation
  - 33mW (LO=500MHz)
  - 57mW (LO=7GHz)

Outline

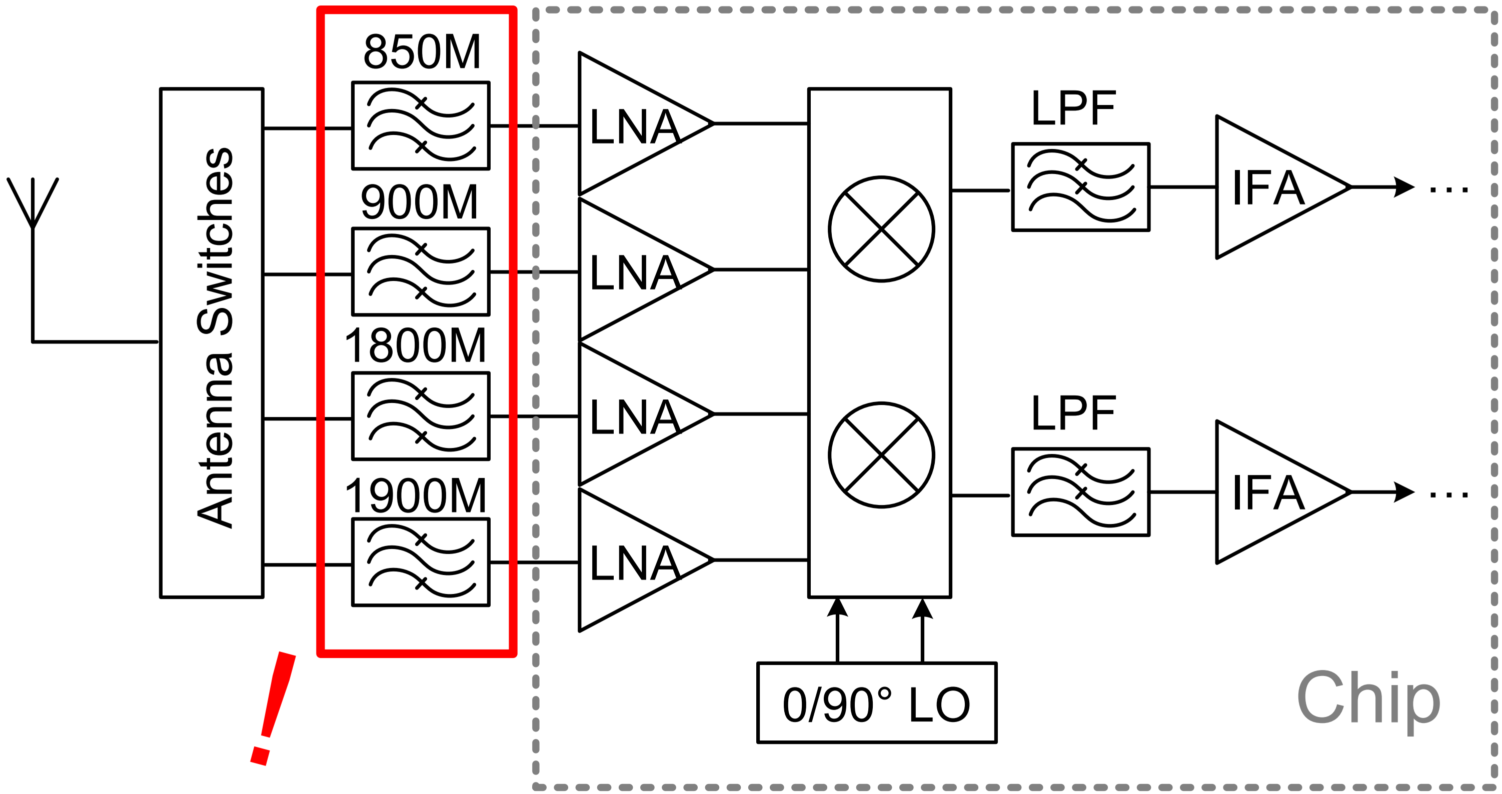
- Introduction
- Balun-LNA-Mixer (BLIXER)
- **Interferer robust SDR RX – analog part**
- Interferer robust SDR RX – digital part
- Summary

A Software-Defined Radio Receiver Architecture Robust to Out-of-Band Interference

[Ru, ISSCC 2009]

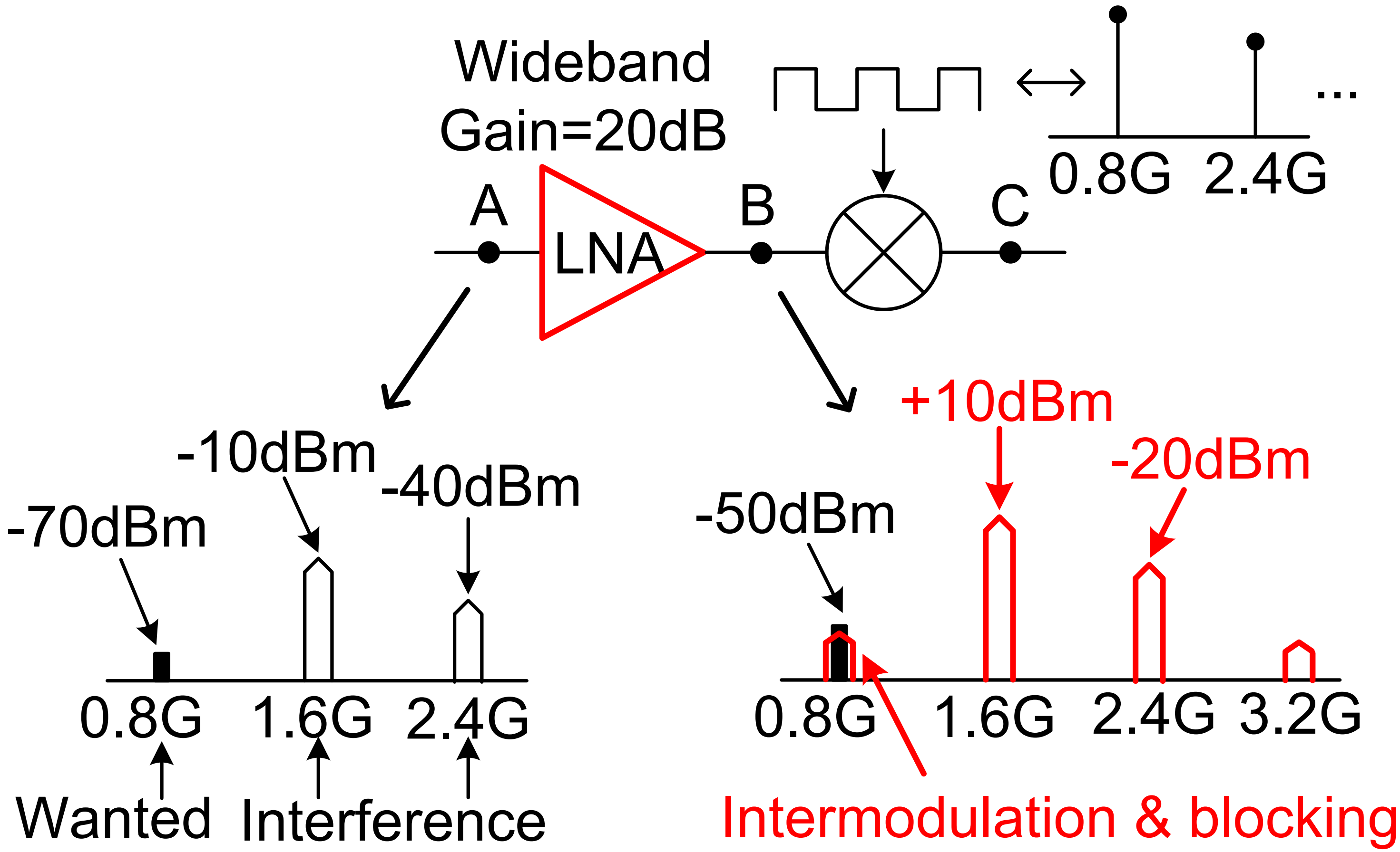

ωLO
ωLO

Conventional Multi-Band Receiver



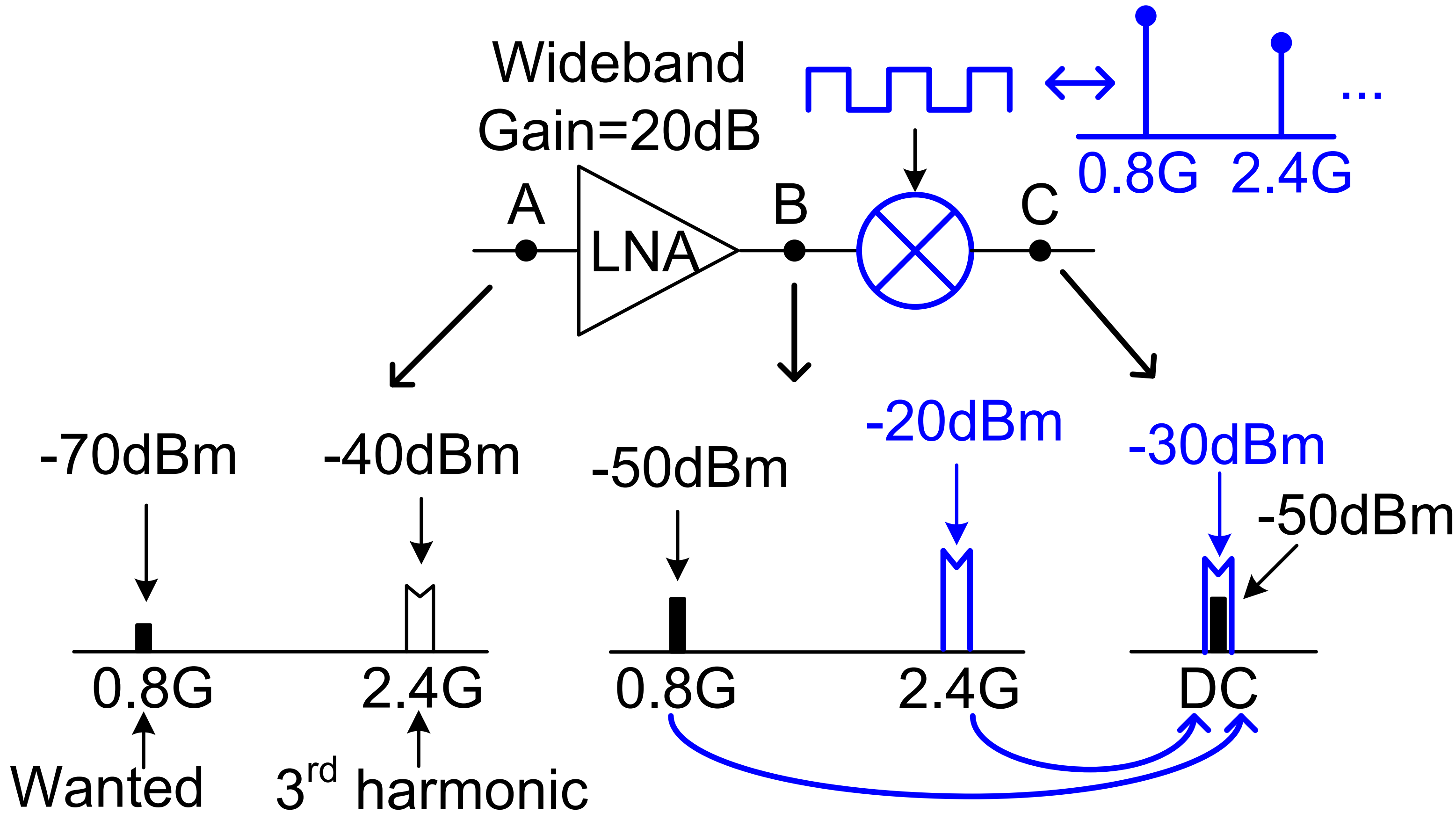
- RF filters for out-of-band interference, but bulky, costly, lossy, inflexible…
- **Our goal: Software Defined Radio with relaxed RF filtering**

Wideband Interfering: Nonlinearity



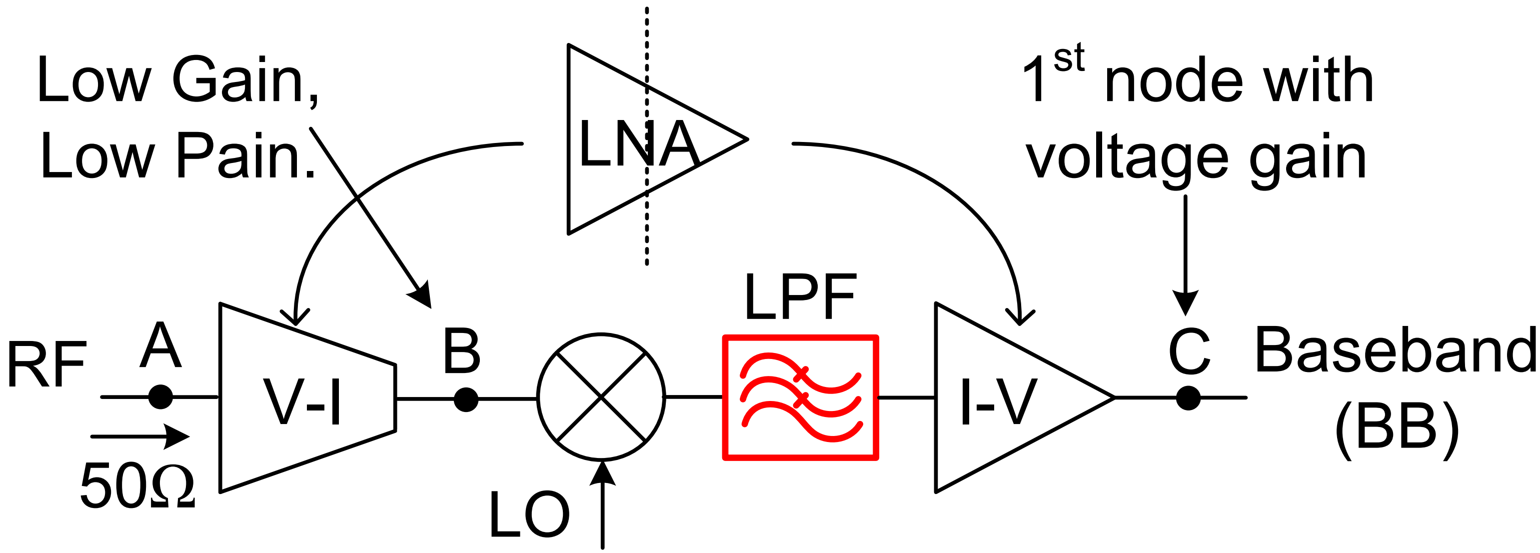
- Wideband LNA: also amplifies interference → nonlinearity

Wideband Interfering: Harmonic Mixing



- Switching mixer: square-wave LO → harmonic mixing

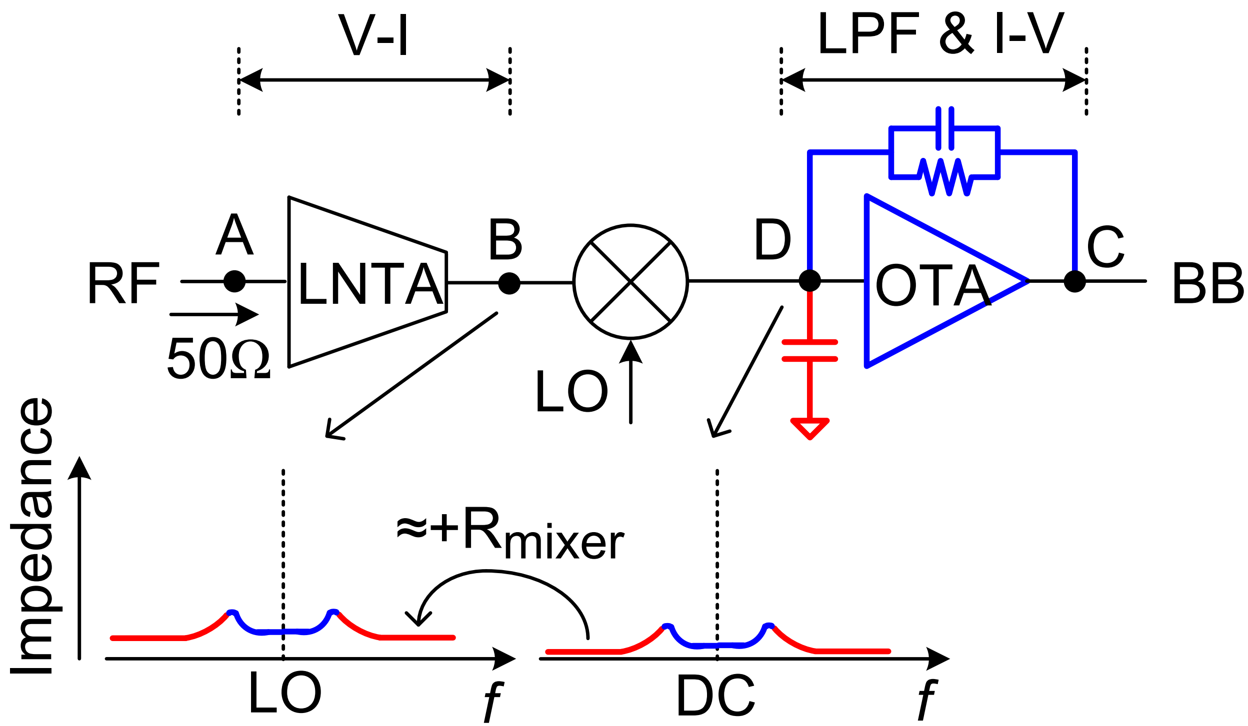
Concept: Use LP Filtering for Selectivity



• Voltage gain only at BB after **low-pass filter (LPF)** to filter blockers

→ Keep low impedance over a wide band at node B

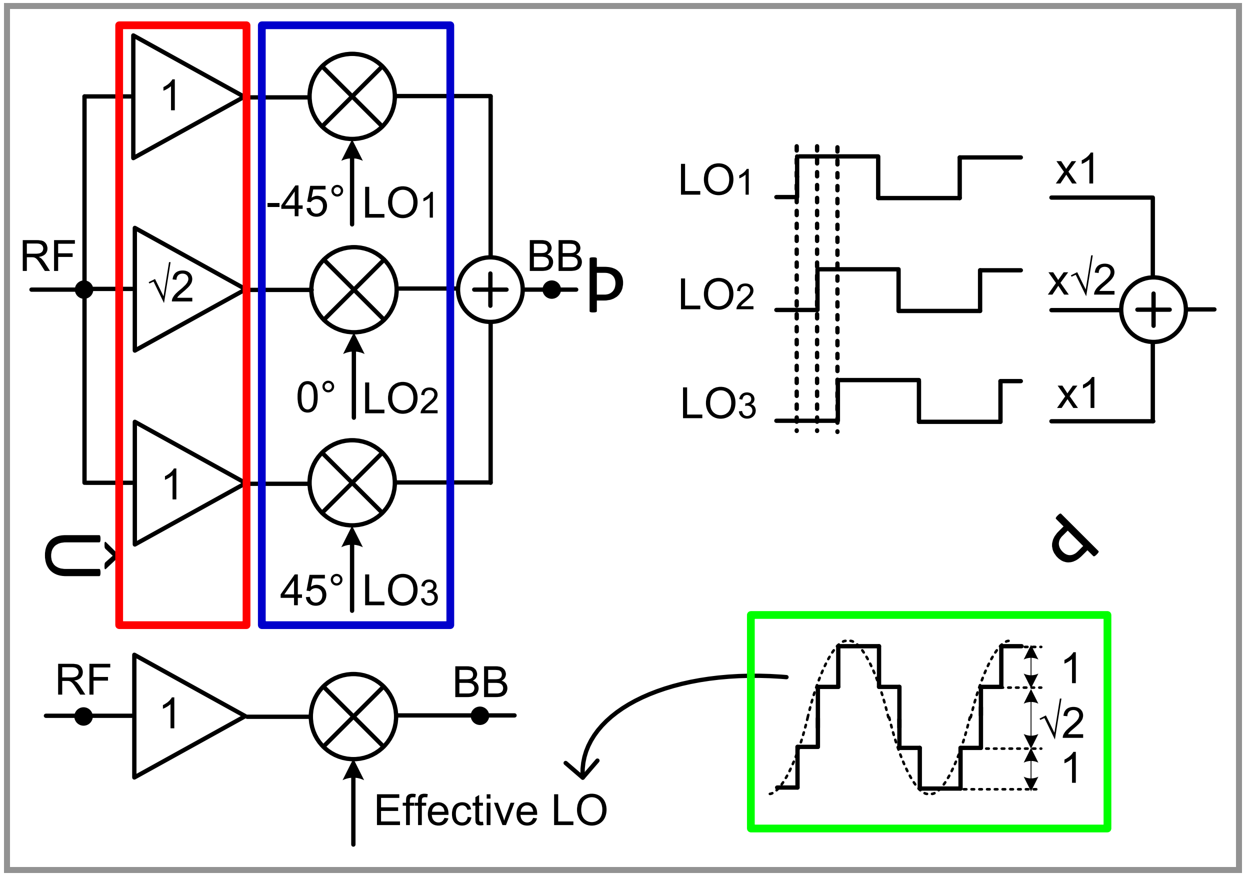
Realization: Wideband LNTA + Mixer + TIA

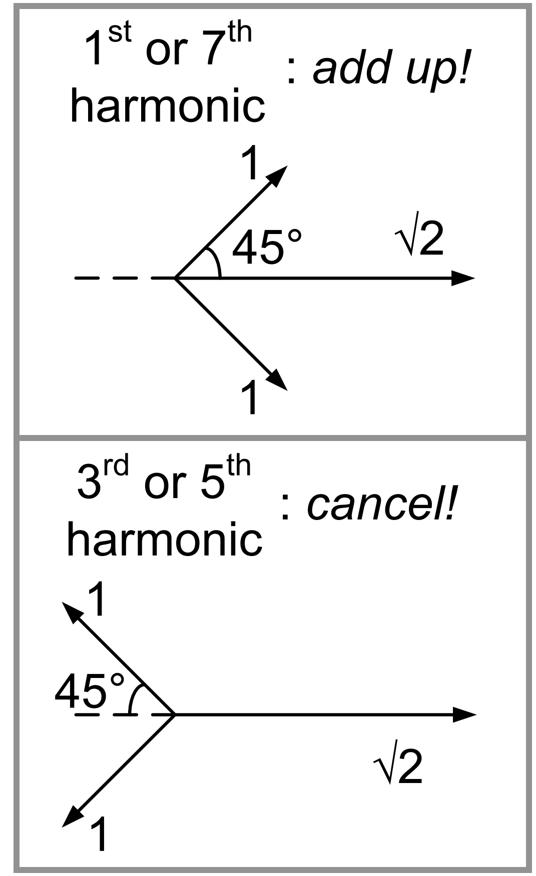


- LNTA: high G_m & high R_{out} → low noise
  small voltage swing at node B → good linearity
- Similar to [1], but now wideband and with blocker filtering

[1] Redman-White & Leenaerts, ESSCIRC07

Harmonic Rejection (HR) Mixer: Remove 3LO and 5LO



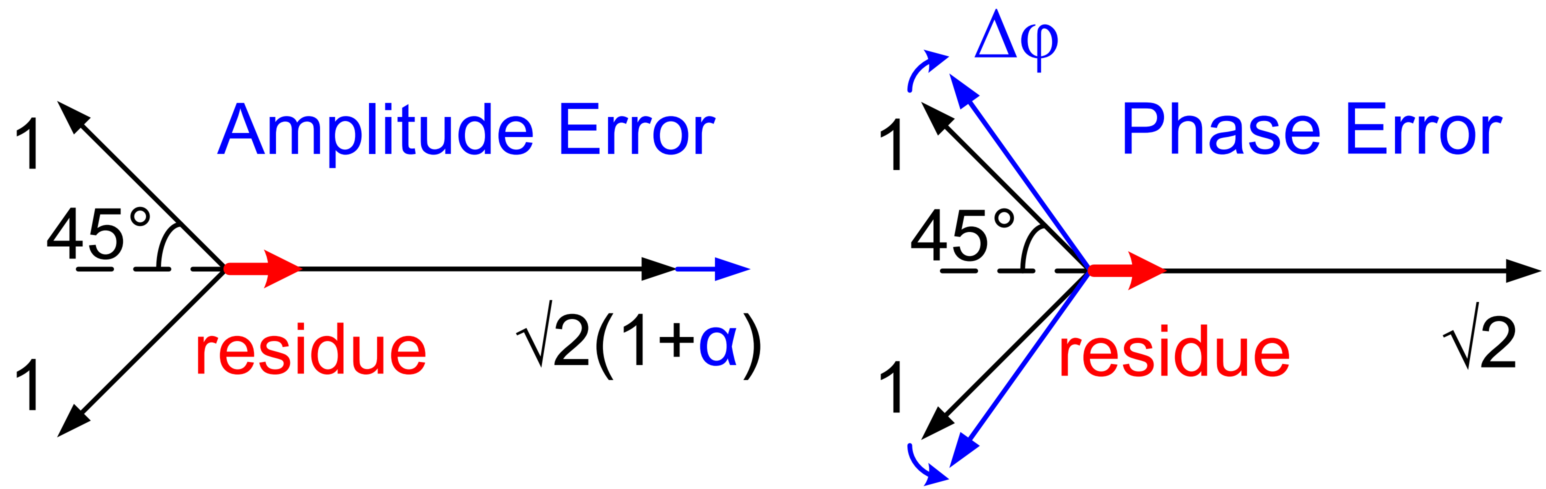


- Amplitude weighting + phase shifting → emulate sine-LO

[2] Weldon et. al., ISSCC01

Problem: Amplitude and Phase Errors

3rd or 5th harmonic vector diagram

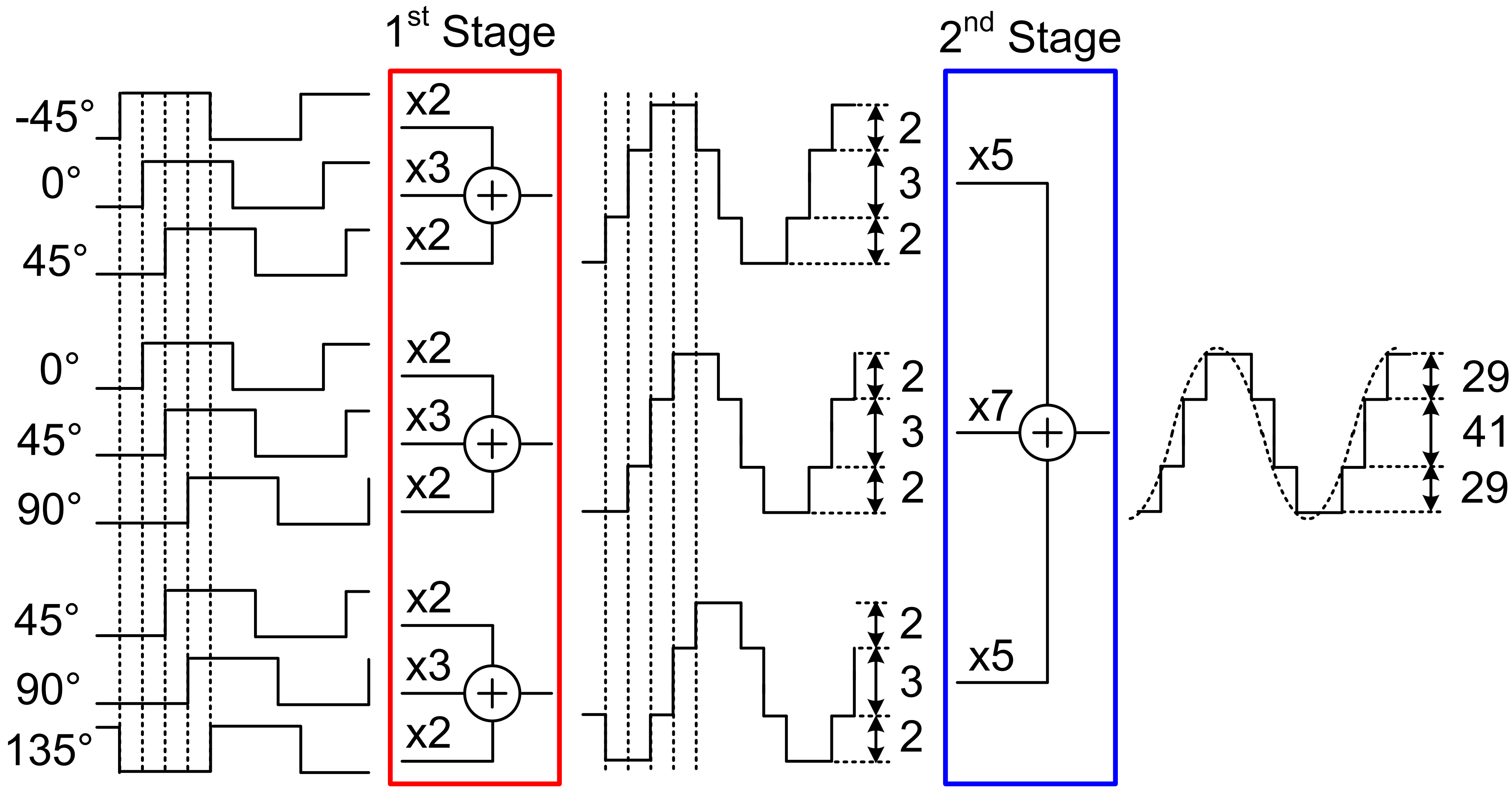


- Amplitude and phase errors

→ unwanted harmonic residue → degrade HR ratio

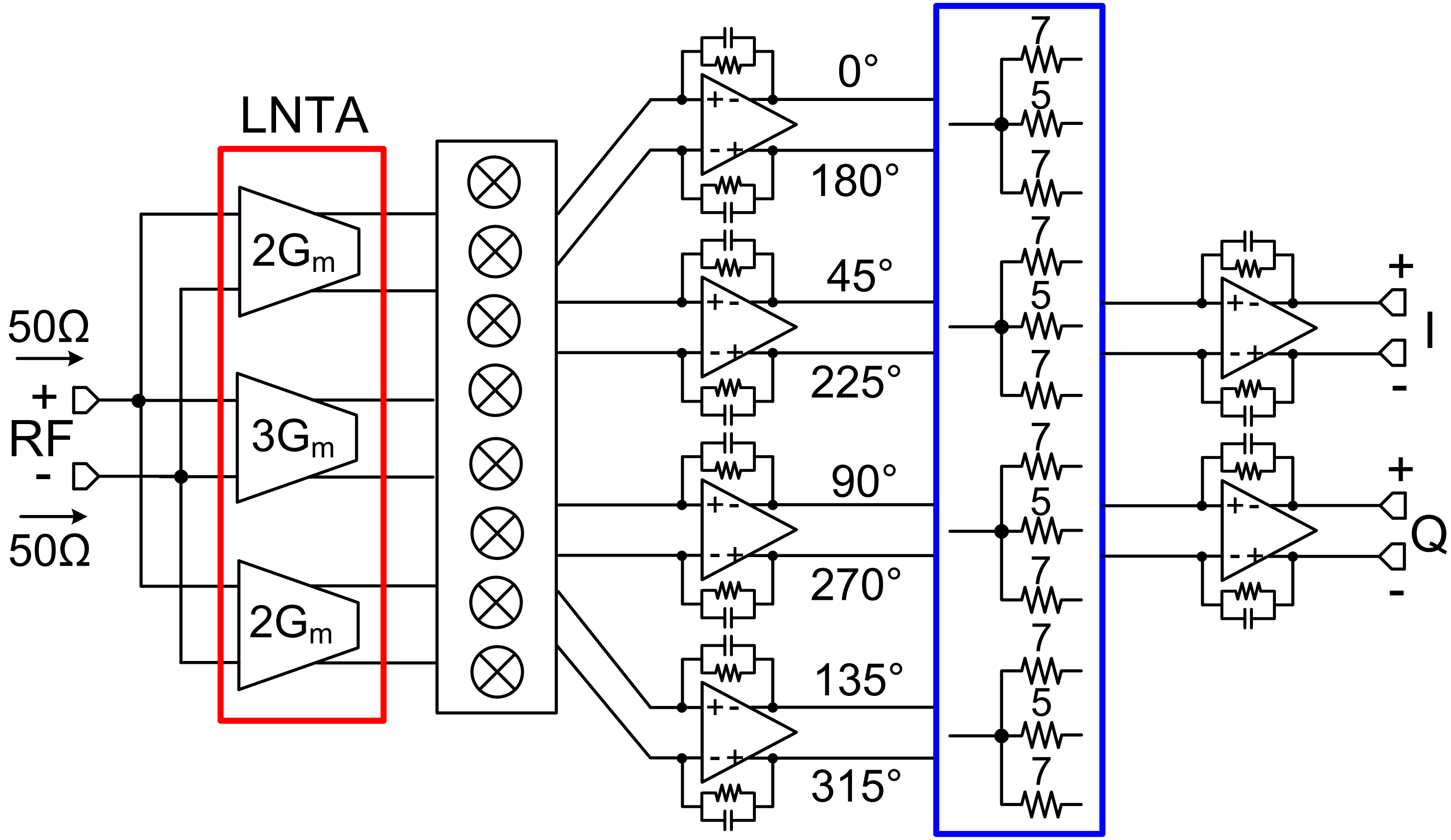
- How to make irrational ratio, e.g. √2, on chip?

2-Stage Polyphase HR: Concept



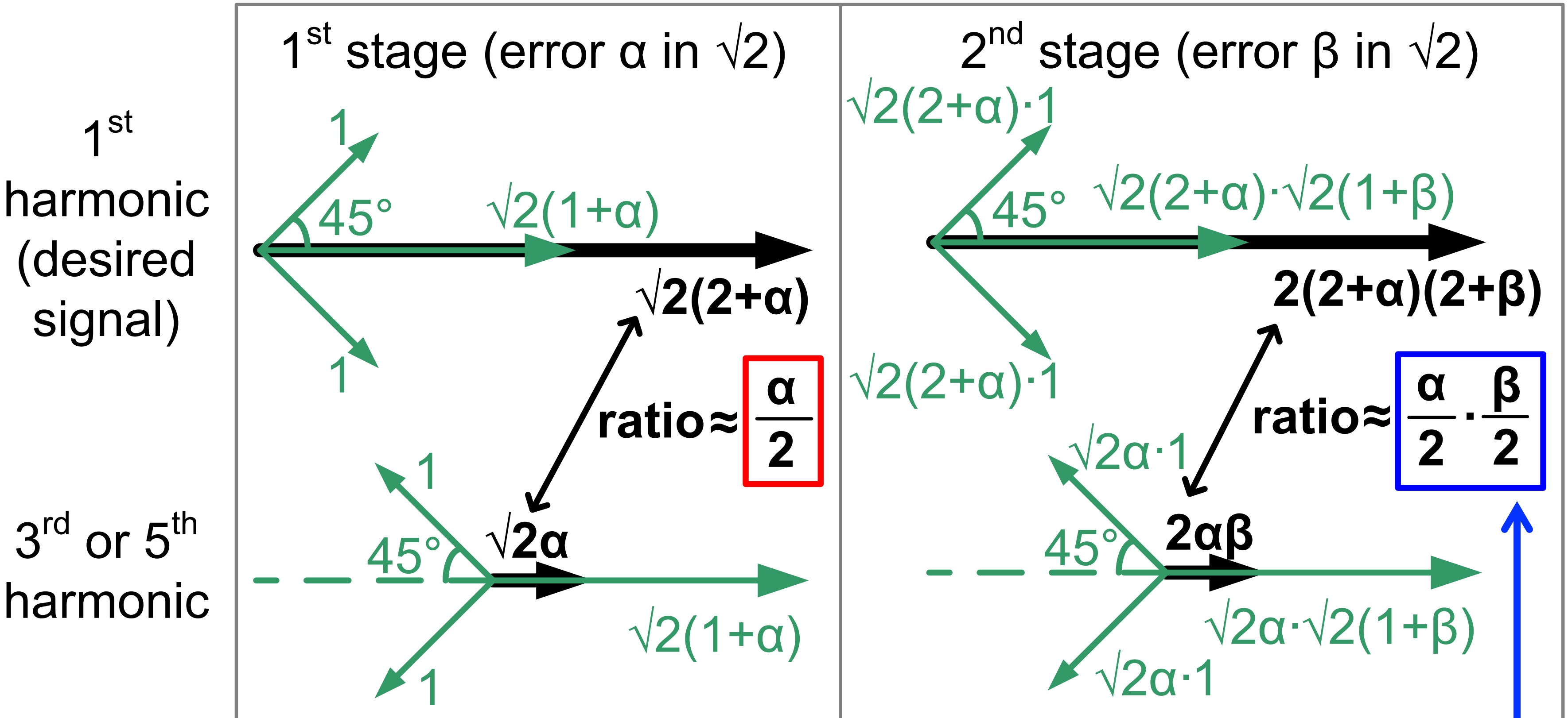
- 41/29=1.4138, √2=1.4142 → **ε=0.03%**

2-Stage Polyphase HR: Realization



- RF LNTA for 1st-stage weighting (2:3:2)
- BB resistor for 2nd-stage weighting (5:7:5)
- Nominally √2, what about influence of mismatch?

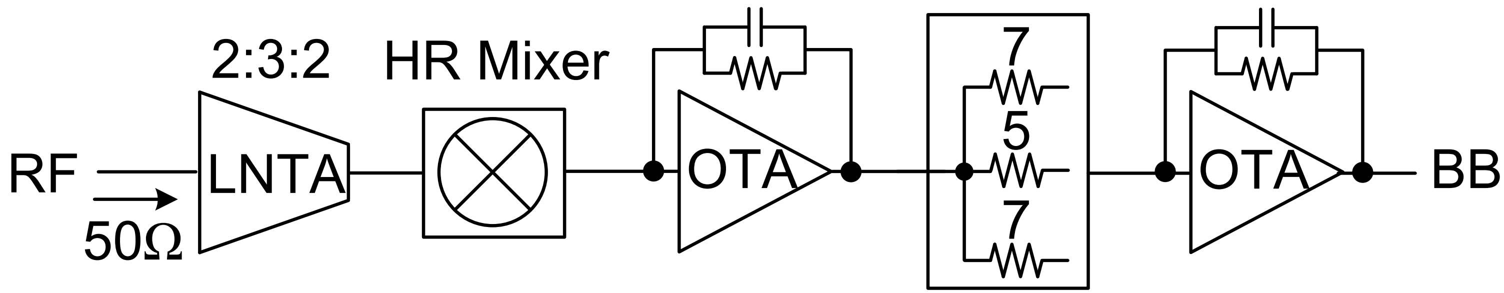
Reduced Effect of Amplitude Mismatch

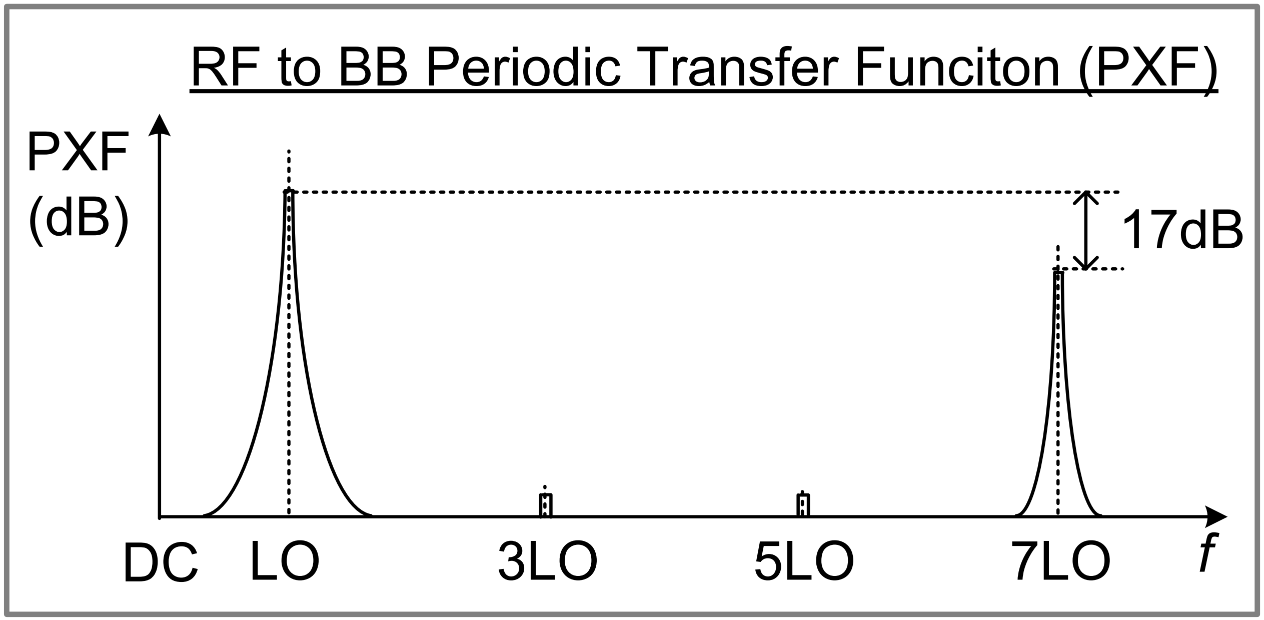


- 2-stage polyphase → product of relative errors
- E.g. 2:3:2 → α=6% → 1st-stage only: HR3=40dB

  5:7:5 → β=1% → 2-stage total: HR3=86dB

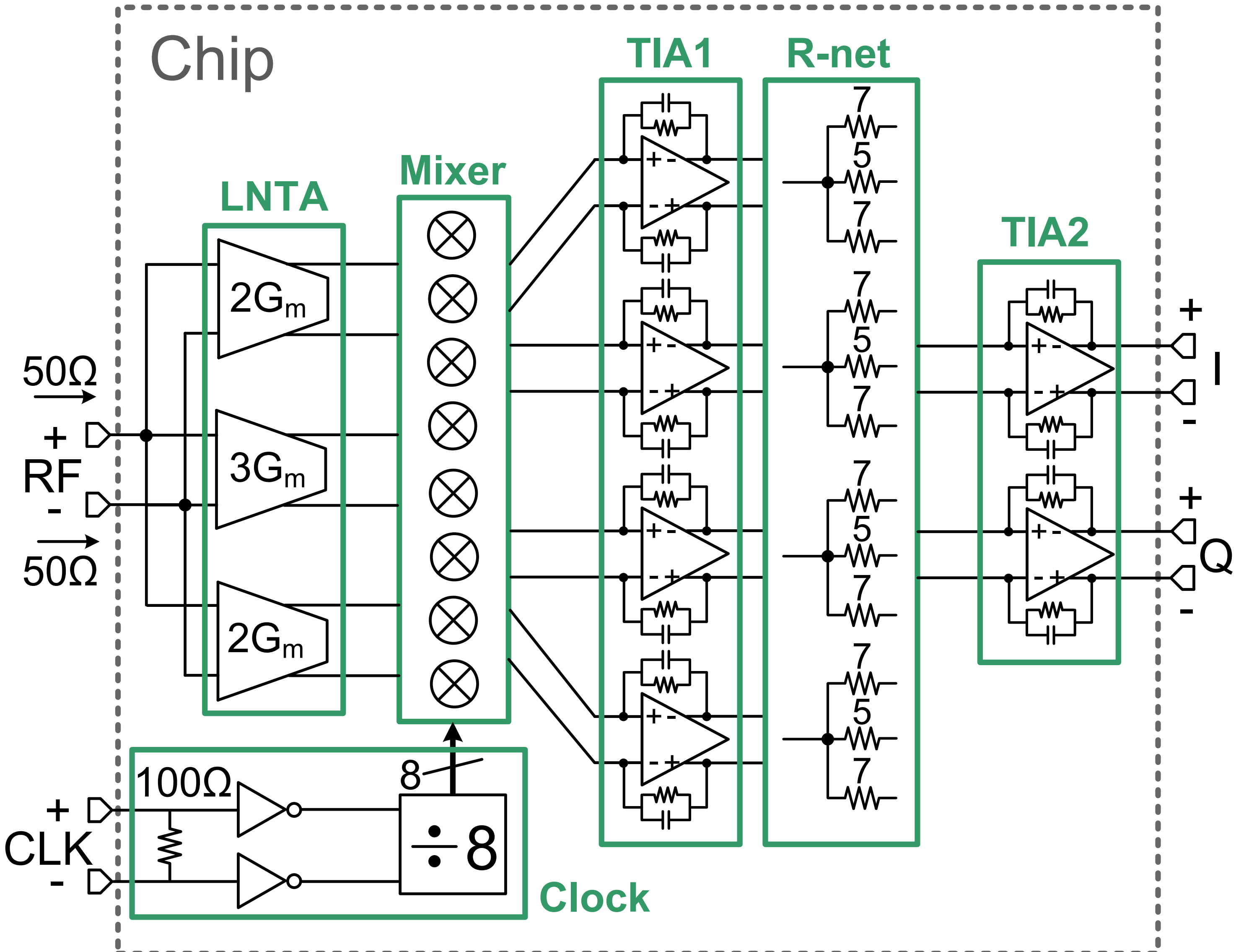
RF Filtering is Relaxed!



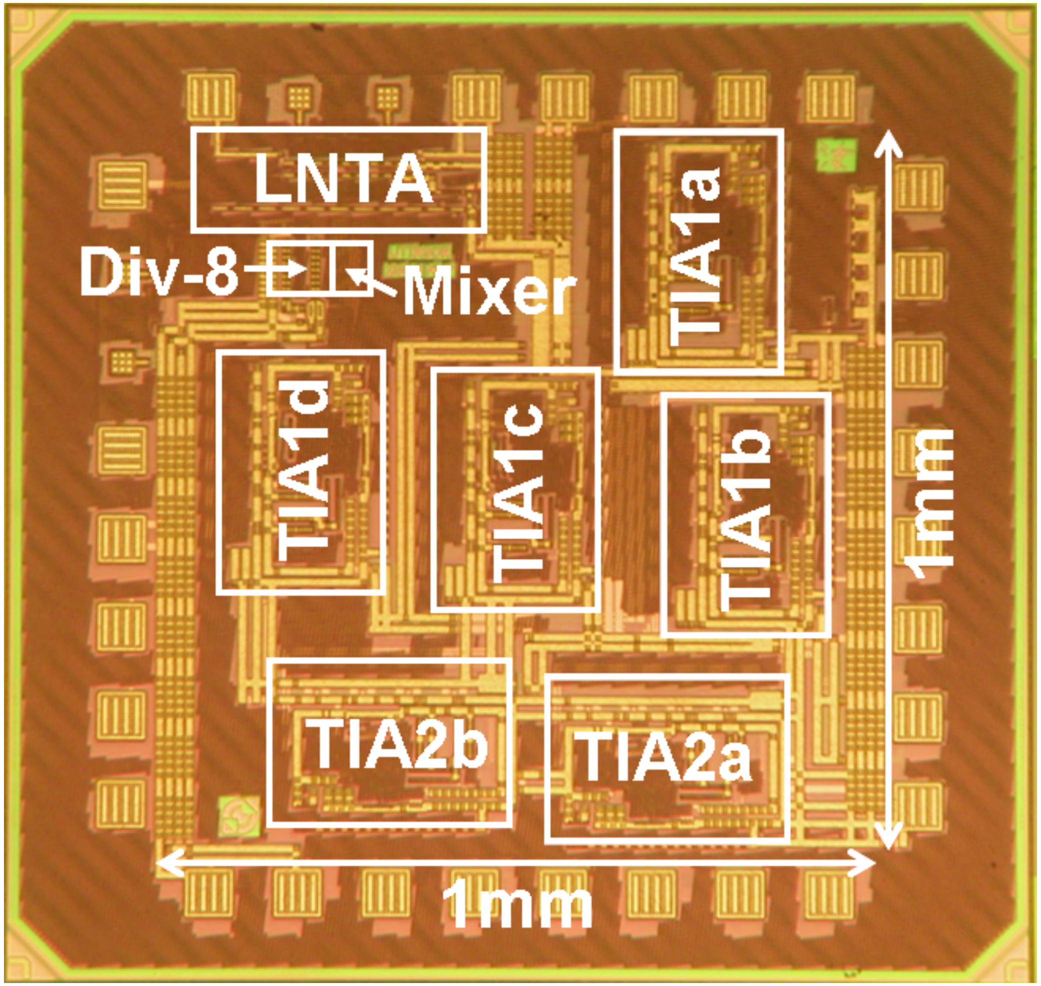


- LP blocker filtering: attenuates interference around LO
- 2-stage polyphase HR: *robustly* attenuates 3LO and 5LO

Zero-IF Receiver Prototype

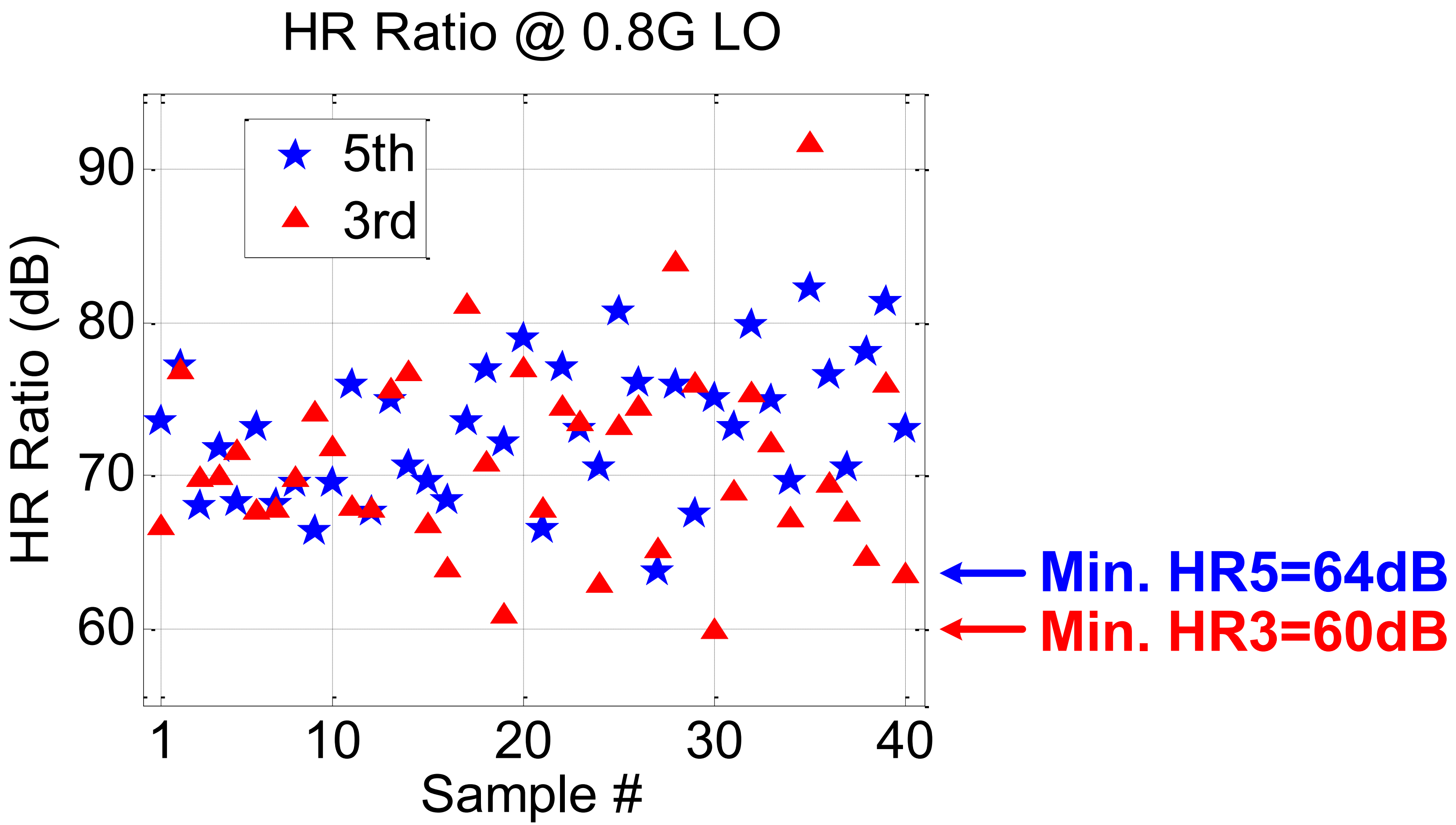


Chip Photo



- $1mm^2$ in 65nm CMOS
- VDD: 1.2V
- Current consumption:
  - Analog 33mA
  - Digital 17mA

Measured HR: 40 Chips



- **No trimming & calibration, no RF filtering**

Measured Performance Summary

LO Frequency	0.4~0.9GHz
Gain	34.4±0.2dB
DSB NF	4dB±0.5dB
S_{11} < -10dB	80M~5.5GHz
In/Out-of-band IIP3[1]	**+3dBm / +18dBm**
In/Out-of-band IIP2[2]	+46dBm / +51dBm
IF Bandwidth	12MHz
1/*f* noise	**30kHz** corner

VDD	1.2V
Current Consumption	Analog: 33mA
	Digital (clock): 8mA @ 0.4GHz 17mA @ 0.9GHz

Harmonic Rejection Ratio @ 0.8GHz LO	
3^{rd}-order	**> 60dB (40 chips)**
5^{th}-order	**> 64dB (40 chips)**
2^{nd}, 4^{th}, 6^{th}	**> 62dB (20 chips)**

[1] Out-of-band IIP3: two tones = 1.61G & 2.40GHz, LO = 819MHz

[2] Out-of-band IIP2: two tones = 1.80G & 2.40GHz, LO = 601MHz

Conclusion:
A SDR Receiver Architecture Robust to Out-of-Band Interference

- Only voltage gain @ BB after low-pass filtering
  - In-band IIP3 +3dBm & out-of-band IIP3 +18dBm

- 2-stage polyphase harmonic rejection technique
  - Robust: error = product of errors
  - Accurate multiphase clock
  - Minimum HR 60dB over 40 chips without calibration / trimming / RF filters

Outline

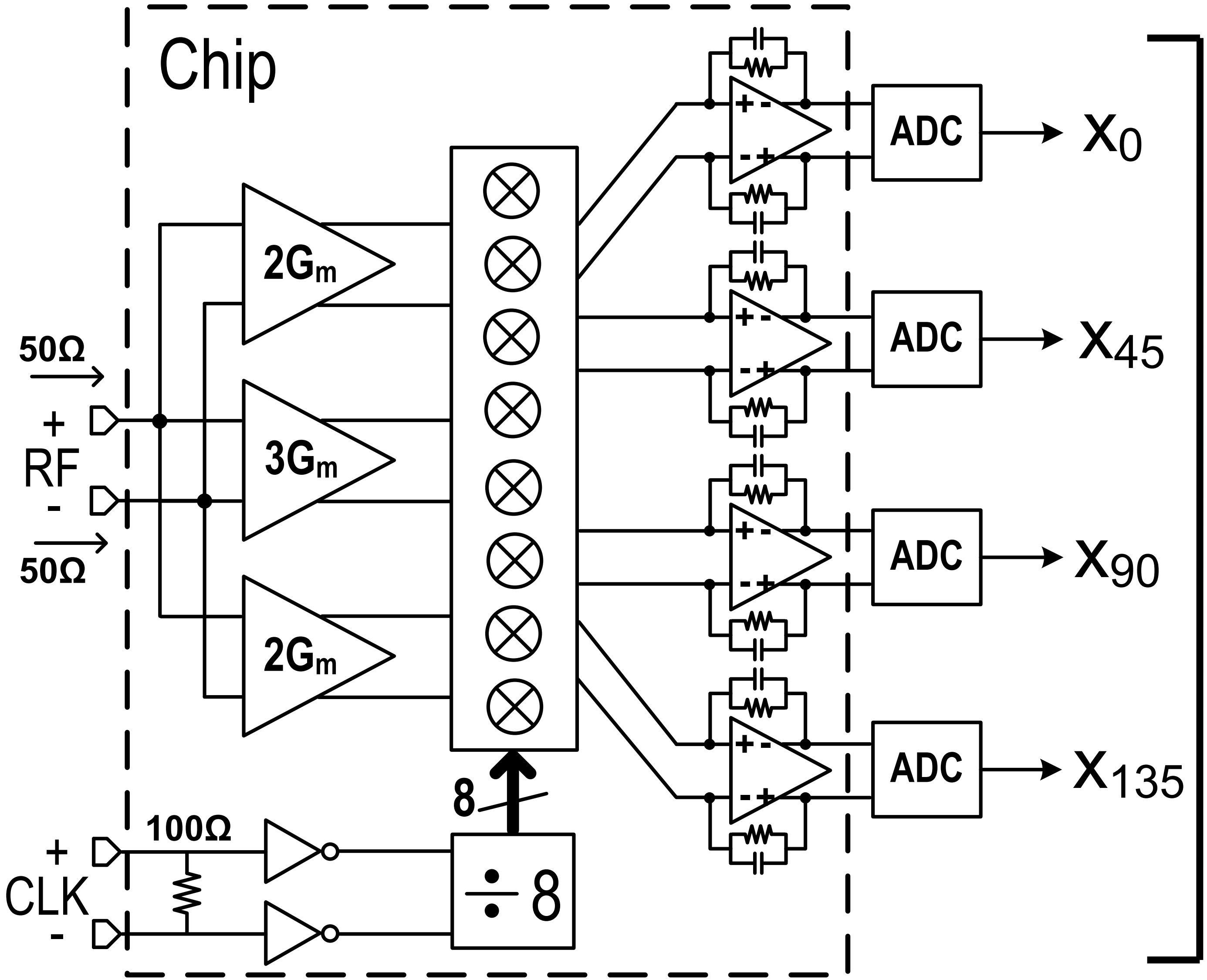
- Introduction
- Balun-LNA-Mixer (BLIXER)
- Interferer robust SDR RX – analog part
- **Interferer robust SDR RX – digital part**
- Summary

The Digital approach:

Harmonic Rejection Exploiting Adaptive Interference Cancellation

[Moseley, ISSCC 2009]

Harmonic Rejection RX: This work



To Digital Harmonic Rejection Algorithm

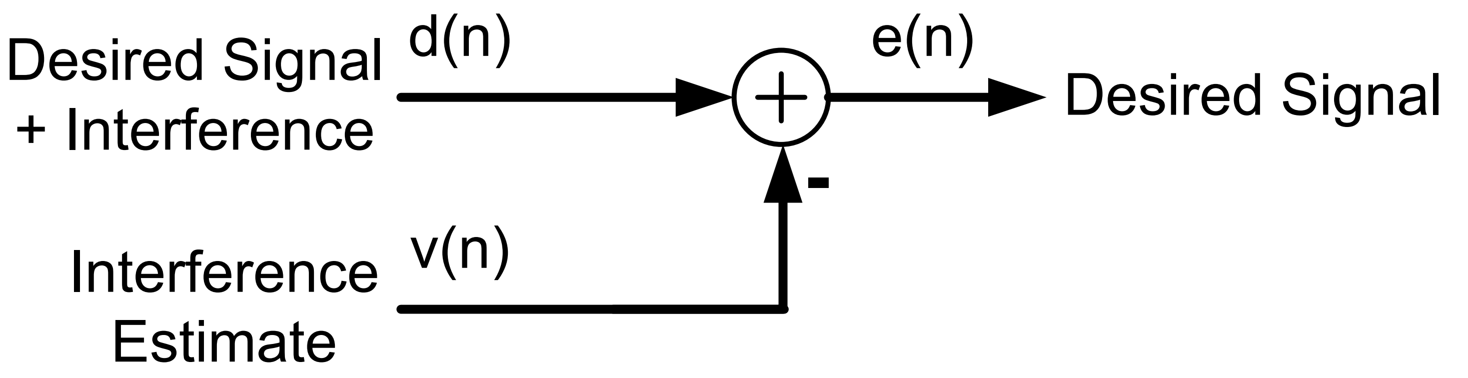
(Baseband processor)

The Basic Idea

Subtract interference

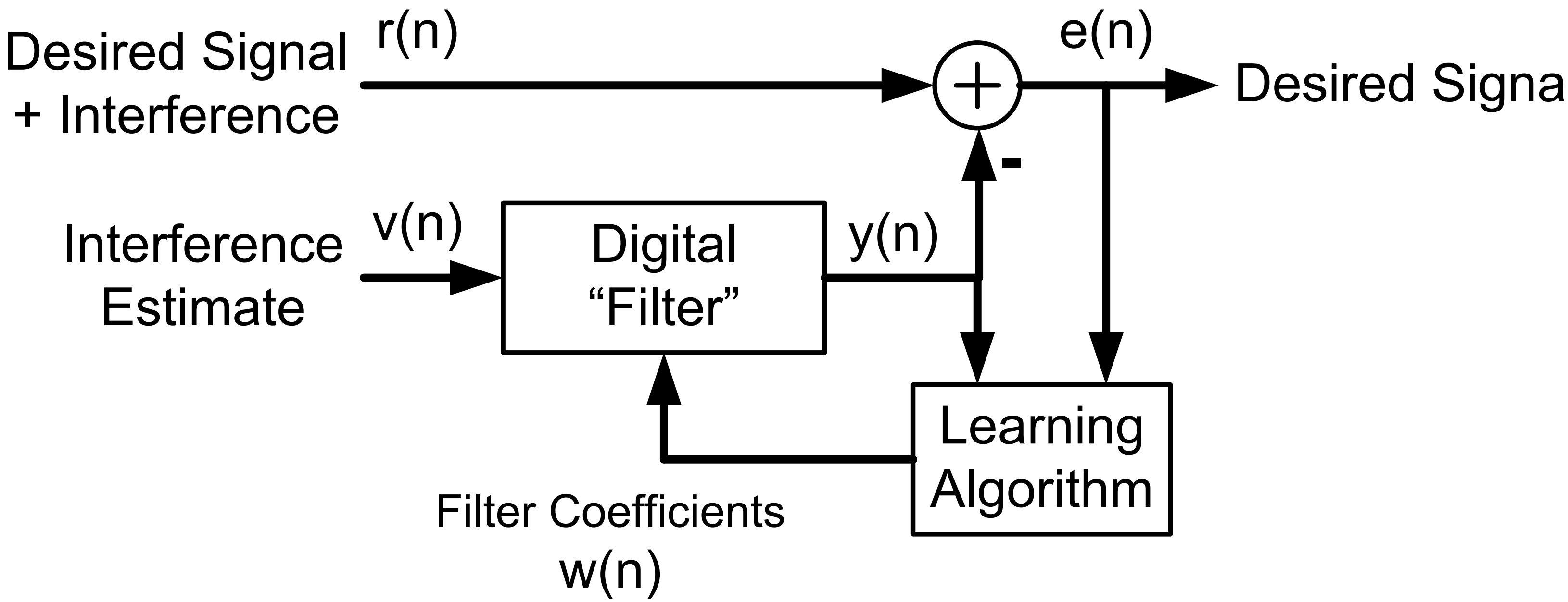
(residual harmonic image responses)

from received signal.



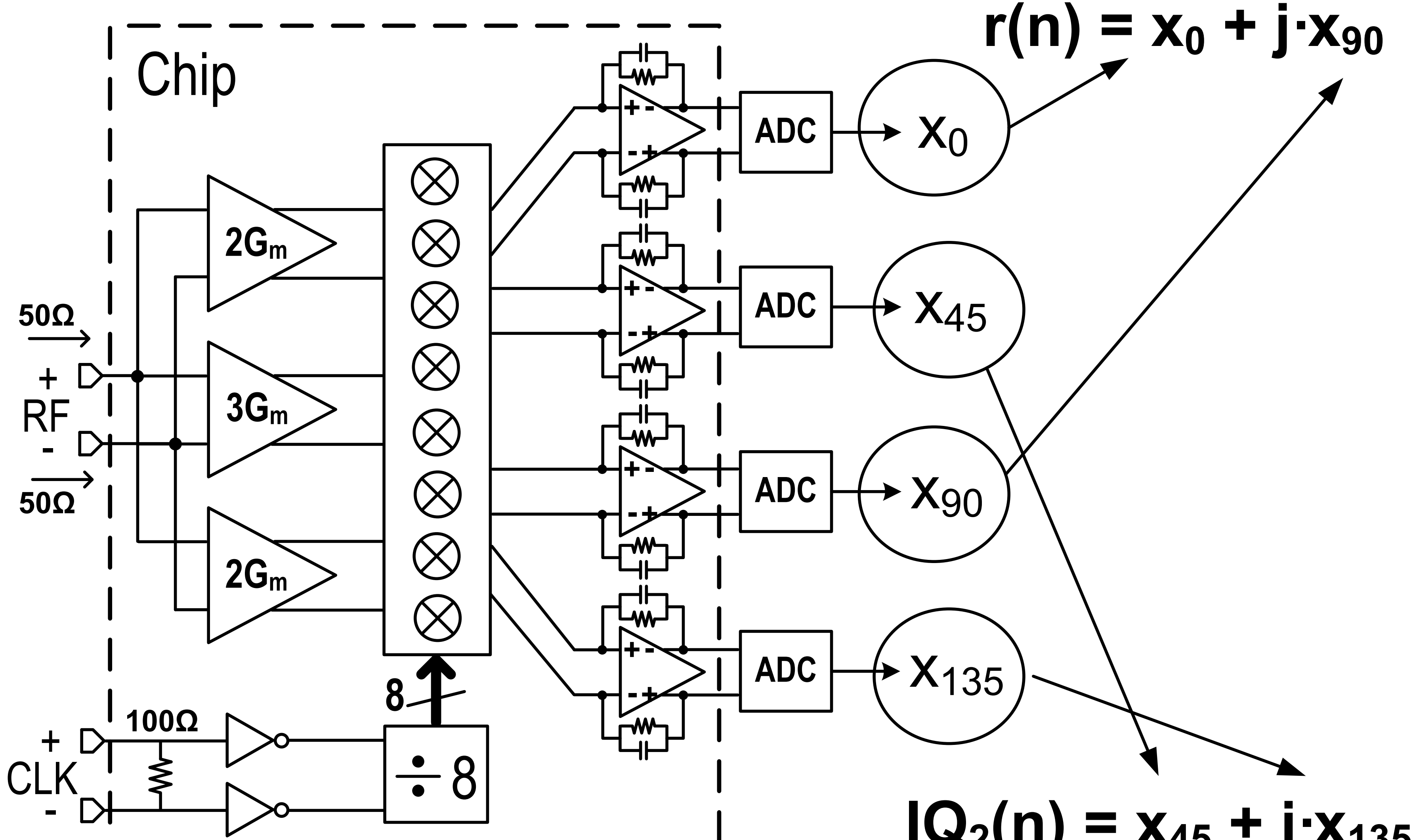
- **Need *interference estimate signal*.**

Adaptive Interference Cancelling (AIC)

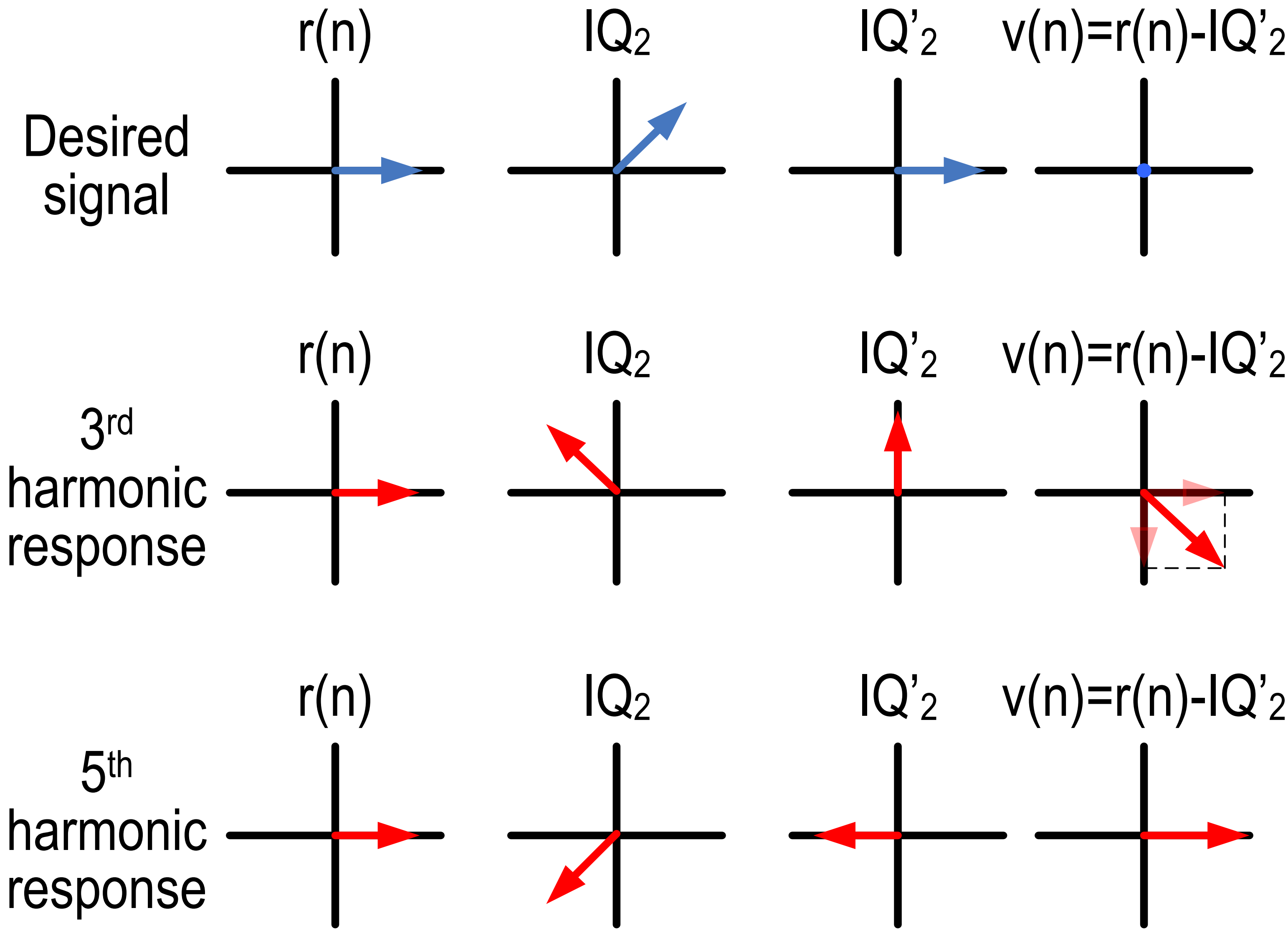


- Adaptive “filter” aligns phase & amplitude.
- Minimizes cross-correlation v(n) and e(n).

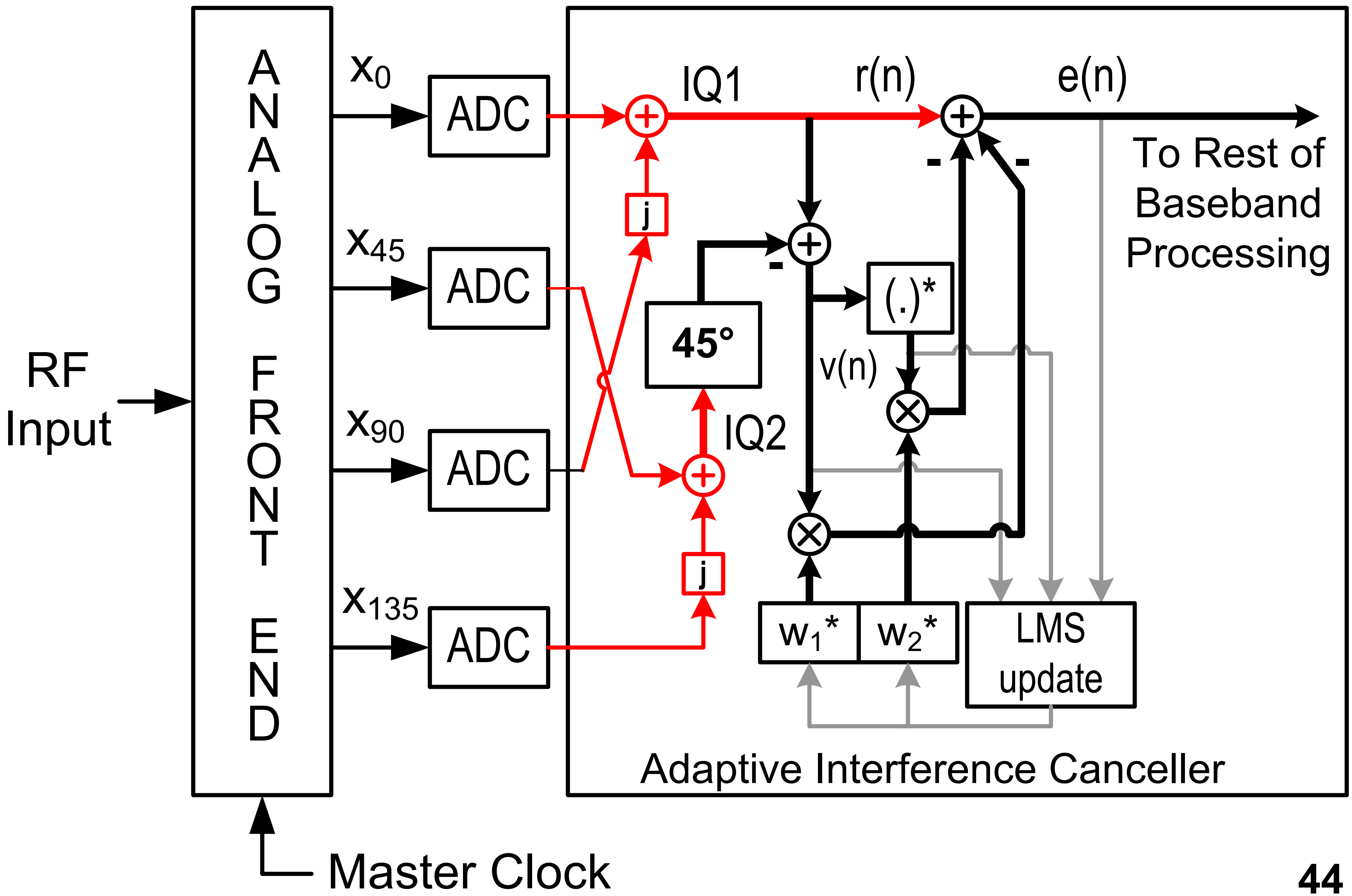
Two I/Q signals



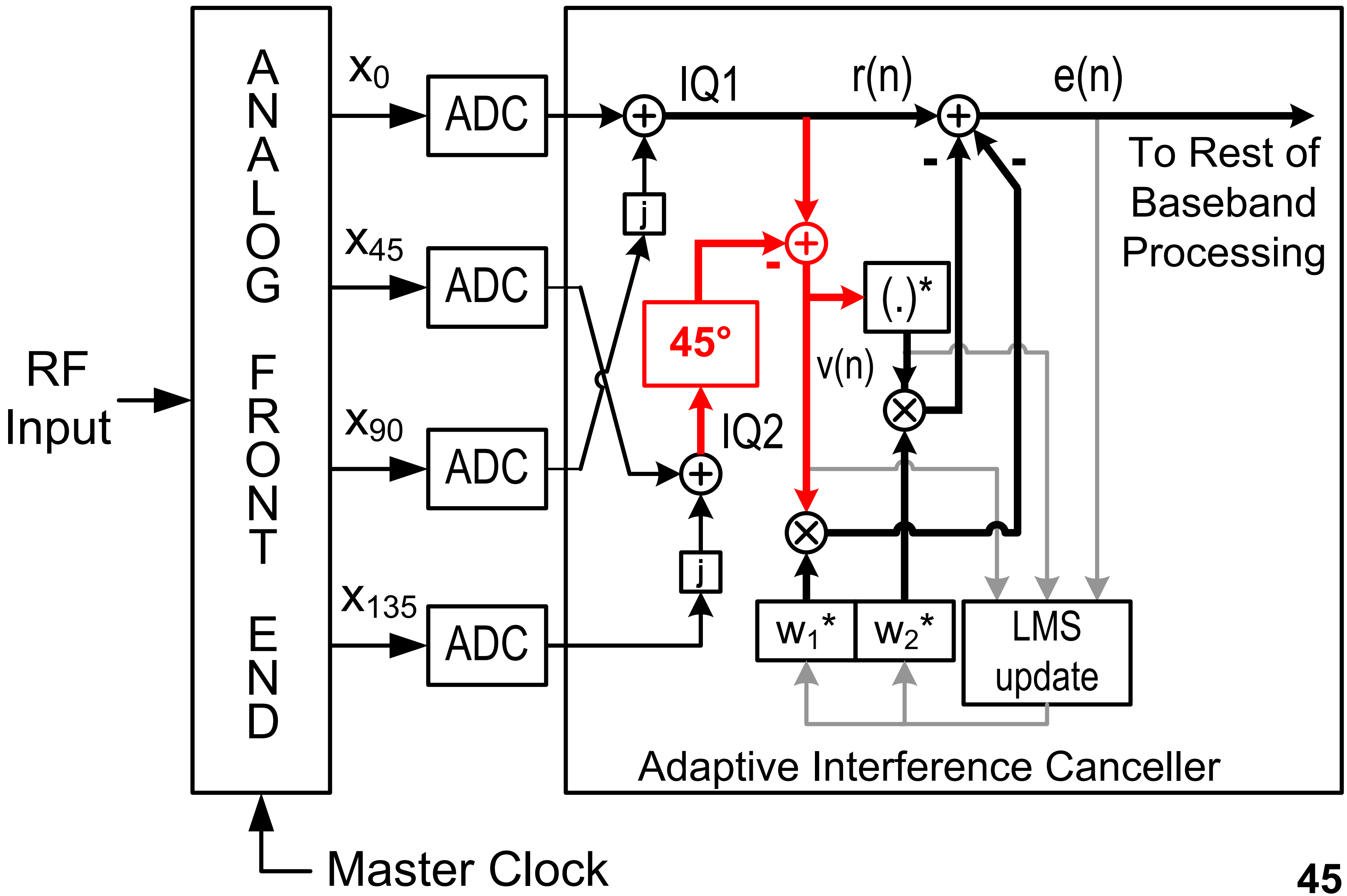
Interference estimate



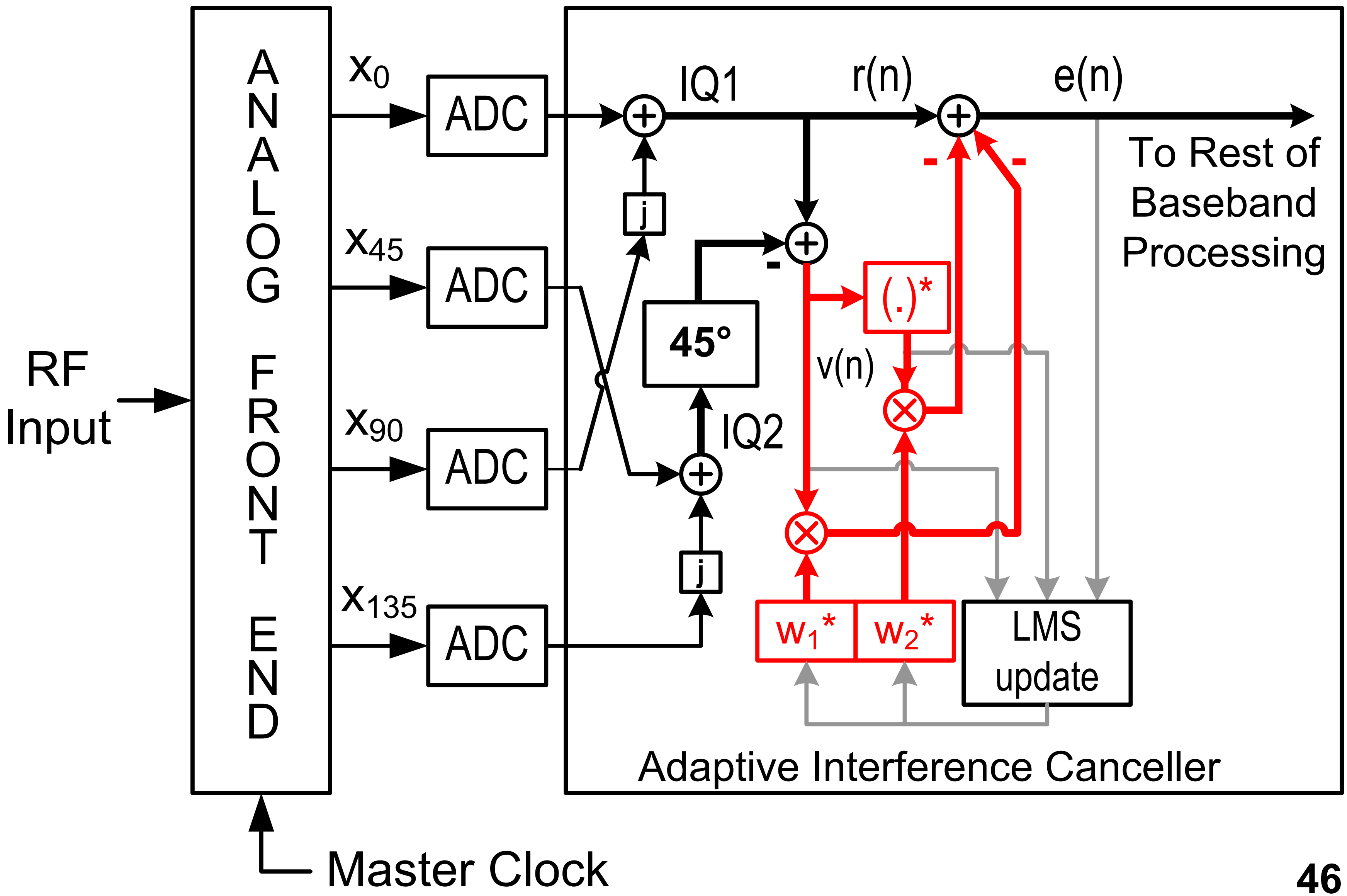
AIC Algorithm 1/5



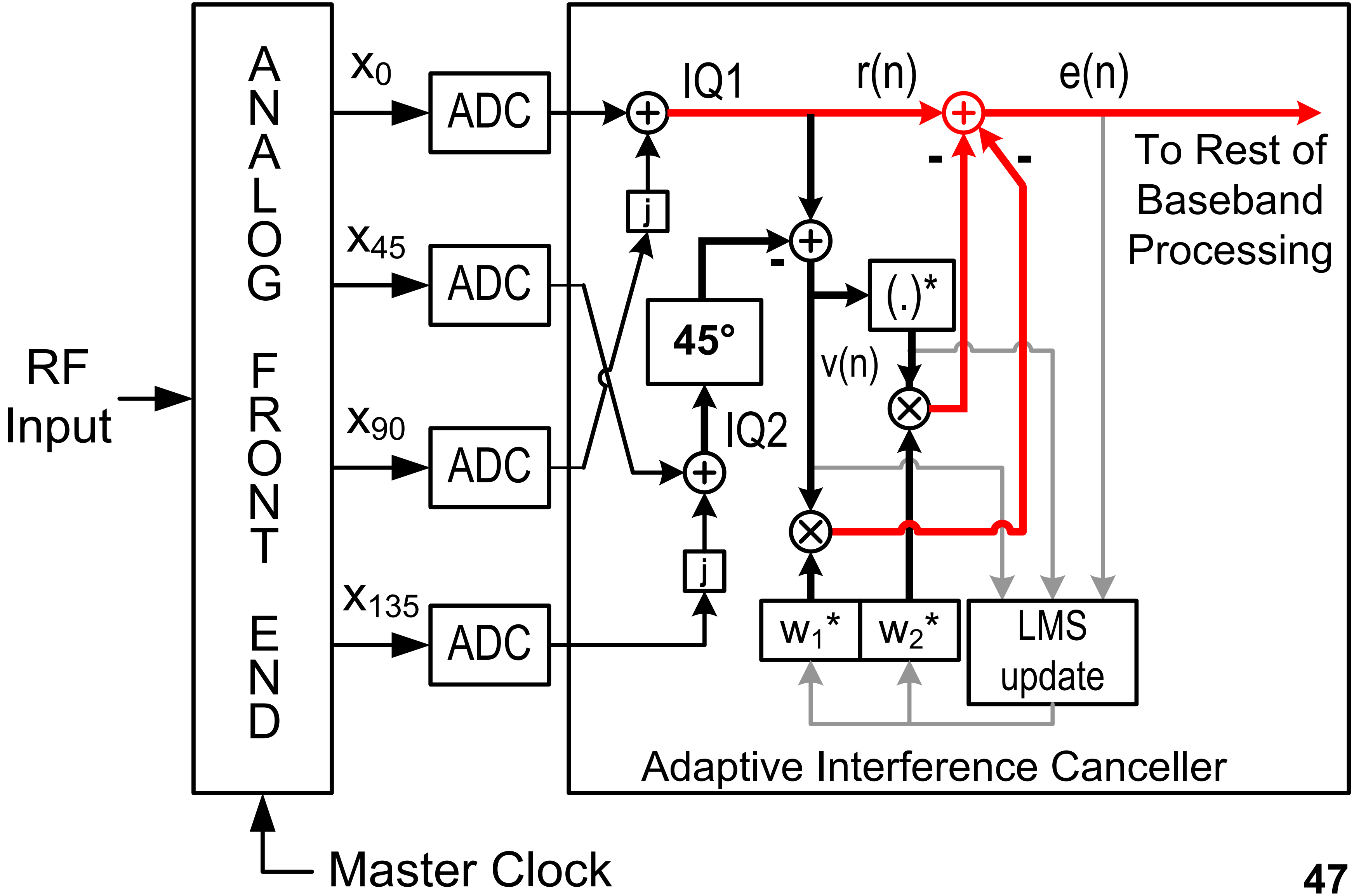
AIC Algorithm 2/5



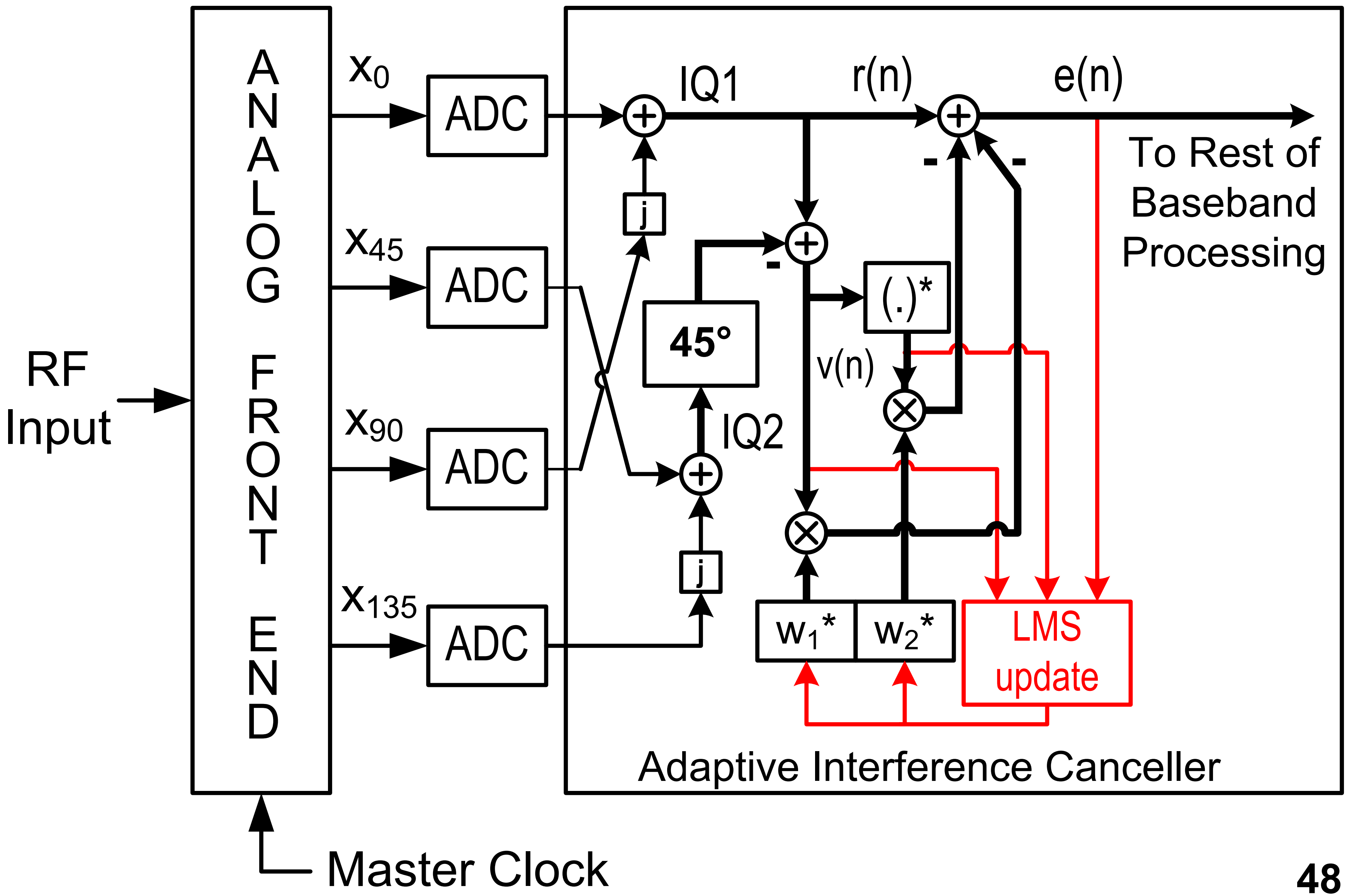
AIC Algorithm 3/5



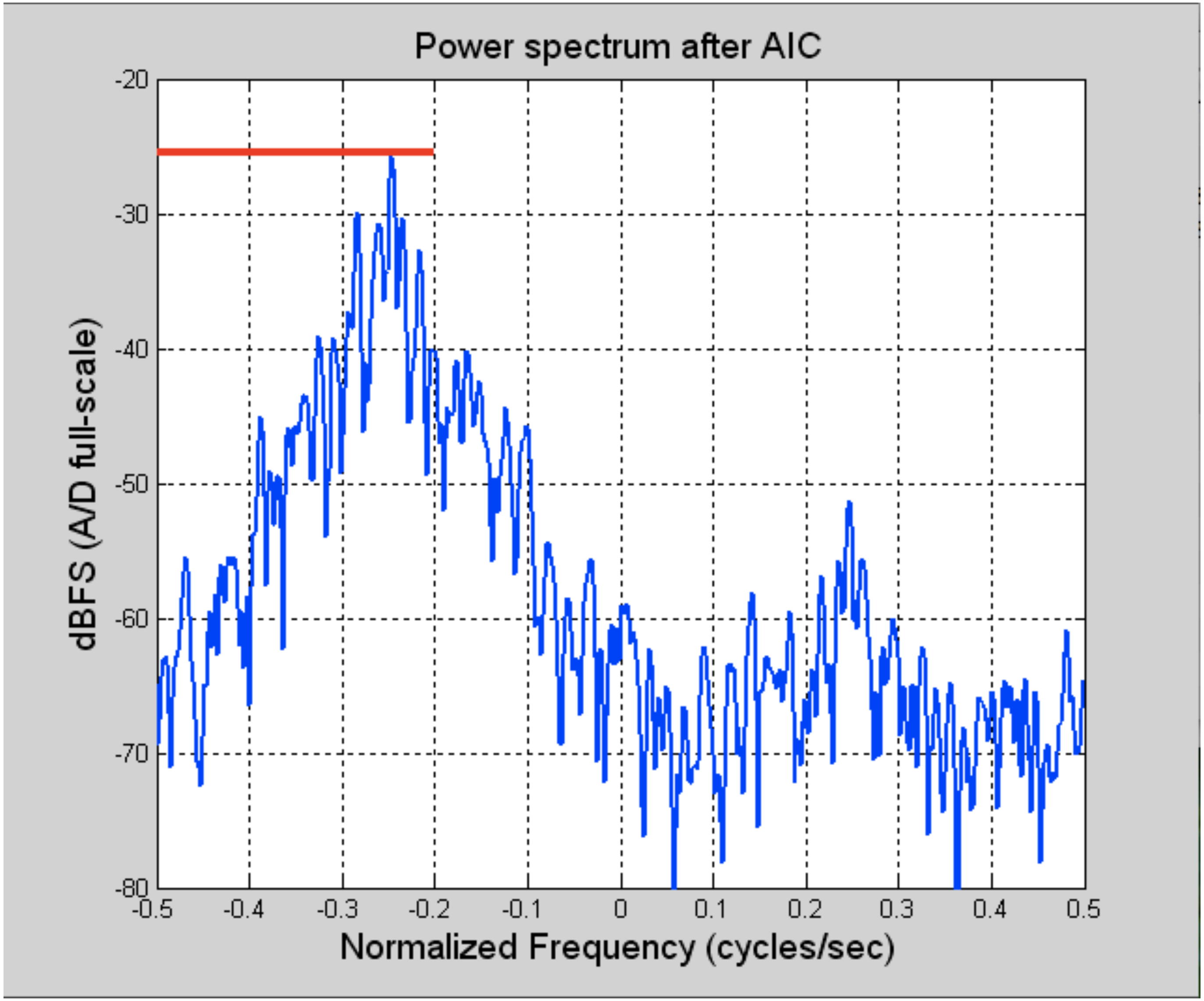
AIC Algorithm 4/5



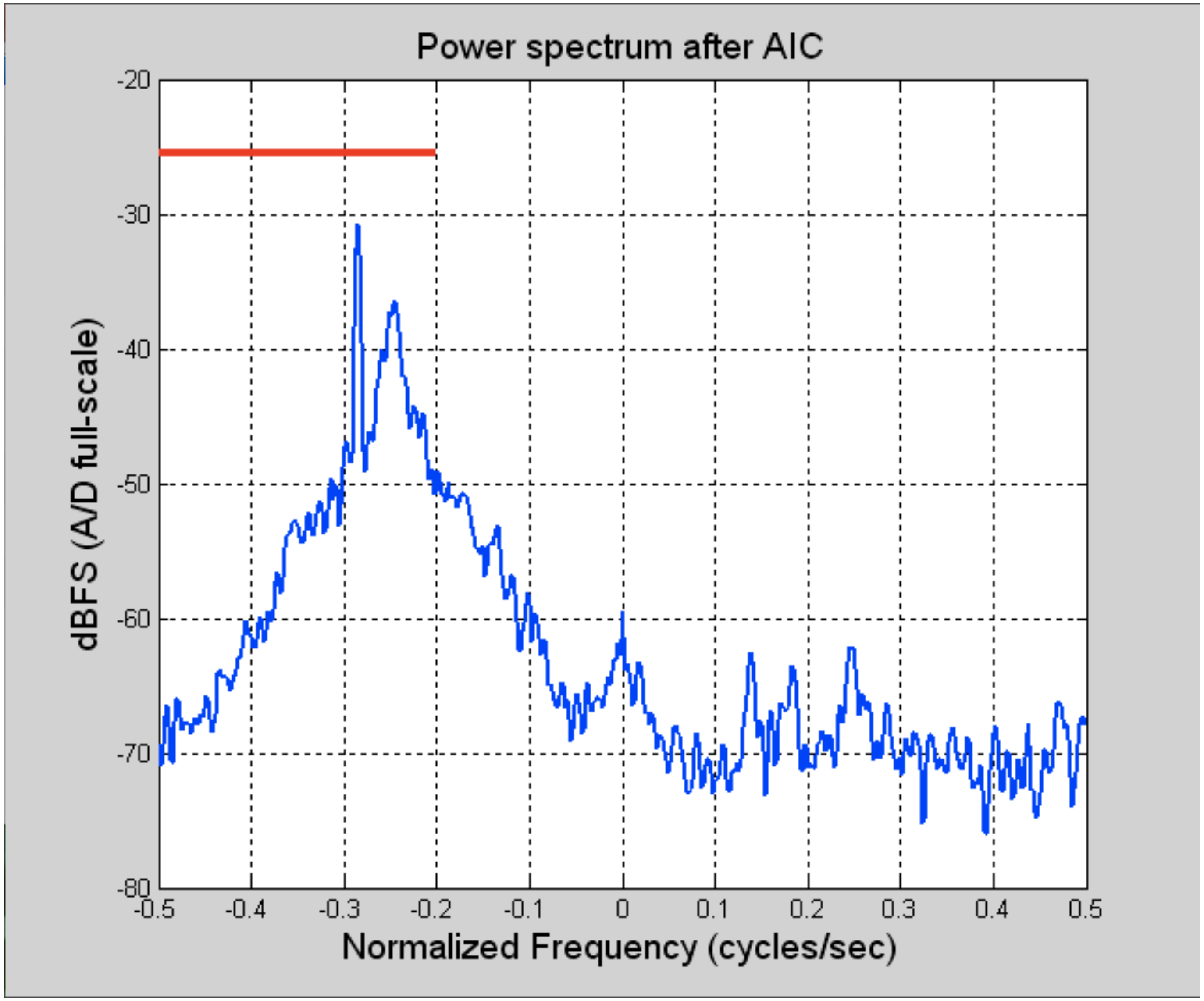
AIC Algorithm 5/5



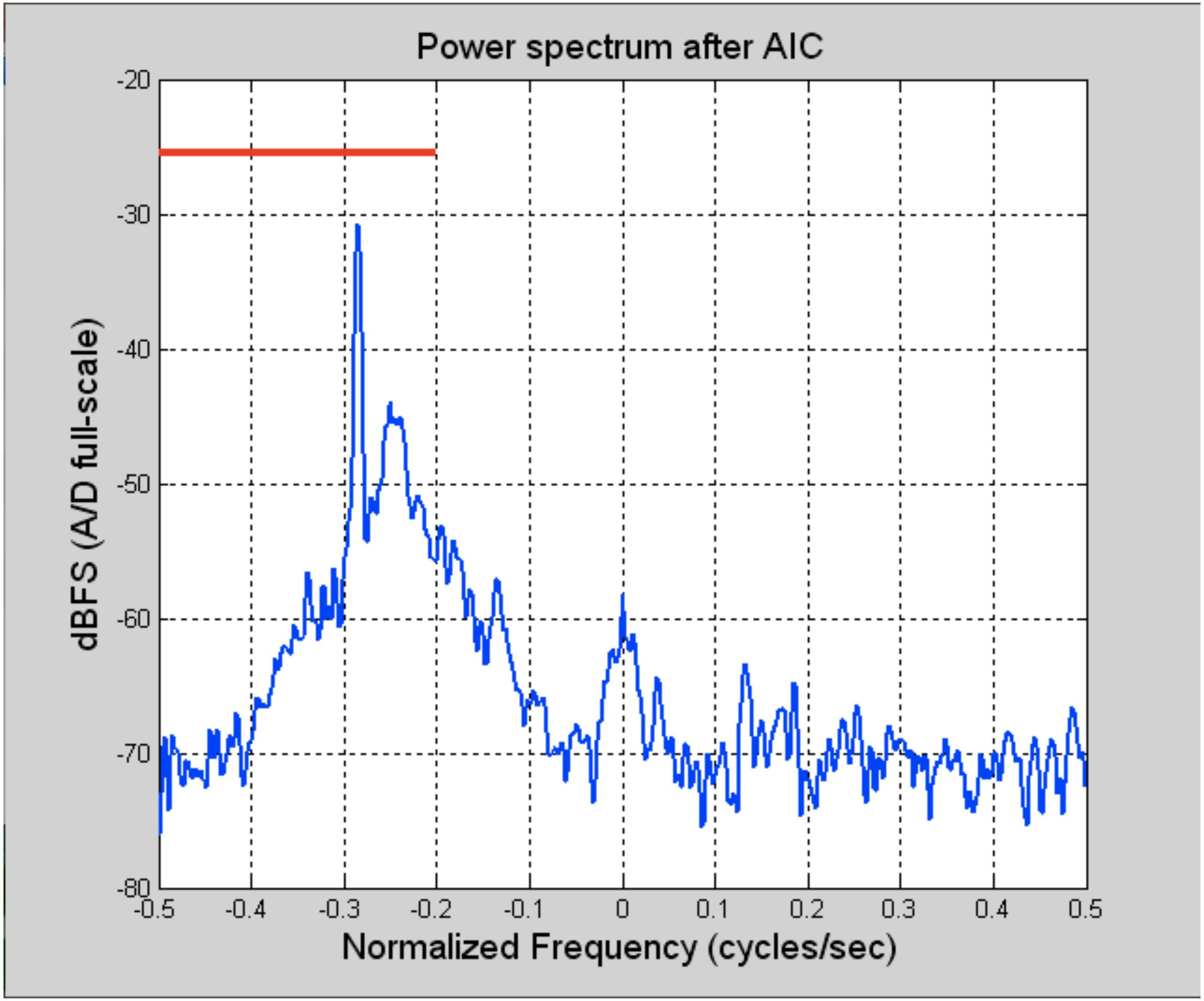
Demonstration



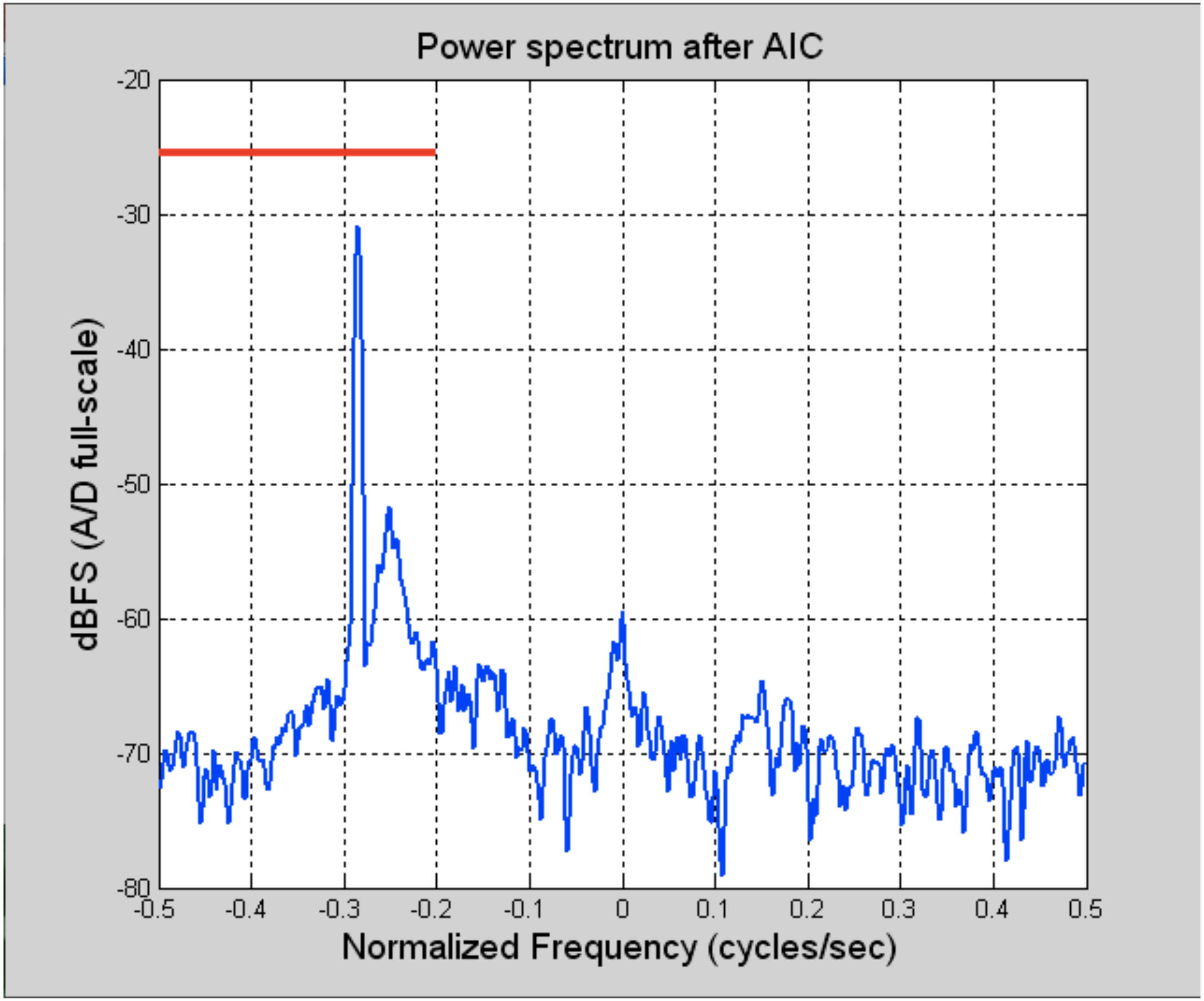
Demonstration



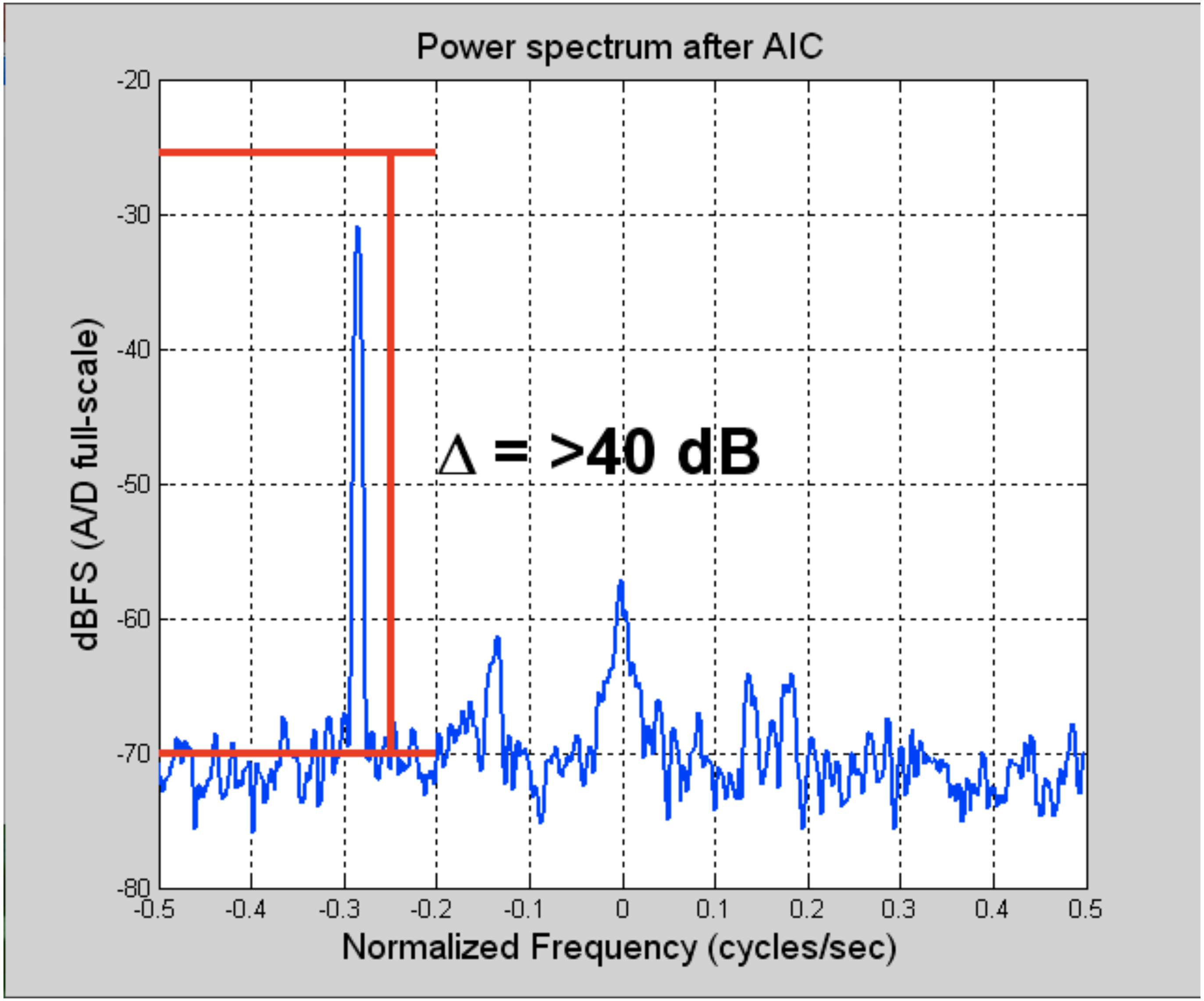
Demonstration



Demonstration



Demonstration



Comparison

	This work	Z. Ru ISSCC 2009 12.8
Rej. strongest	**>80 dB** (1)	>60 dB
Rej. other odd	>36 dB	>60 dB
Rej. even	>64 dB	>62 dB
Power frontend	45 mA @ 1.2 V (excl. ADCs)	50 mA @ 1.2 V (excl. ADCs)
Power DSP (100 Msps)	<8.5 mA @ 1.2 V (simulated)	N/A
# ADCs	4 / 2 if AIC off	2

(1) If one harmonic interference image band is dominating.

Adaptive Interference Cancellation: Conclusions

Dual-domain Harmonic Rejection Mixer (HRM) proposed:

- Analog HRM + 4 ADCs + Digital AIC.
- Strongest correlating harmonic image is removed
- X-correlation -> independent of signal shape.
- Stronger interferer -> more rejection

- Measurements:
  - First stage (analog) HR > 36 dB.
  - Dual domain HR3 or HR5 > 80 dB.
  - Limitation: even-order HR > 64 dB.

Outline

- Introduction
- Balun-LNA-Mixer (BLIXER)
- Interferer robust SDR RX – analog part
- Interferer robust SDR RX – digital part
- **Summary**

Summary

- BLIXER
  - Noise cancelling
  - no voltage gain @ RF
- Interferer robust RX
  - No voltage gain @ RF
  - Filter before voltage gain
  - HR: error of errors

Summary

- Digital Harmonic Rejection RX
  - Adaptively kills the biggest harmonic interferer