Sep. 14 '06 SSCS Kansai

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– Trend of Advanced SiP –
–Technology Development –

Renesas Technology Corp.
System Solution Business Group
Takafumi Kikuchi

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Contents

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1. Semiconductor Needs for Ubiquitous Network Era

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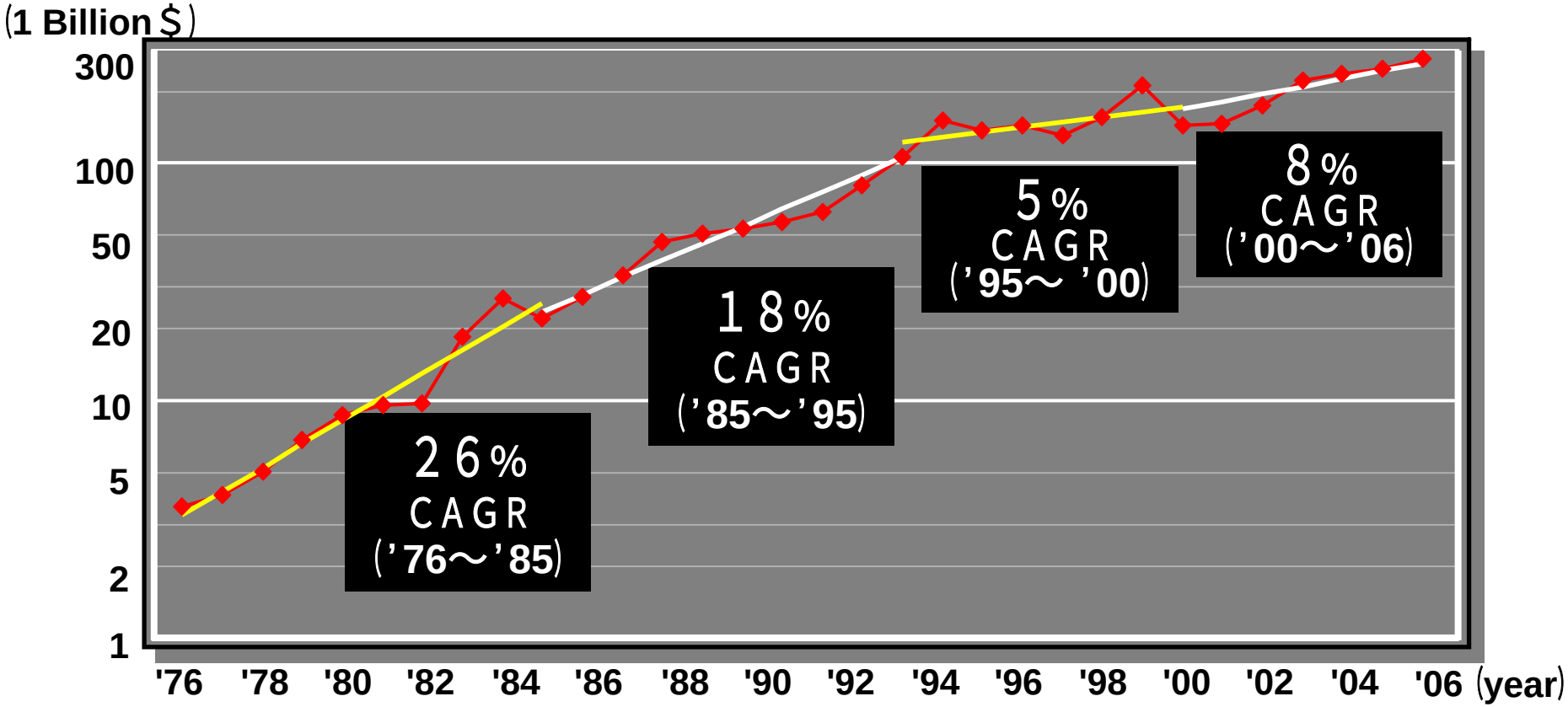
Macro trend of growth rate at Semiconductor Market

The rate of market growth is tend to become slow
Action item is Determination of
“The Next Generation Growth Market” and Resource Concentration



∗CAGR is calculated after it approximates in order to decrease influence to Silicon Cycle.

Ref. :WSTS(2005.10)

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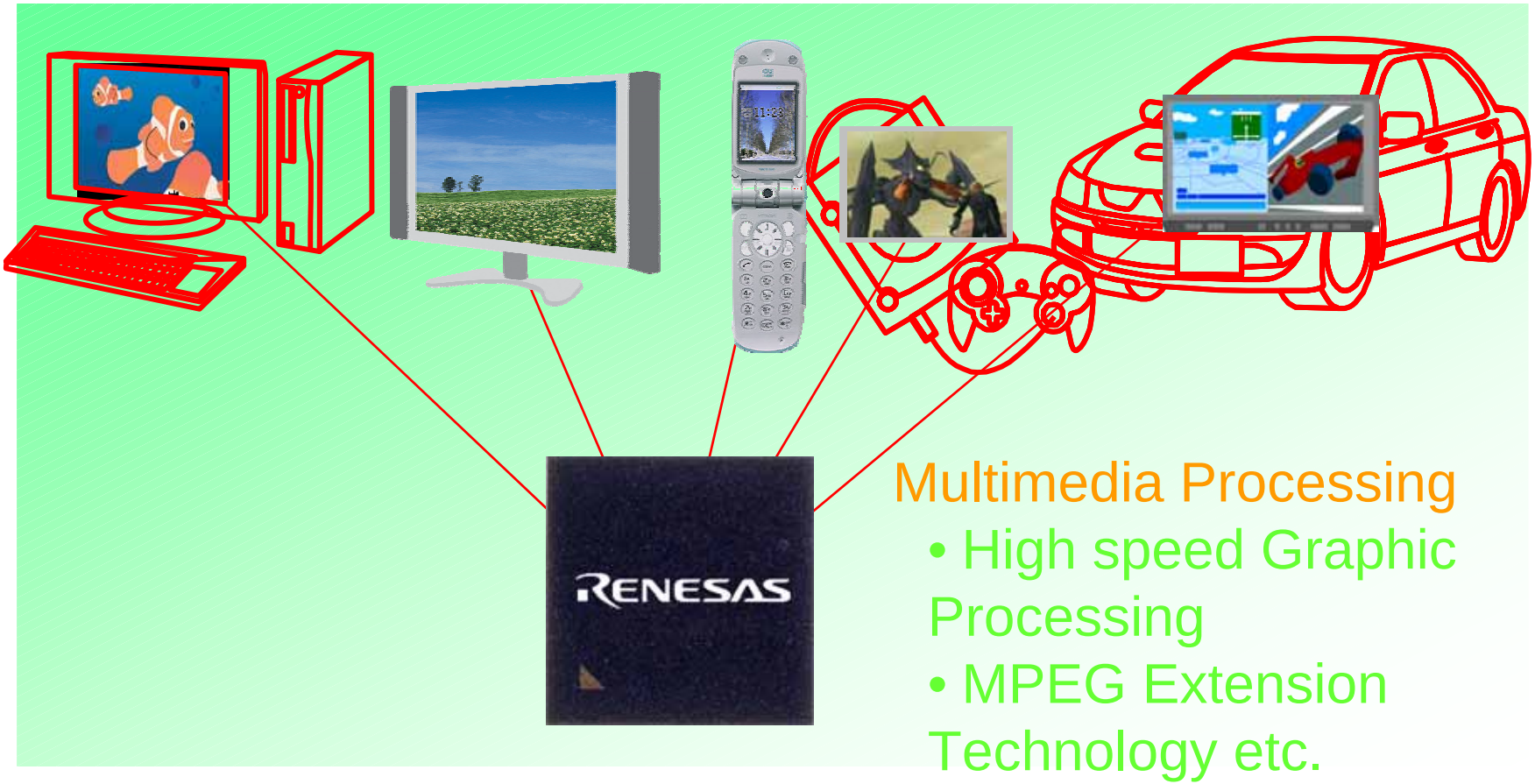
Classification of Application and Convergence

Developing function convergence such as Multimedia Processing and Network. Continuity and development of Excellent Hard IP and Software IP become Important.



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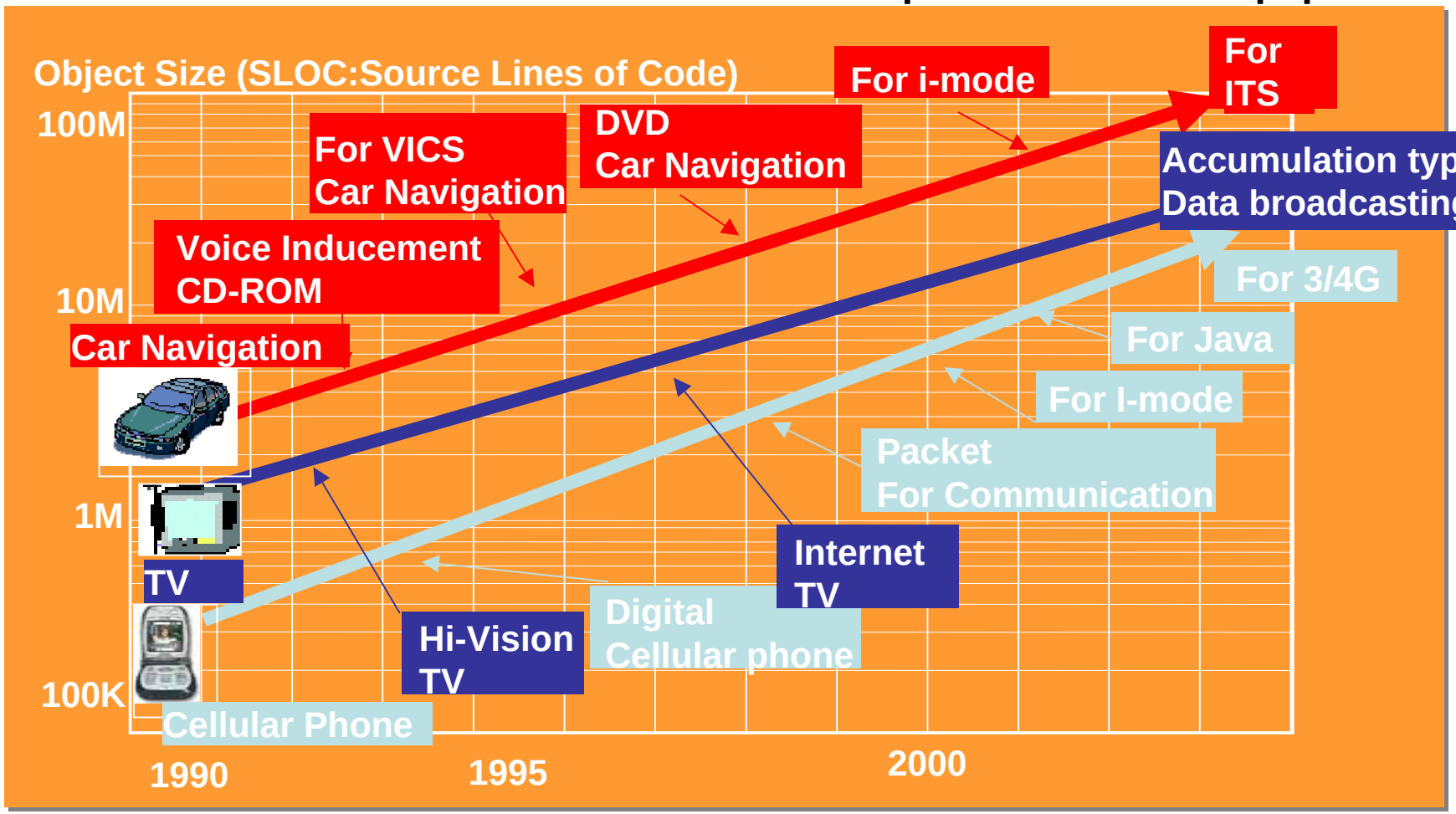
Huge Expansion of Application Software Development

Progressing Expansion of Software Development in Ubiquitous Network Equipment



Source：IPA Information Processing System Society of Japan embedded system research Gr establishment commemoration symposium (July, '05)

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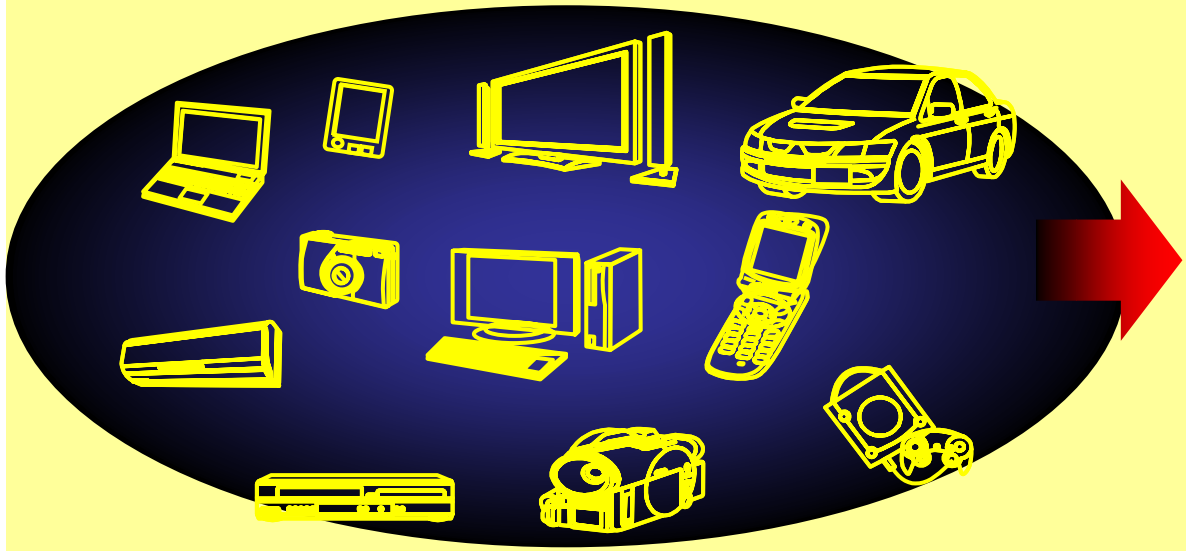
Action item of Semiconductor System Solution

“Diversification”, which is Action item of Ubiquitous Network Equipment Semiconductor is required revenge of “Convergence”, “Development Expansion of Software”, “Short-term Development Cycle”

Ubiquitous Network Device



Device Action item Semiconductor Needs

- For Diversification
- Technology/Device Convergence
- Expansion of Software Development
- Development Cycle Short-Term

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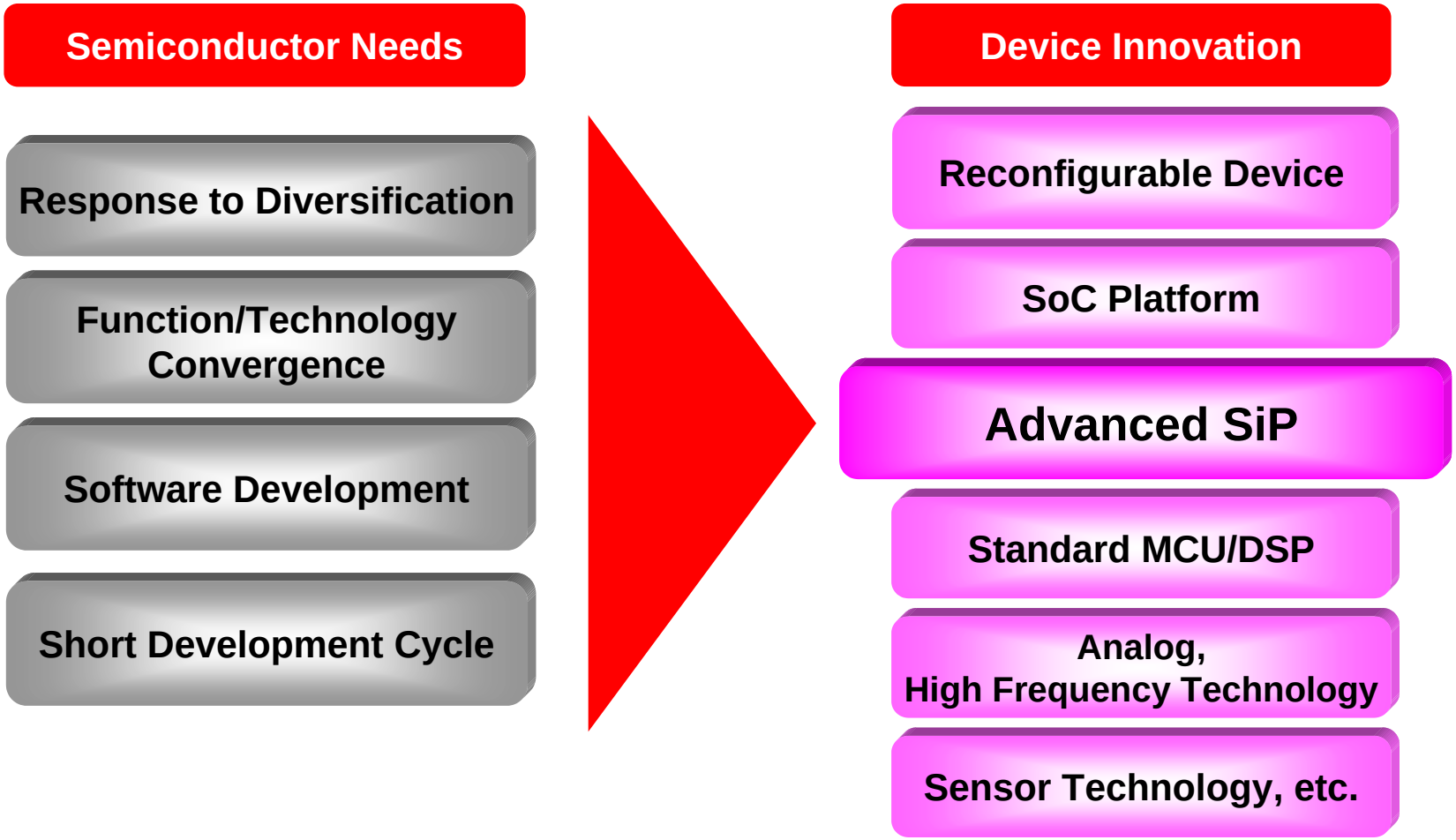
Device Innovation which realizes semiconductor needs in the ubiquitous generation

SoC Platform and Advanced SiP get more important



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2. Approach toward System Solution

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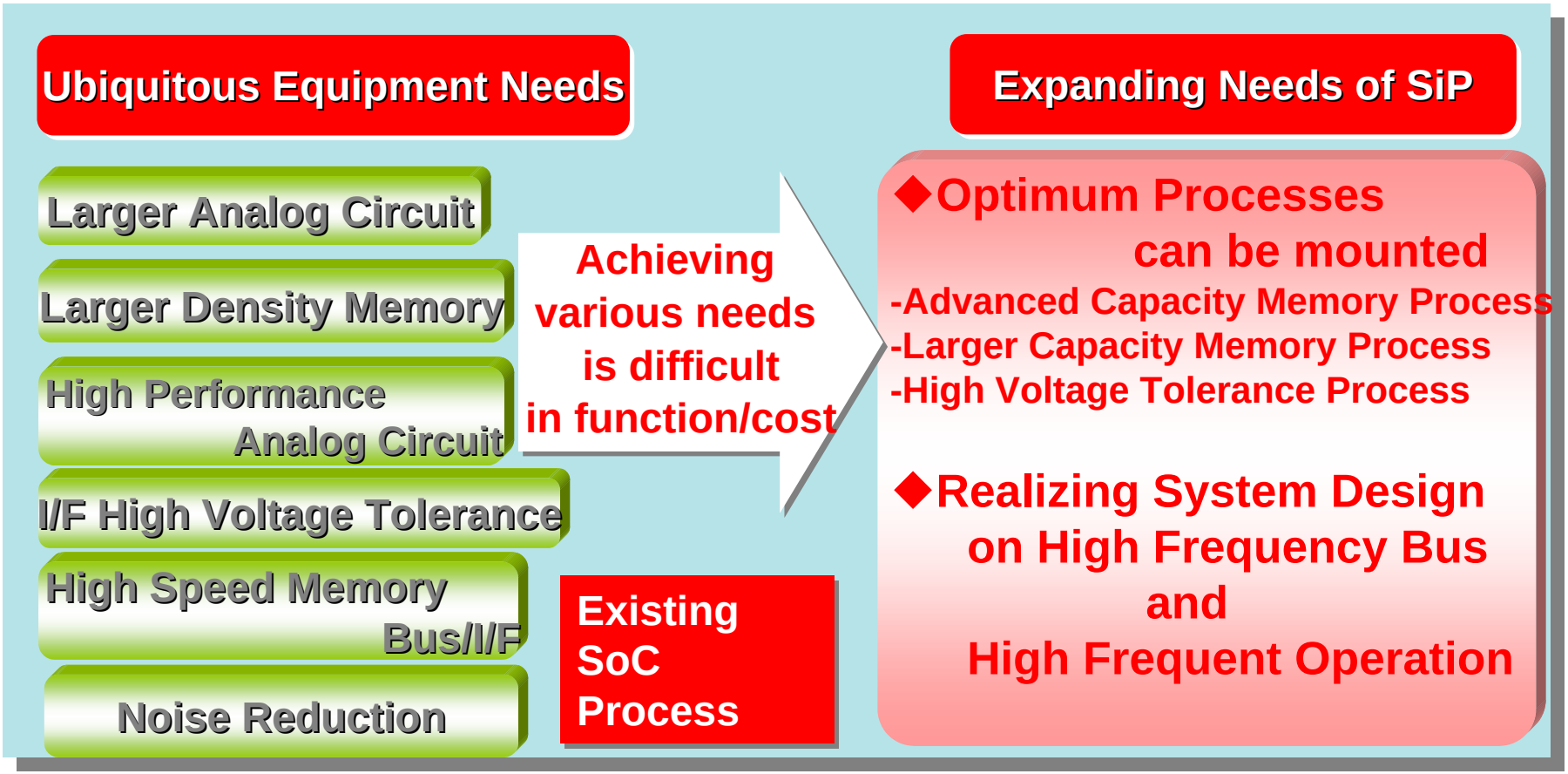
More Difficult Needs for SoC to Realize

- Larger Capacity Memory, High Frequency Bus and High Performance Analog Circuit are Required to Realize Ubiquitous Equipment
- Realize the best solution with SiP to combine High Powered SoC, Mass Memory and Highly Accurate



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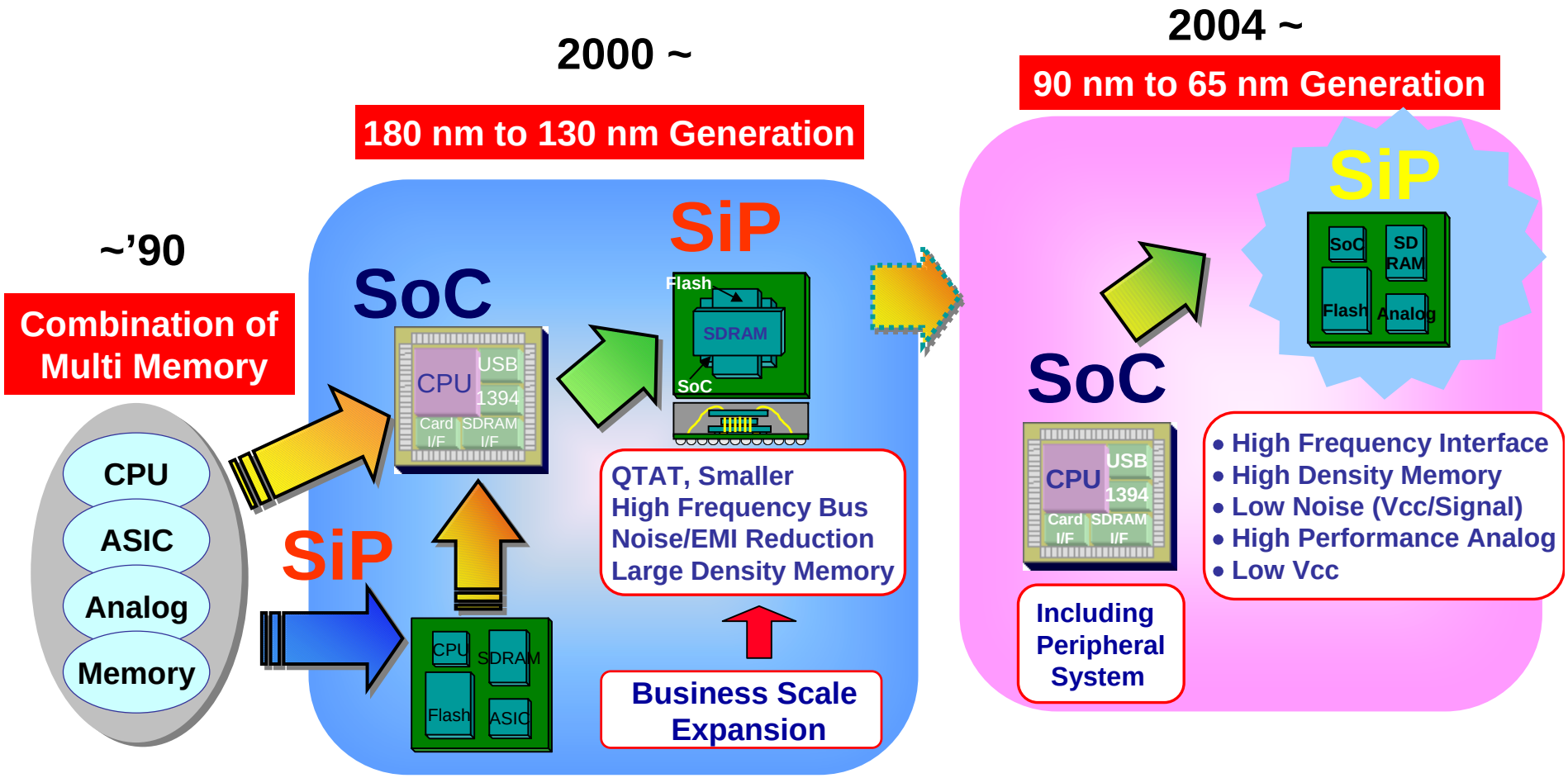
System LSI Business Trend

SiP can drive Maximum Performance for SoC



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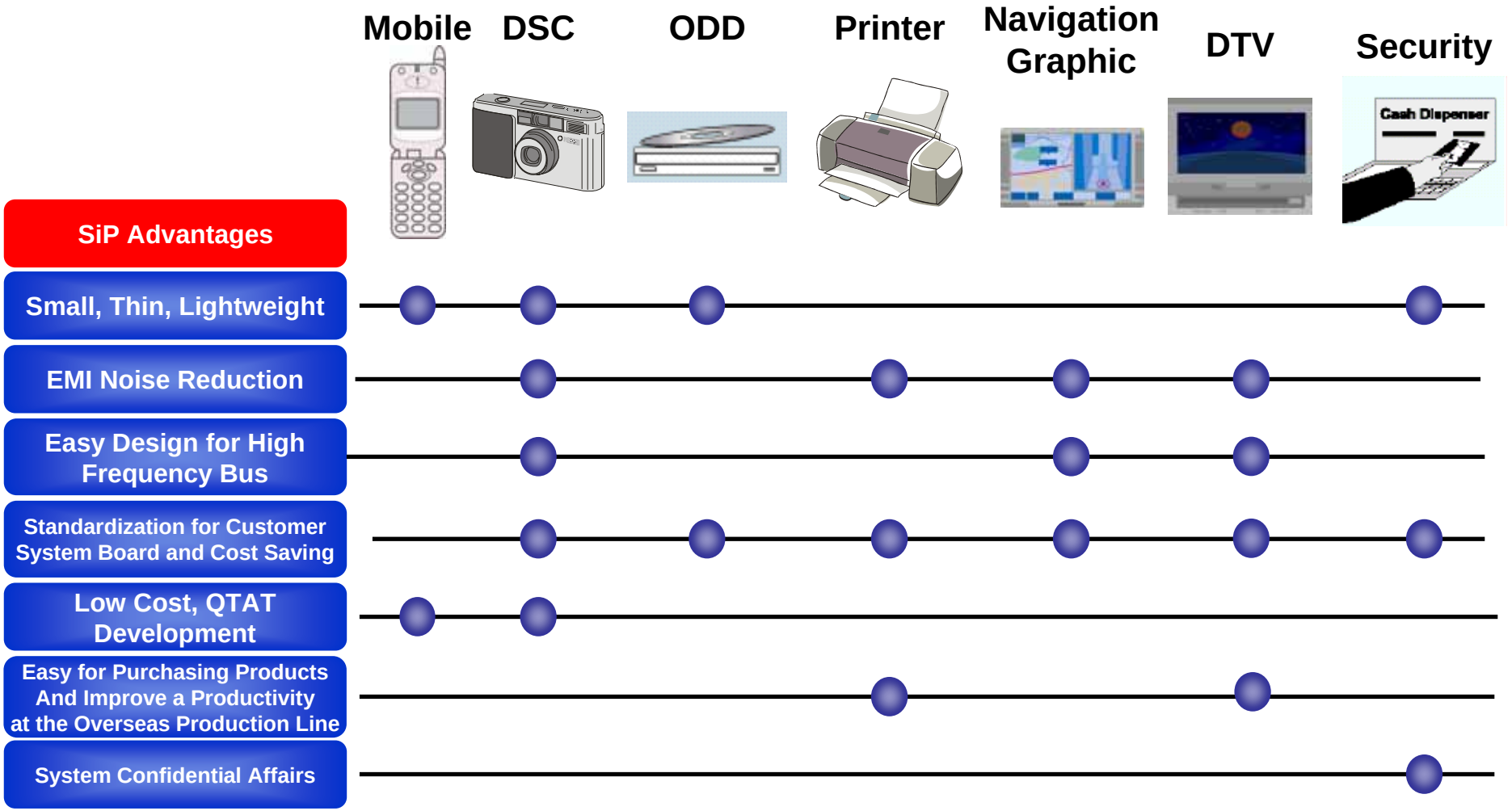
SiP Technology Realizes Various Application Needs

~ SiP Realizes Various Advanced Applications ~



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Advancing SiP Technology to realize Multi Function and High Powered

Request to SiP	Corresponding SiP technology and approach
High-Powered System, Muti Function	High-Speed I/F(DDR), Noise Reduction, Analog
Achievement of Best and Low Cost SiP	Design for SiP (DFS)
Small, Thin, Higher Heatproof inclination	High Density SiP Mounting Technology
Large Capacity, High Speed Memory	KGD*, Multi Bit Bus Memory, Tie-up with Memory Supplier
Remain High reliability as single chip	Optimization of test process

*KGD-Known Good Die

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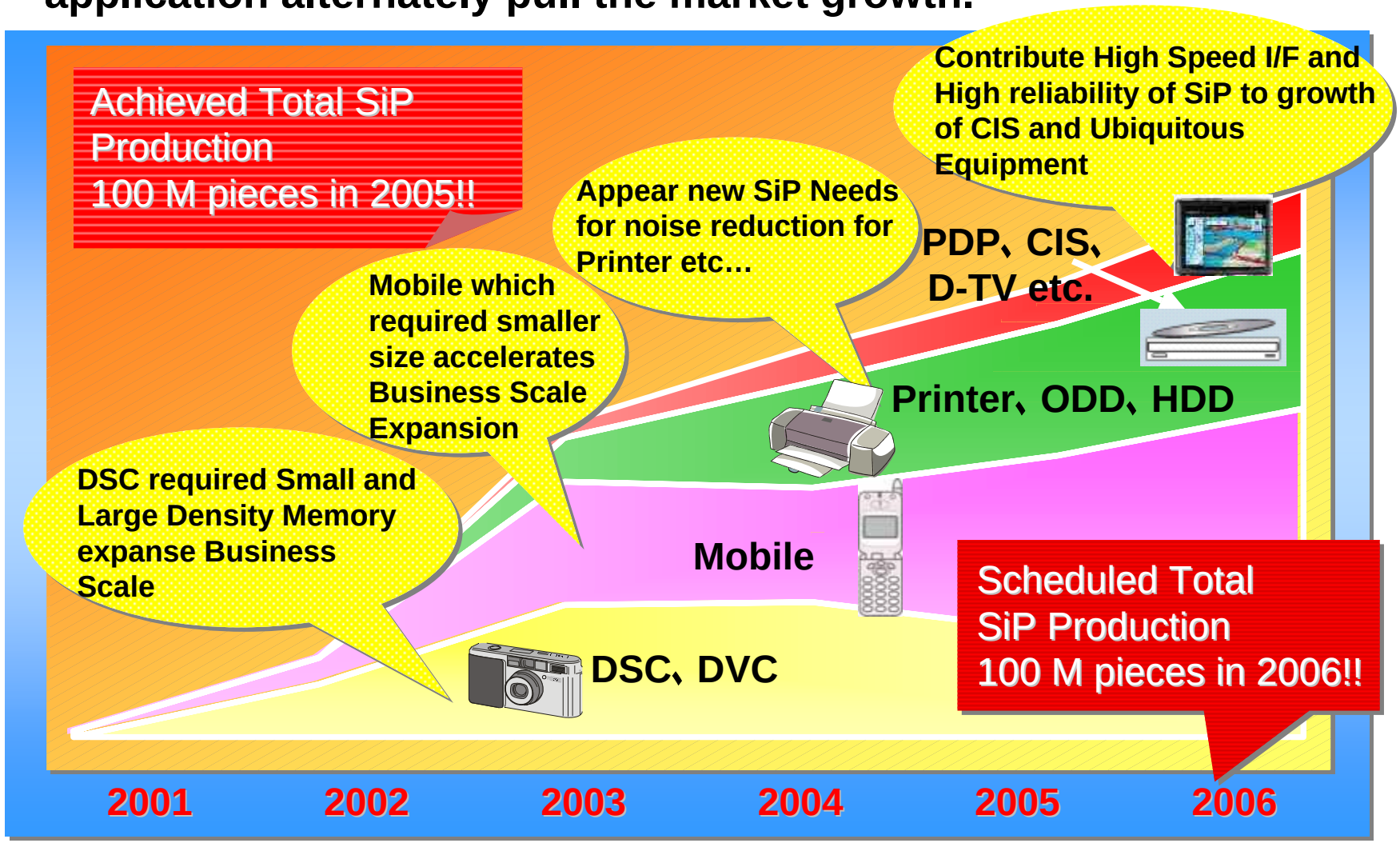
Renesas Leading SiP Market

- Making to high performance and the SiP technology of the application alternately pull the market growth.



Renesas SiP Production Quantity

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5. Renesas SiP Consistent Design System

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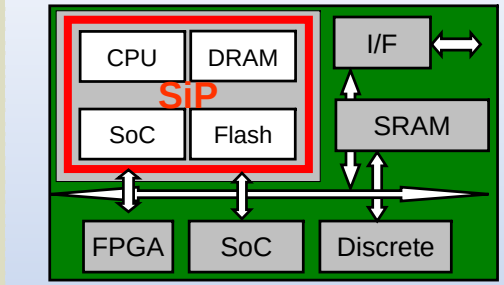
SiP Consistent Design System

- **SiP Test Design**
  - SiP Test Pattern
- **SiP Substrate Design**
  - (1) Reflection, Cross Talk Simultaneous Switching Noise
  - (2) Thermal Register
  - (3) High-frequency Substrate Design
- **SiP Functional Validation**
  - (1) SiP Characteristics
  - (2) Production Reliability etc.

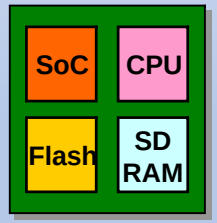
System Design → SiP Spec → SiP Design → Trial/Evaluation → Functional Validation → Mass Production

Total Support from System Design to Test Design



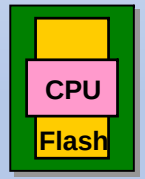
Design For SiP Configuration

Side by Side Type



or

Stacked Type



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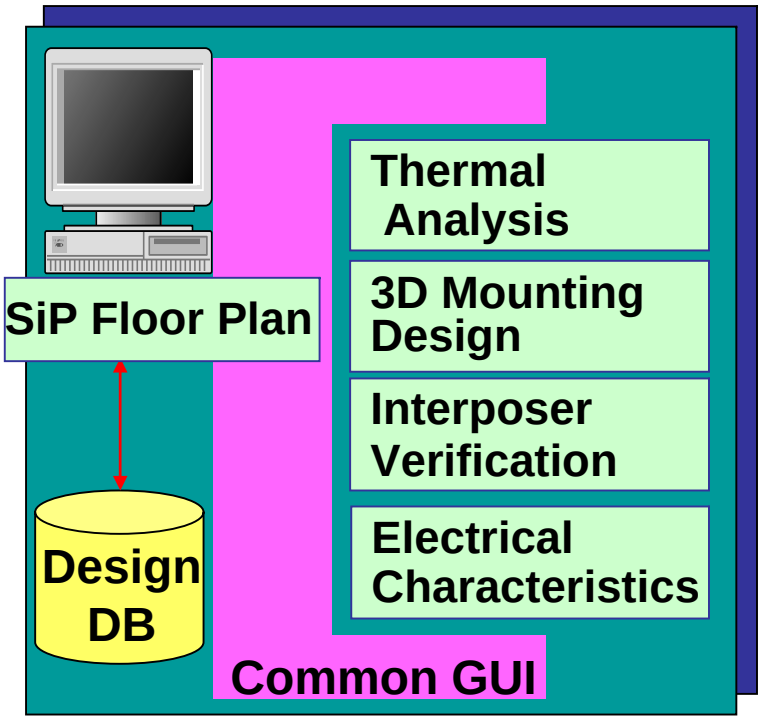
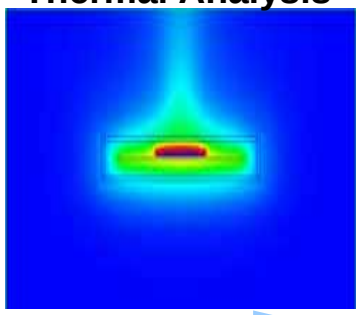
SiP integration design environment

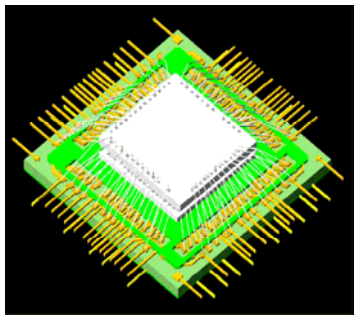
Design Quality Improvement by Electrical Characteristics Check and Verification



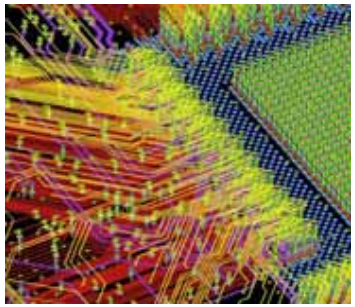
Thermal Analysis



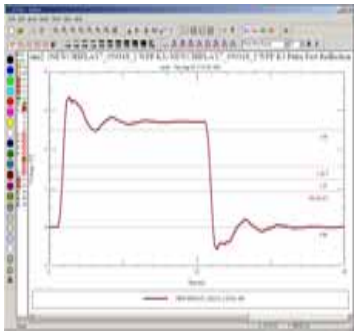
3D Mounting



Interposer Pattern Verification



Electrical Characteristics Check



*ERC：Electrical Rule Check

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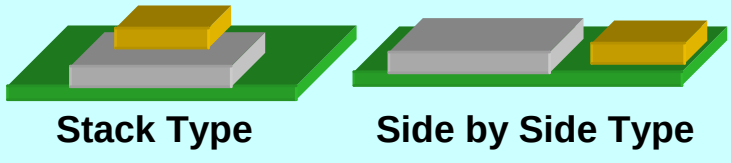
SiP Floor Plan

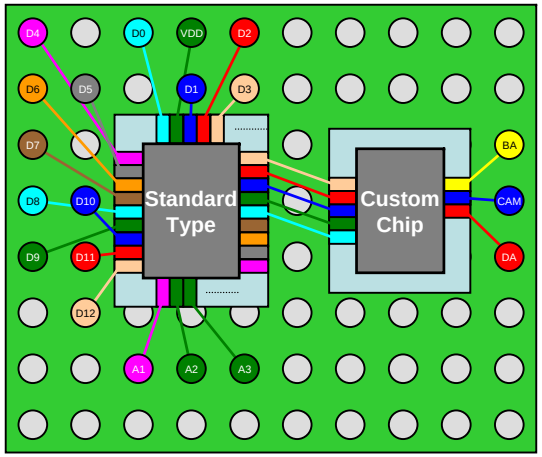
Our Goal:
SiP Design Which Fulfills the Performance, Power, Cost, PKG Size and Pin Numbers

- **SiP Floor Plan**
  1. **Decision on Mounting Type (Stack Type or Side by Side Type)**
  2. **Decision on Chip Alignment with Considerations of Simple Substrate Pattern**

Chip Alignment Inspection

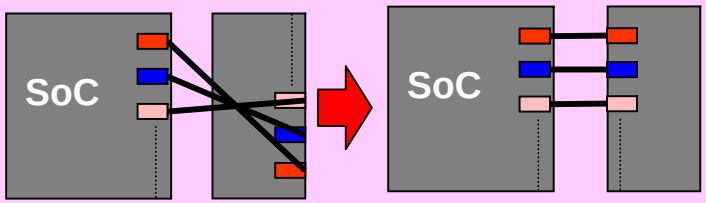


Stack Type **Side by Side Type**

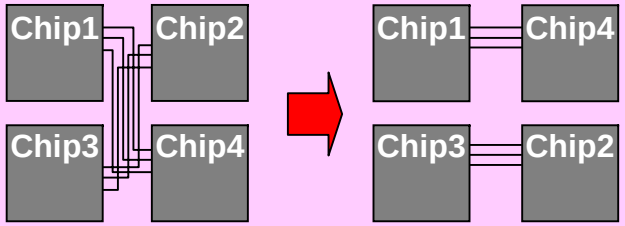


SiP Floor Plan Result

Examination of Simple Substrate Pattern (1)



Examination of Simple Substrate Pattern (2)



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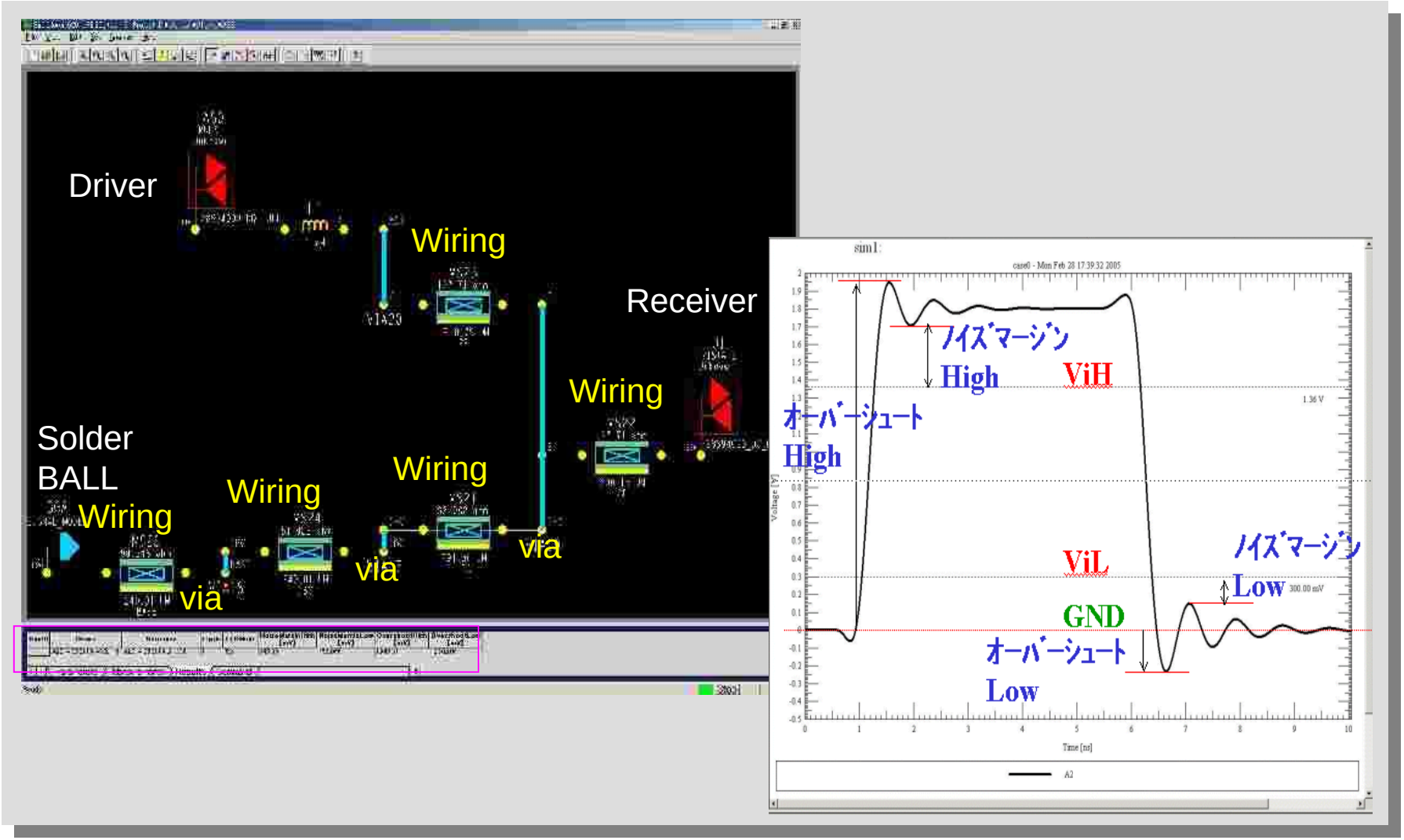
Example of chip interconnection SI analysis result



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IR-drop Analysis Enhancing Technique Examination for SiP

Achievement means

Making Macro Model From Non-Attention Chip
(RLCG+Equivalent circuit by current)

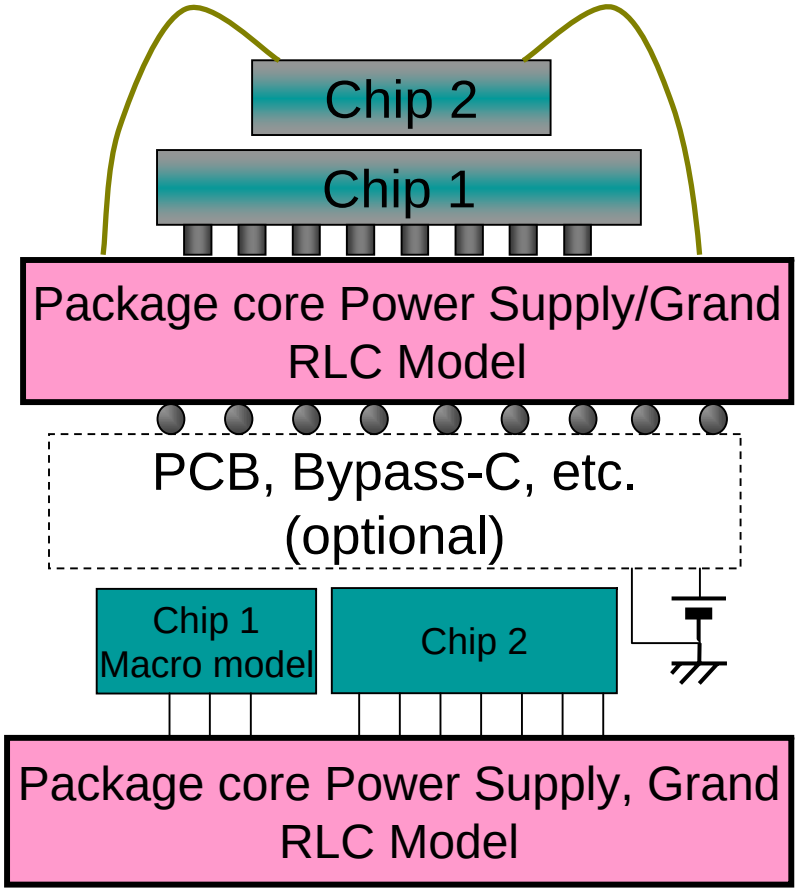
Action Item

Chip Power Supply・Means of Making
GND of Macro Model
Chip Power Supply・Analyzing Means of including
GND of Macro Model

Effect

Grasp achievement of chip interconnection noise spread for which Interposer is used

Reduction in power supply and number of GND balls in SiP PKG



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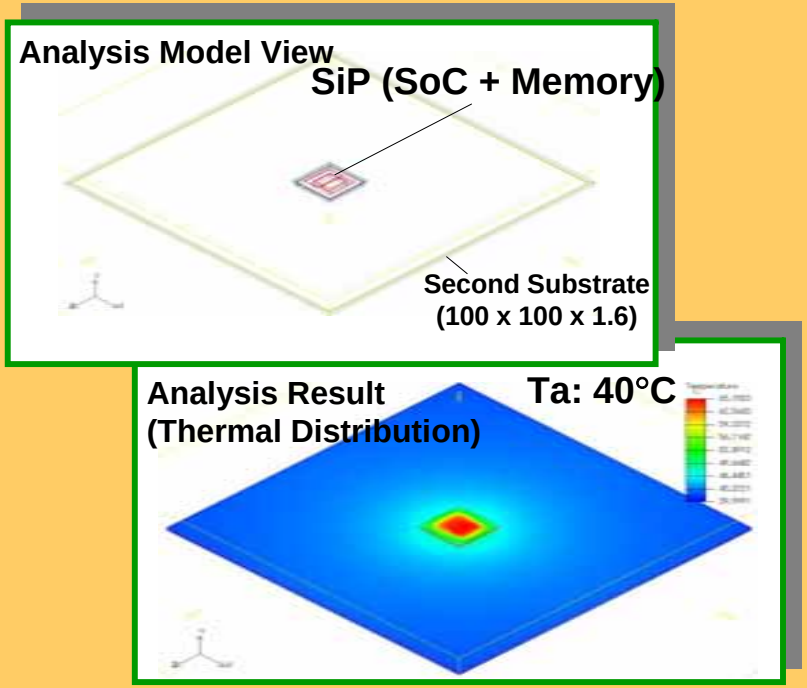
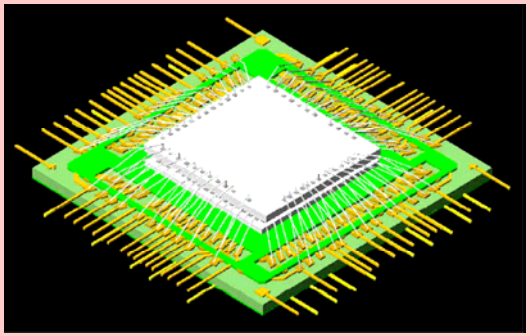
SiP Simulation Cases

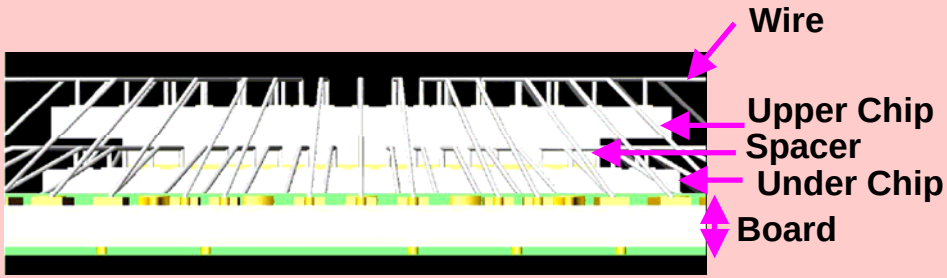
• Thermal Analysis Simulation



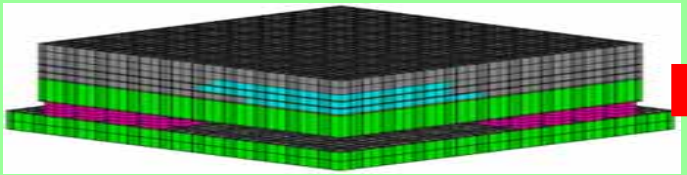
• 3D Wire Bonding Design and Verification



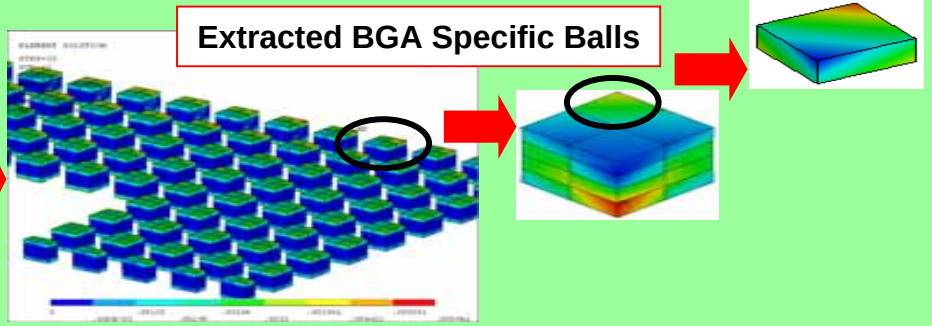
Verification Wire Clearance by 3D Model



• Evaluation of SiP Stress Simulation



SiP Simulation Model



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6. Design for SiP

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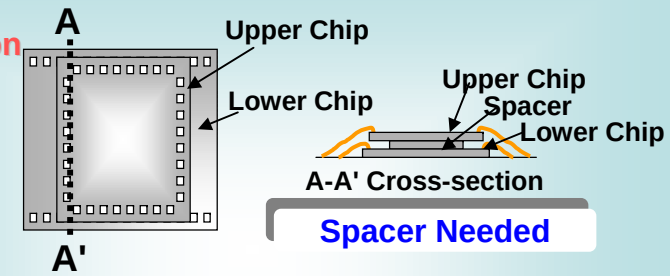
SoC design to consider SiP (Design For SiP)

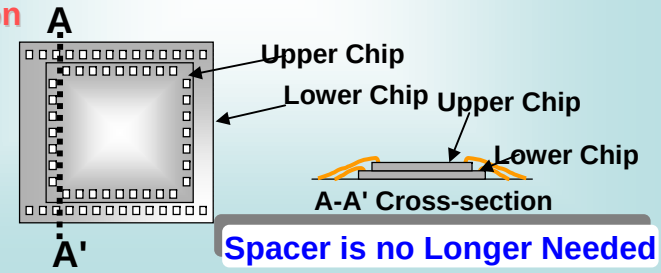
- Realize Suitable SiP Structure ⇒ Consideration cost for SiP Design Technology -

[1] Optimization of Chip Configuration

Before Optimization



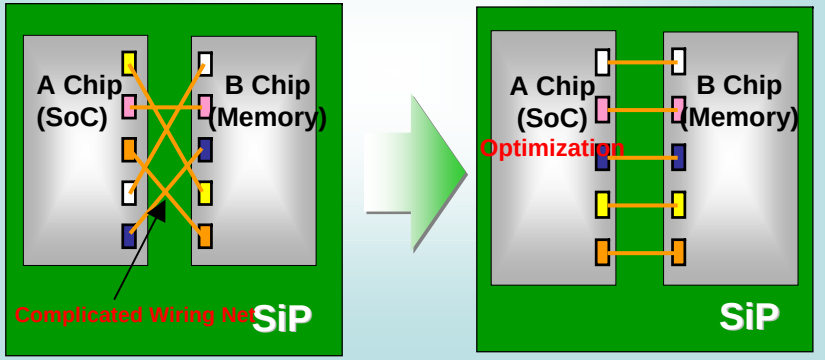
After Optimization



[2] Optimization of I/O Pad Arrangement

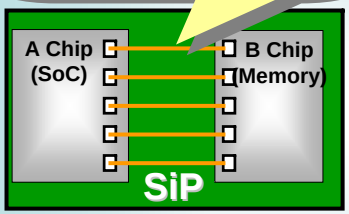
Before Optimization
Many SiP Substrate Layers
More Layers, Must use B/U Substrate

After Optimization
Less SiP Substrate Layers
4 or Less Layers,
Able to use Glass Epoxy



[3] Optimization of I/O Buffer Drivability

Wiring on the Substrate
Long/Short Wire
⇒ Less Parasitic Components



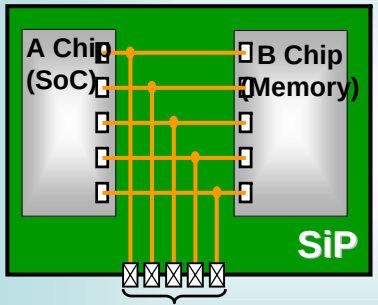
Increase Noise
Difficulty with SI Management

Effect
- Lower I/O Electric Power
- Reduce Simultaneous Switching Noise

Better SI Management by Optimizing Buffer Drivability

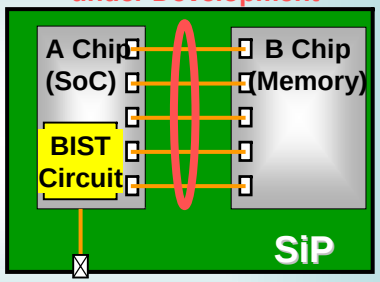
[4] Embedded Test Circuit Saves the Number of External Terminals

Conventional



Signal Terminals Used Only in SiP
(Ex. Memory Bus)
Output All signals

Embed a Test Circuit on Chips under Development



Output Test Results

Reduce External Terminals
Input Special BIST Circuit

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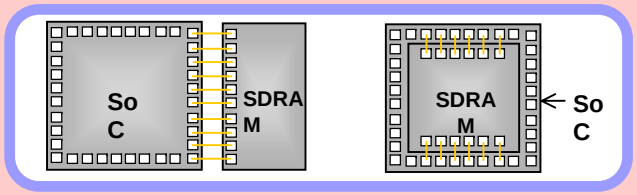
Design for SiP

QFP Type SiP

Side by Side QFP Stack-QFP

<Advantage>
- Possible to reduce assembly cost for using standard lead frame

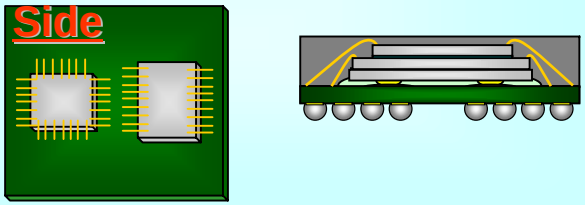
<Disadvantage>
- Required SoC design for embedded memory
- Limited Quantity of Embedded Chip (about 2chip)
- Low Wiring Flexibility



Need to adjust pad position perfectly

BGA Type SiP

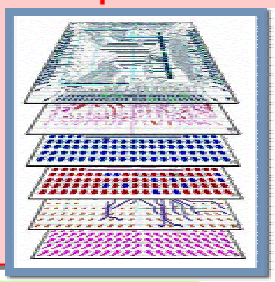
Side by Side Chip-Stack



<Advantage>
-Possible to improve free wiring by multi-Substrate and electrical characteristics improvement
-Possible to optimize wiring high speed bus and power supply/GND wiring

<Disadvantage>
- Cost higer compared to QFP type

Design of interposer optimized



<Advantage with SiP>
-Reduce design load by high-speed bus unnecessary design
-Reduce quantity of system board, size and substrate quantity
-Part arrangements simplification

<Strategy of total SiP cost reduction>
- Reduction of number of signal
  => Reduction of number of layers
- Reduction of external terminals by adopting test circuit test
- Customized SoC design for optimizing SiP structure

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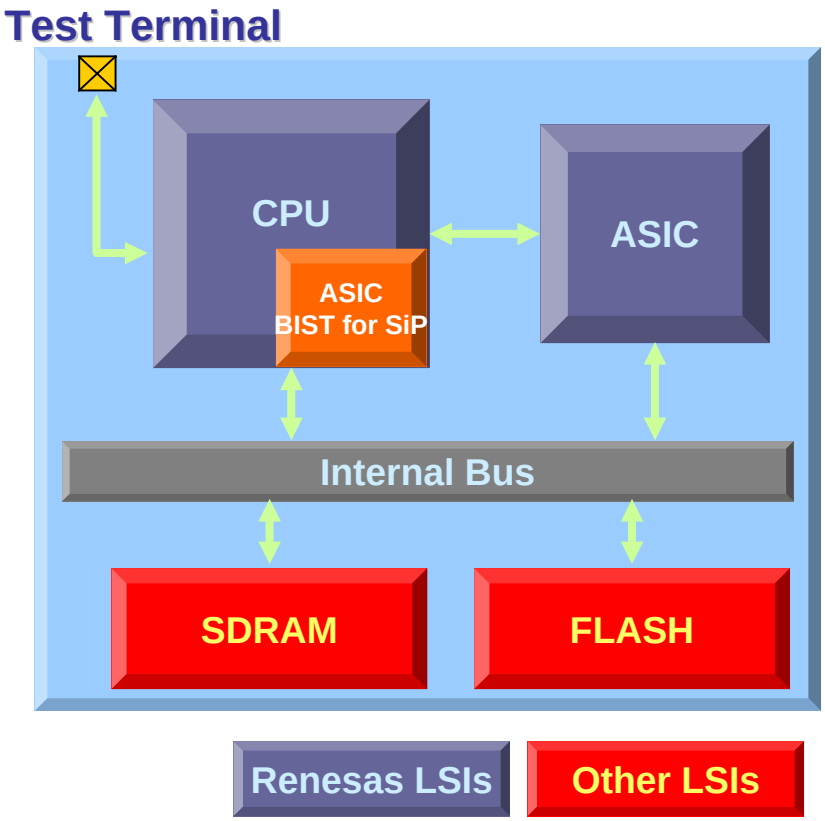
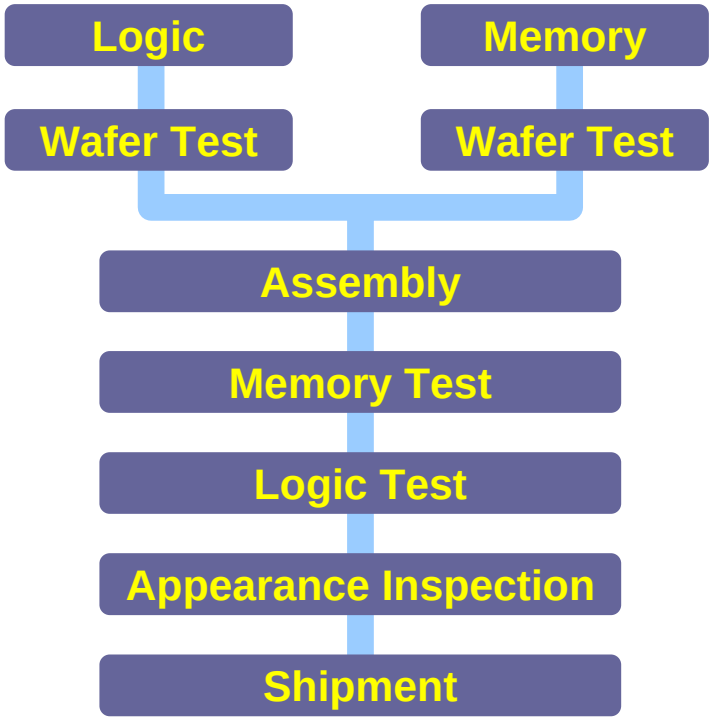
SiP Test Strategy

Quality Guaranteed by RENESAS Original Testing Method

SiP System Test with Test Terminal





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7. SiP Design Technology for High Speed I/F

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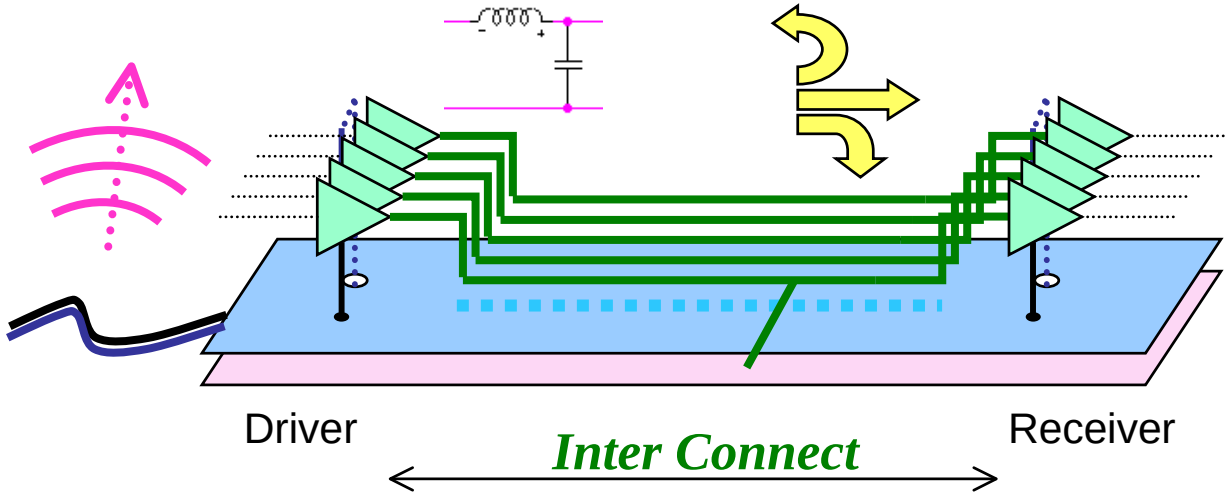
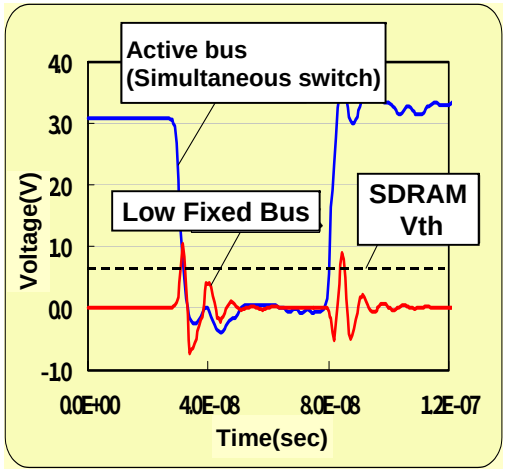
Noise Problem of Speed-up and Mounting System

High Speed Devices

Higher frequency operation

- **SI (Signal Integrity)** → **Signal System** <Reflection / Cross Talk>
- **PI (Power Integrity)** → **Power Supply** <Simultaneous switch noise>
- **EMI (Electromagnetic Interference)** → **Power Supply** <No-need electromagnetic radiation>





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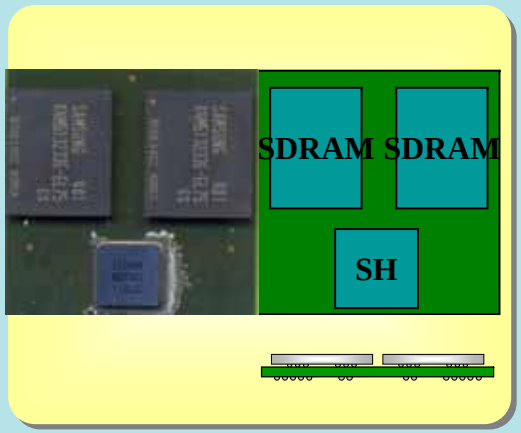
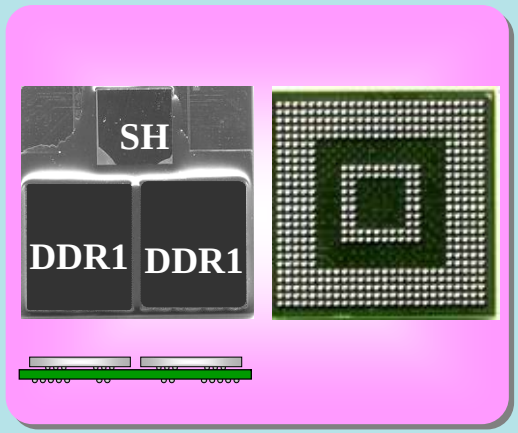
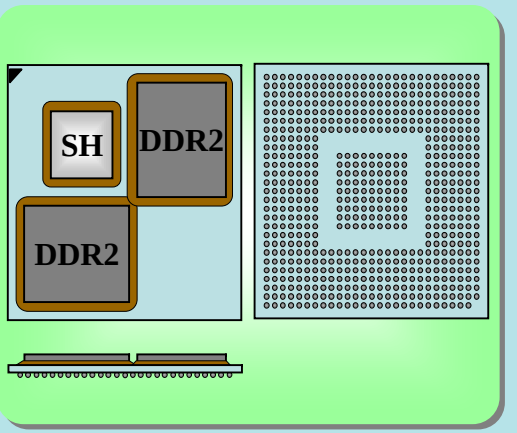
SiP Product Roadmap for High Speed







Embedded LSI	・SH7751R ・512Mbit SDRAM (x32bit) CSP 2pcs	Embedded LSI	・SH7780 ・512Mbit DDR333 (x16bit) CSP 2pcs	Embedded LSI	・SH-Navi ・512Mbit DDR667 (x16bit) CSP 2pcs
Outline	27mm x 27mm 408pin BGA 1.27mm Pitch 20x20 (5row)	Outline	23mm x 23mm 484pin BGA 0.8mm Pitch 26x26 (5row) +10x10 (2row)	Outline	29mm x 29mm 640pin BGA 1.0mm Pitch 27x27 (7row) + 9x9
133MHz SDRAM		**333MHz DDR1**		**667MHz DDR2**	

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SiP Solution for High Frequency System

DDR System Solution Business Proposal by Renesas Original Technology

Customer's Development Term Reduction for Complicated DDR I/F Design
Reducing Mounting C/R Number and Customer Board Size

EMI Noise Reduction
Switching Noise Reduction

Renesas Supports Memory

Reduce System Power Consumption

Total Cost Reduction, Improve Performance

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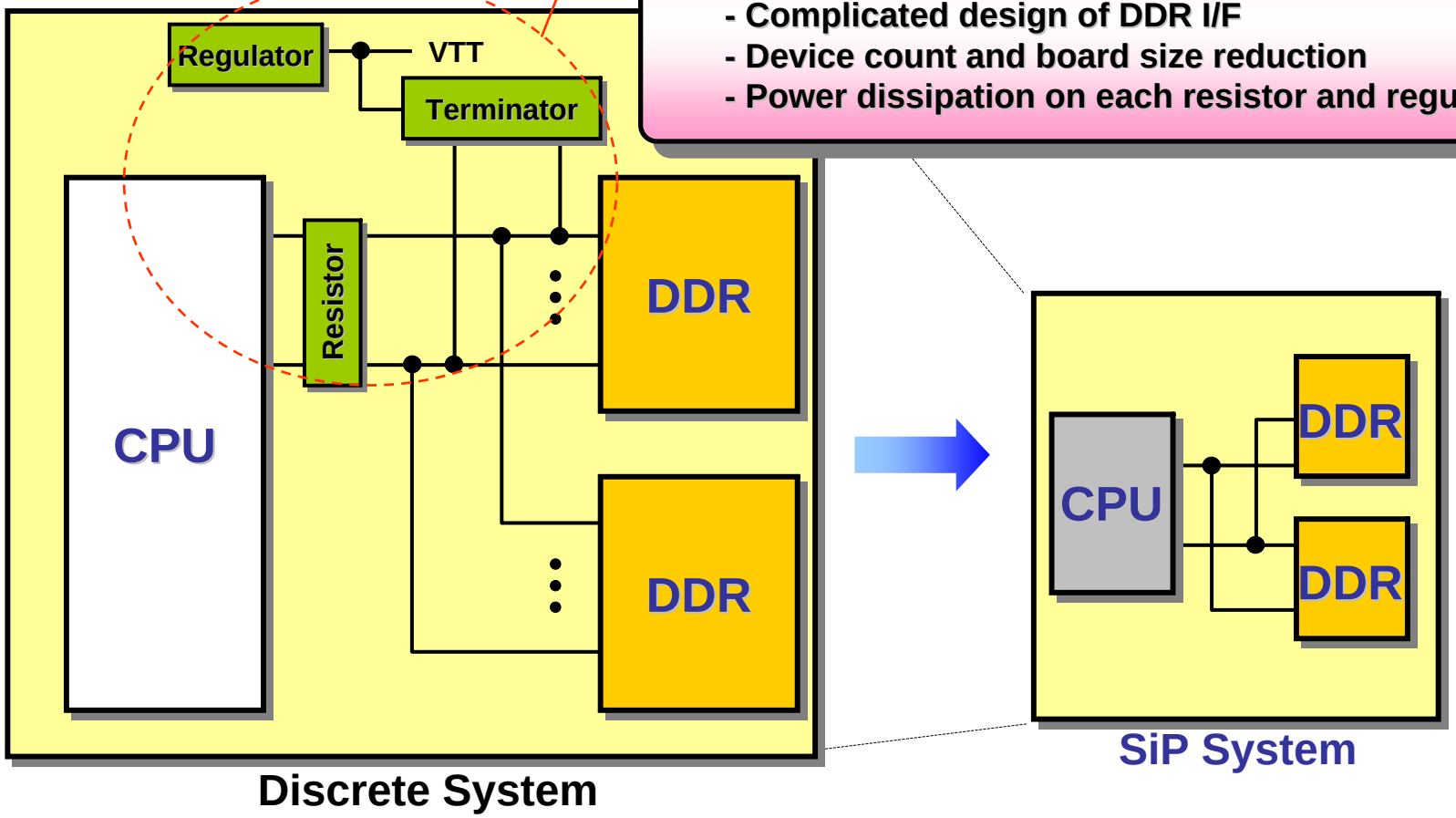
Easy DDR System Design by SiP

Renesas SiP makes customer free from the design of complicated DDR I/F

Almost all devices can be removed with SiP solution.
Then, customer does NOT need to care about
- Complicated design of DDR I/F
- Device count and board size reduction
- Power dissipation on each resistor and regulator



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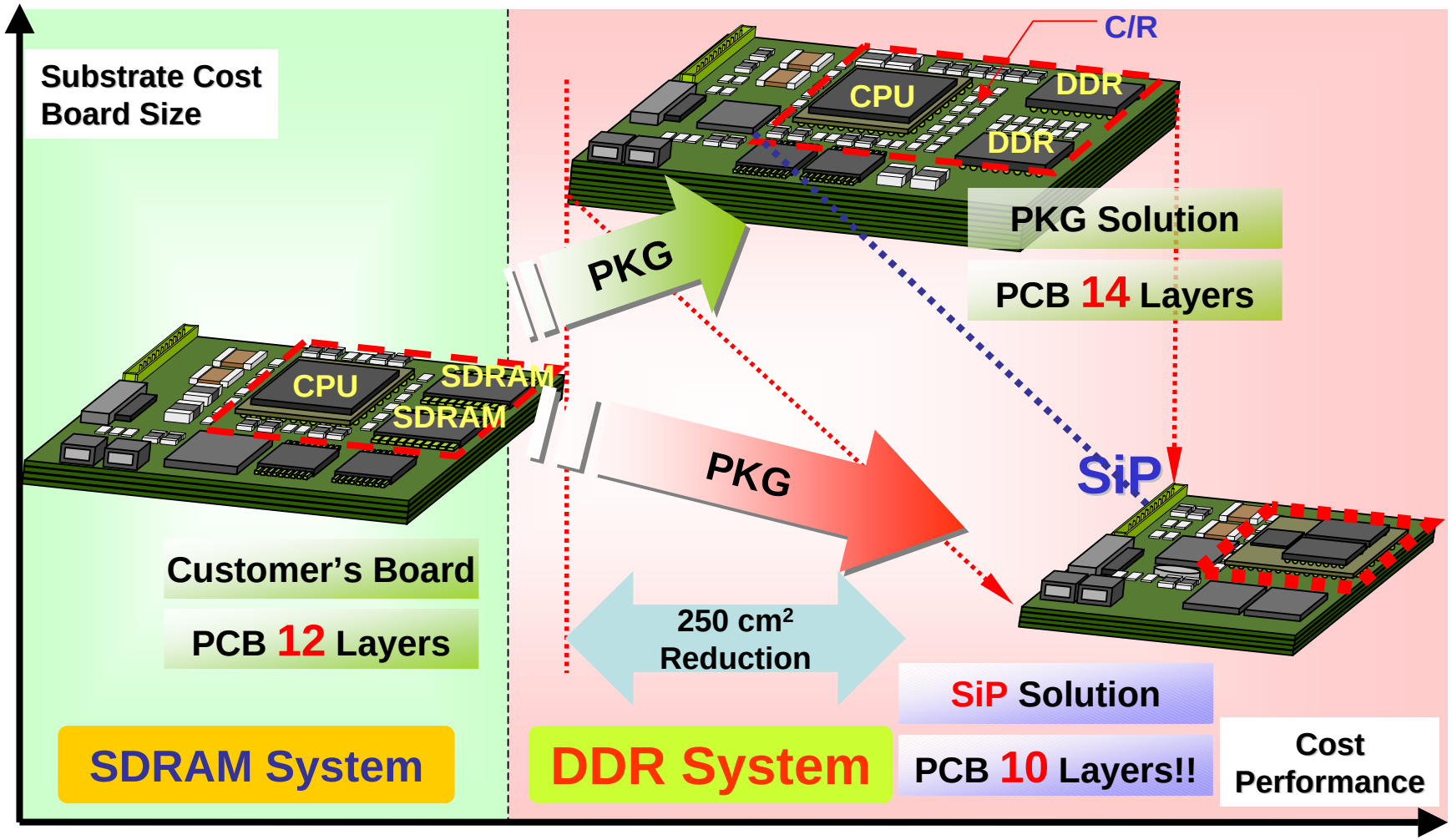
Total System Cost Advantage of SiP DDR



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The strengths based on DDR-System

■Reduction of Resistance of DDR IF Series and Terminate Resistance

* The Optimization Design of SiP

Reduces series resistance and the terminator.

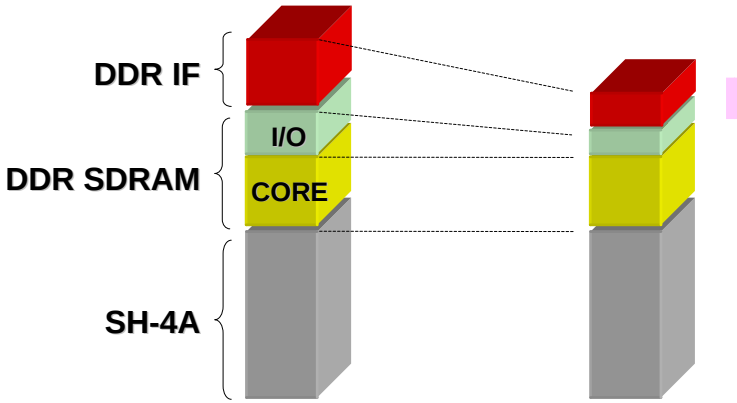
* A high-speed design of DDR IF is unnecessary.

■Effect of electric power decrease

* The power consumption of DDR IF can be decreased.
* Half the output electric power of DDR can be decreased by the drivability control.
* The power consumption of the regulator of VTT can also be decreased.

Graphic・DTVField

■Power Comparison

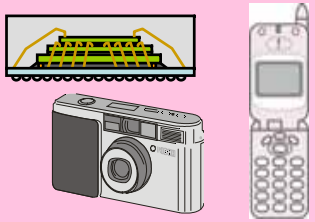


Discrete System SiP System

Reduce Power Consumption of DDR I/F Power

CIS Field

Celler・DSC Field



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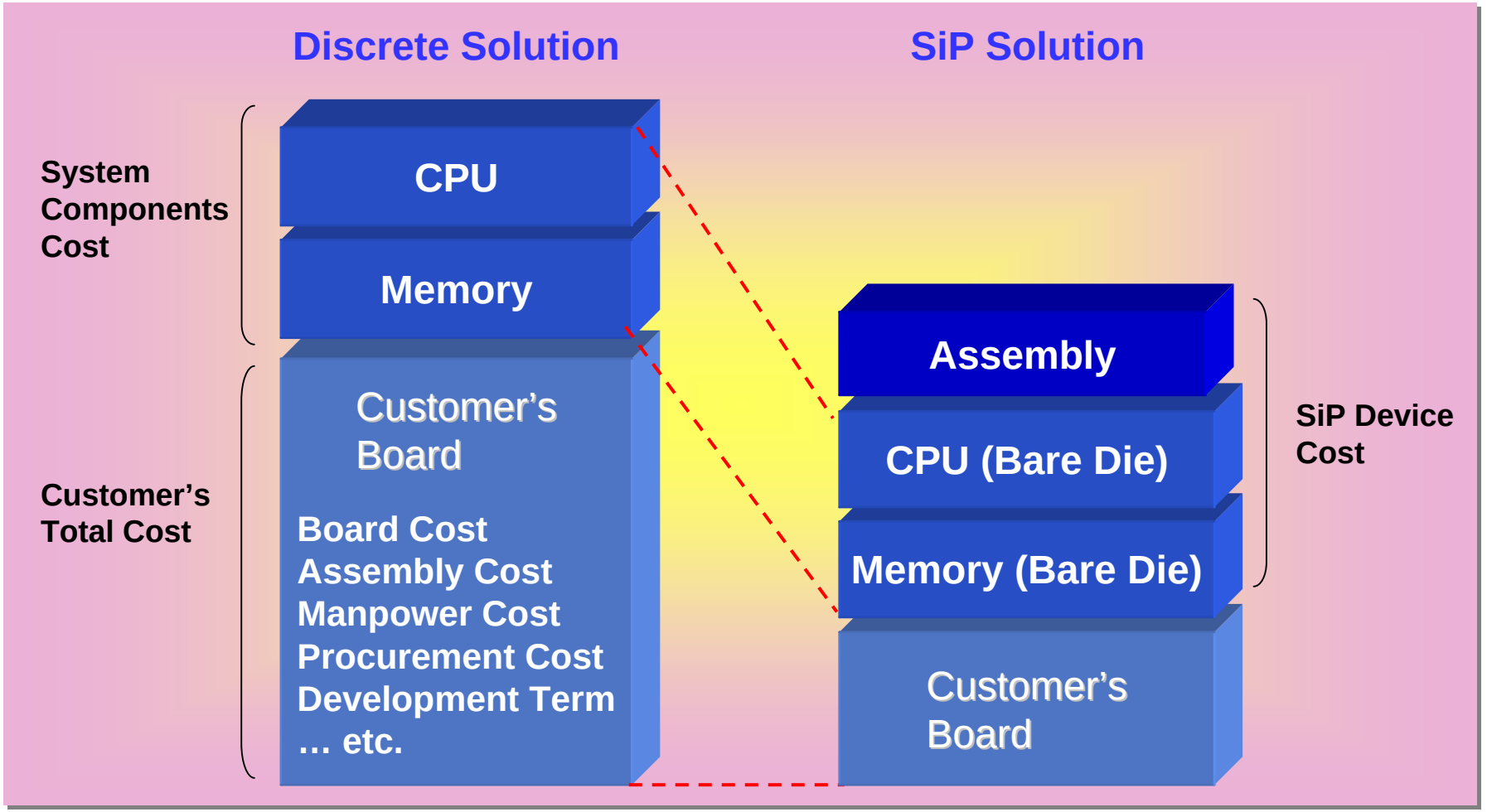
SiP can save Customer's Total System Cost



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8. SiP Mounting Technology

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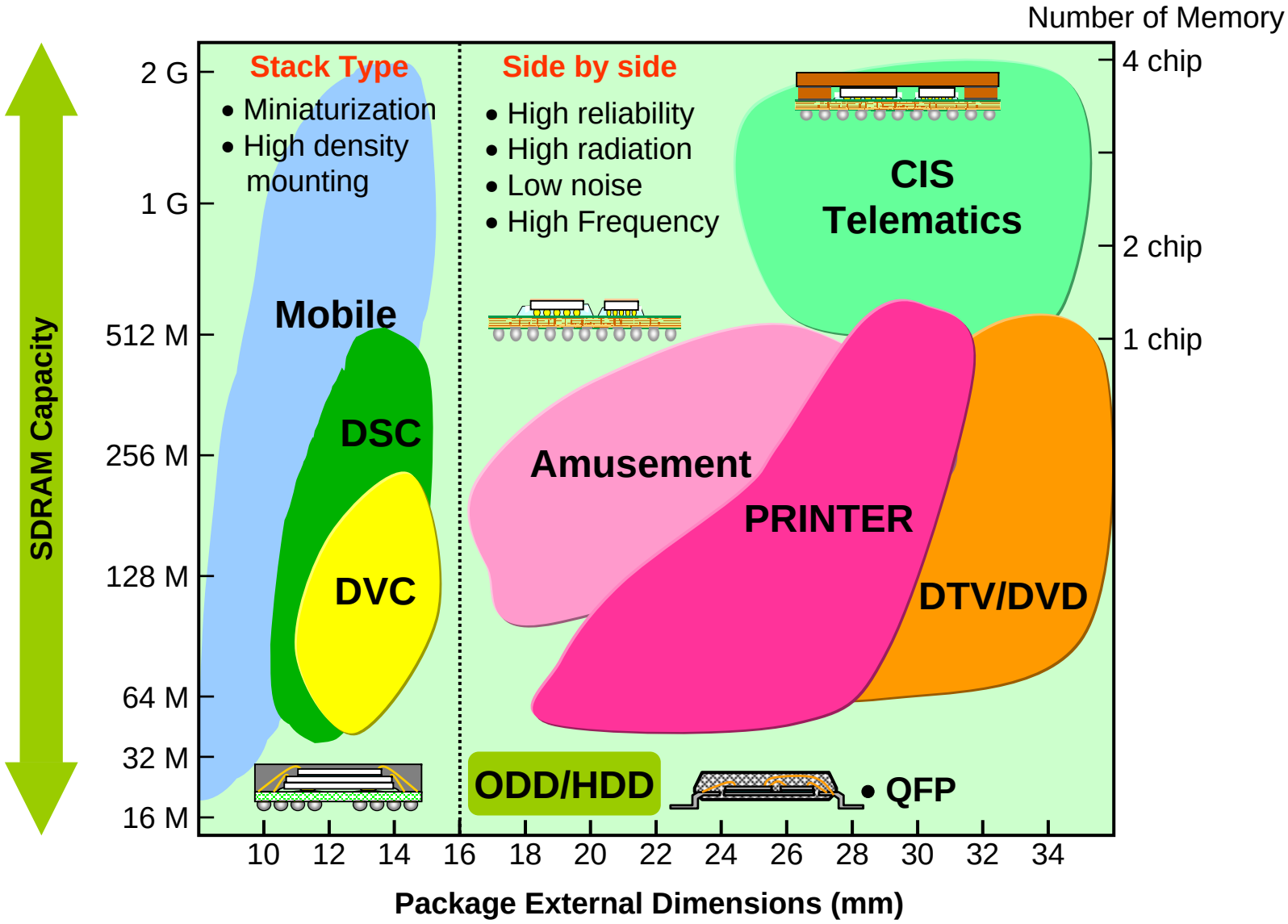
Required Memory size by Application



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Technology to realize miniaturize and high quality

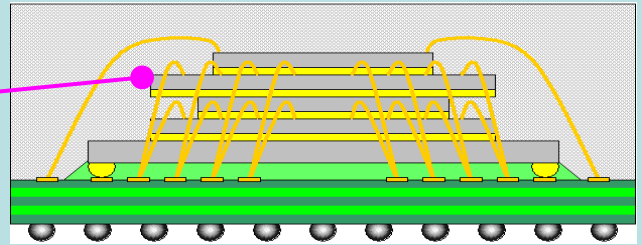
- Applied the result of the top-level world research to the mounting technology.
- Support from design to mass production by mounting technology as the ITDM manufacturer

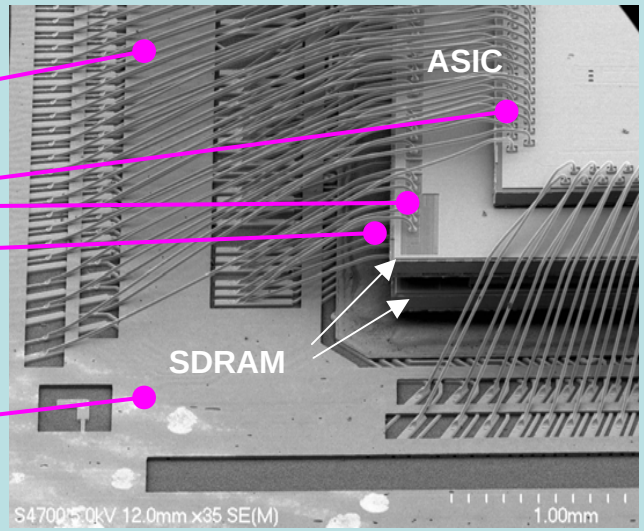
~ Realization of small size/high density SiP by FC technology + WB technology ~

Wafer super thin grinding technology
-300mm wafer super thin processing technology
- 90μm ：mass production
  50～70μm ：under development
- same processing level as 200mm wafer

Wire bonding connection
- Long wire formation
- Super low loop wire formation
- narrow pitch wire bonding tech.
  - 50μm pitch under mass production

Board Technique
- thin board technique, low warpage substrate technology





5 layer solution for DSC

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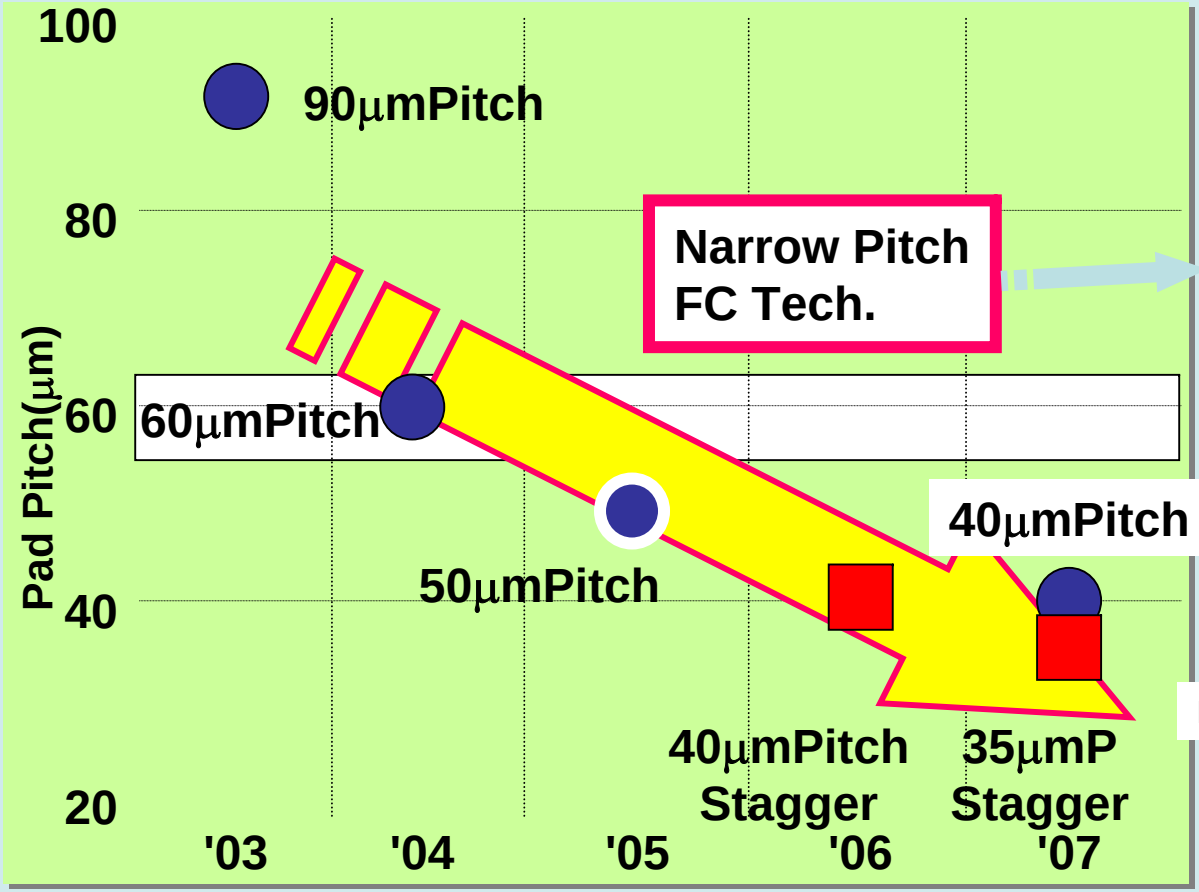
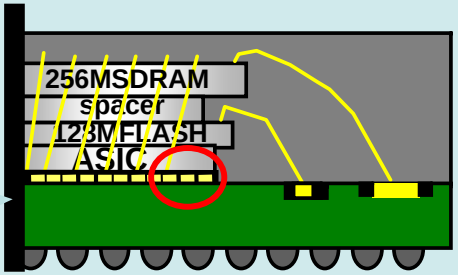
The Trend of FC (flip chip) Technology

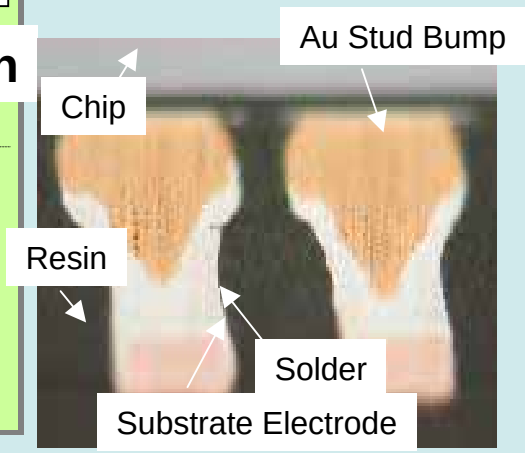
■Au Solder connection technology



Effect of FC mounting technology development road map



Structure of SiP



View of Connected section

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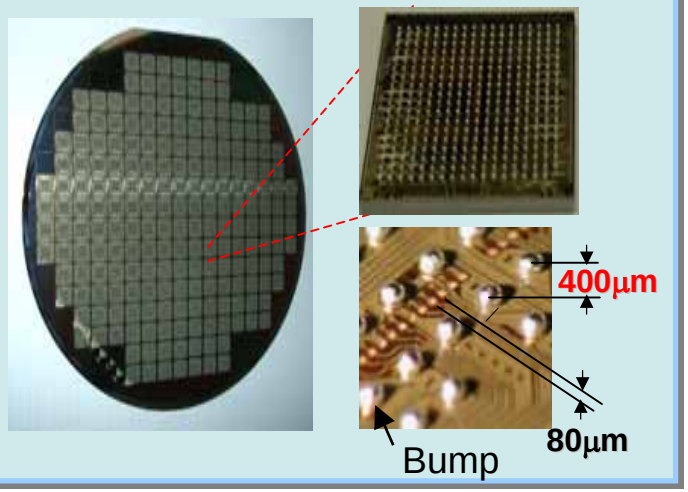
Renesas SiP Highly Reliable Flip-Chip Connection Technology

～ RENESAS Original Highly Reliable Technology by WPP Technology ～

■WPP (Wafer Process Package)Technology

- ■Realized Real Chip Size Package
- ■Reduced Resistance・Inductance, the best for High-Speed Device
- ■Improvement of Connected Reliability with soldered joint
- ■Executed Test/Burn In to each chip, and make possible The High Reliability Guarantee



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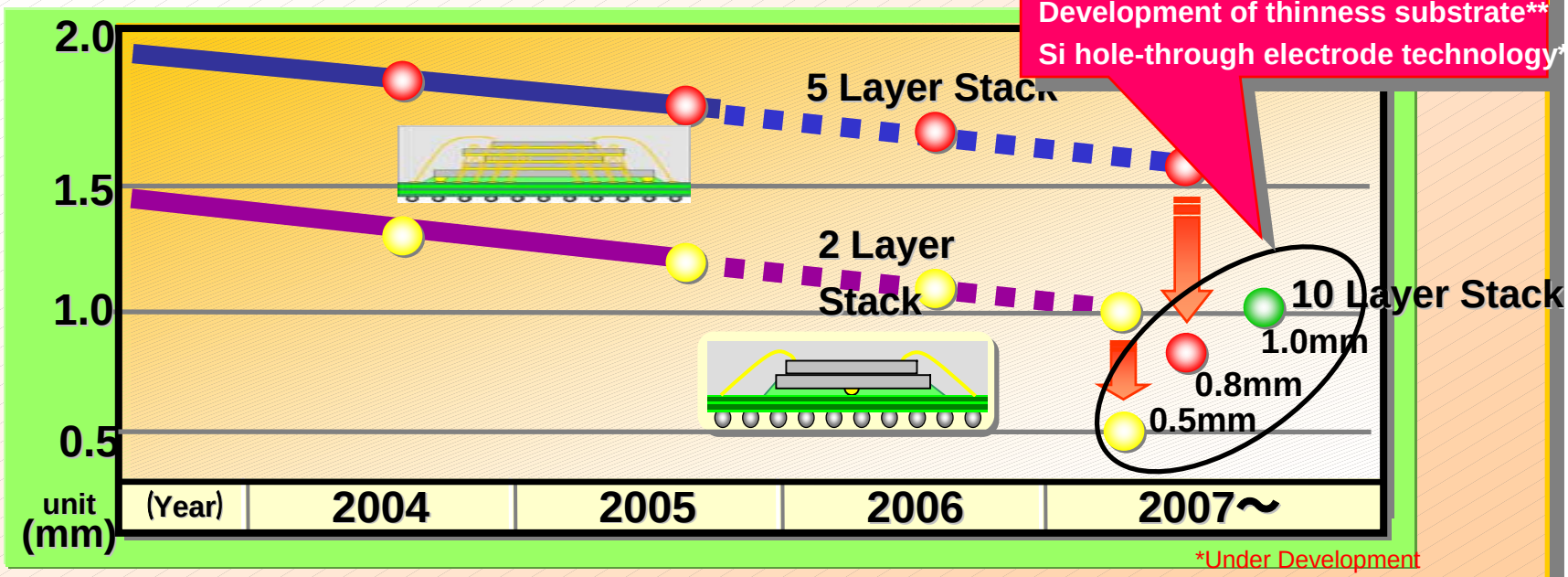
Super Thin Stack SiP Trend

Trend of Package Height

~ For Large Capacity, High-Density Mounting~



Required Technology Development

300ϕ wafer ultra thin processing technology, thin substrate technology, and super-low loop wire bonding technology, narrow pitch FC die-attach technology

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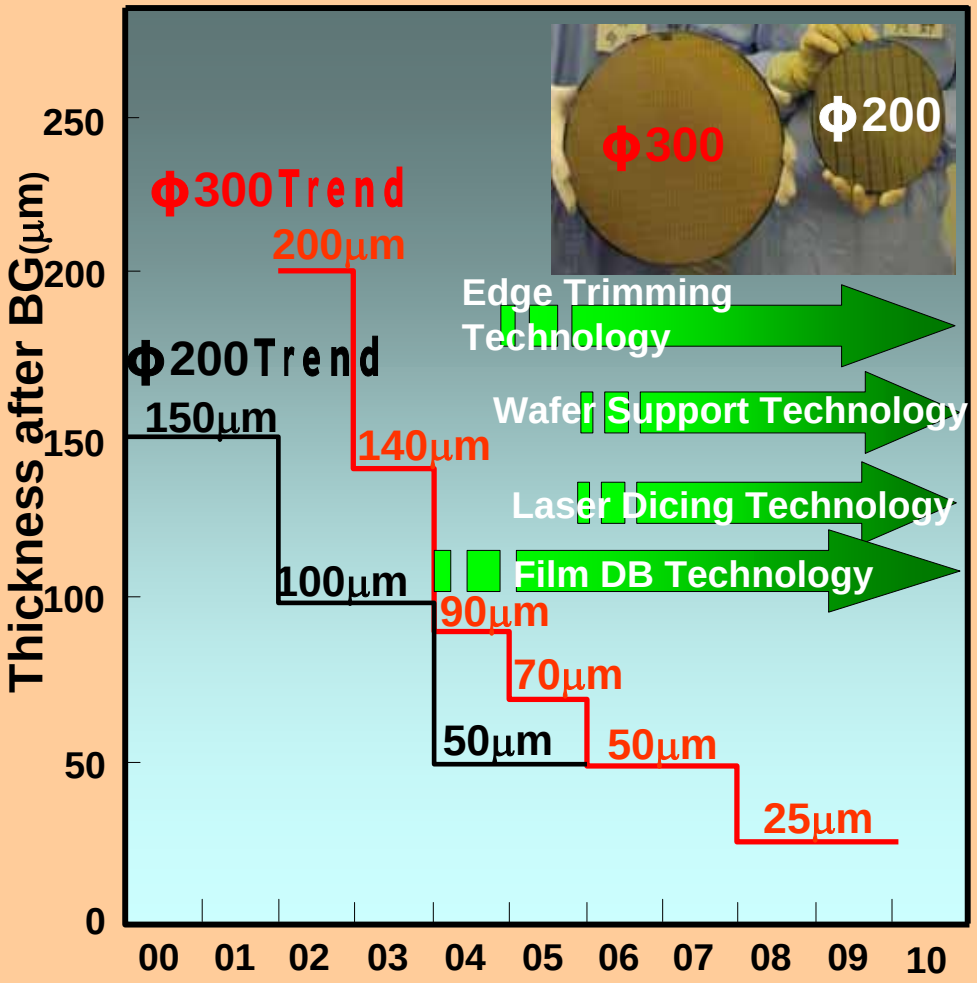
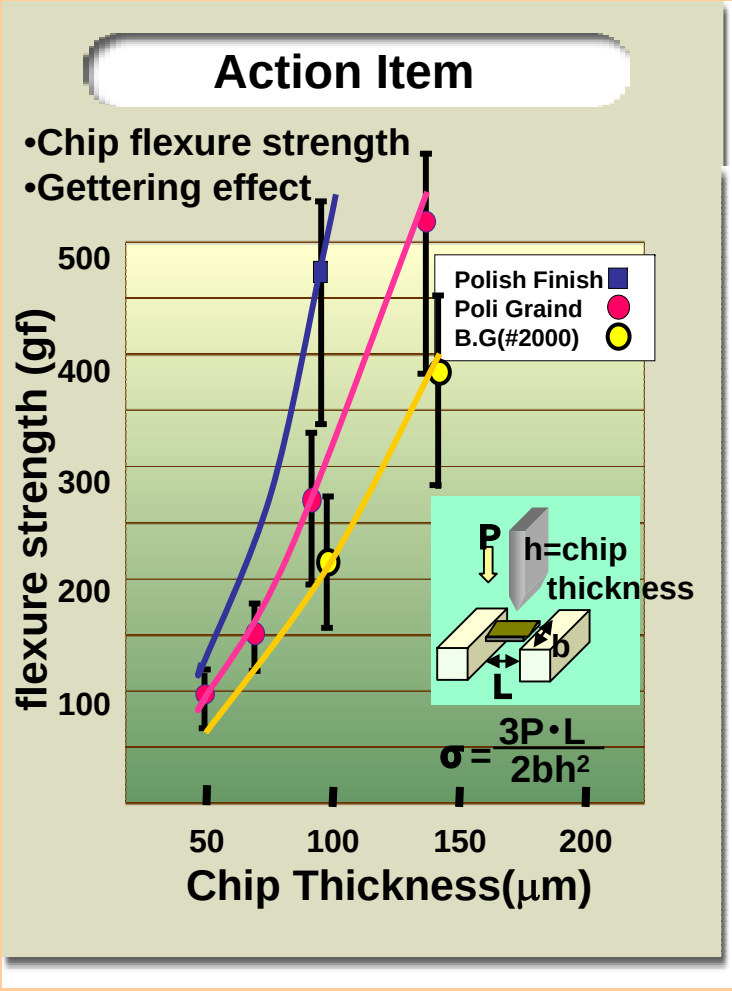
BG(Back Grind) Processing Technology and DB Technology Development Road map

~ To Realize high density multiple memories, miniaturization ~





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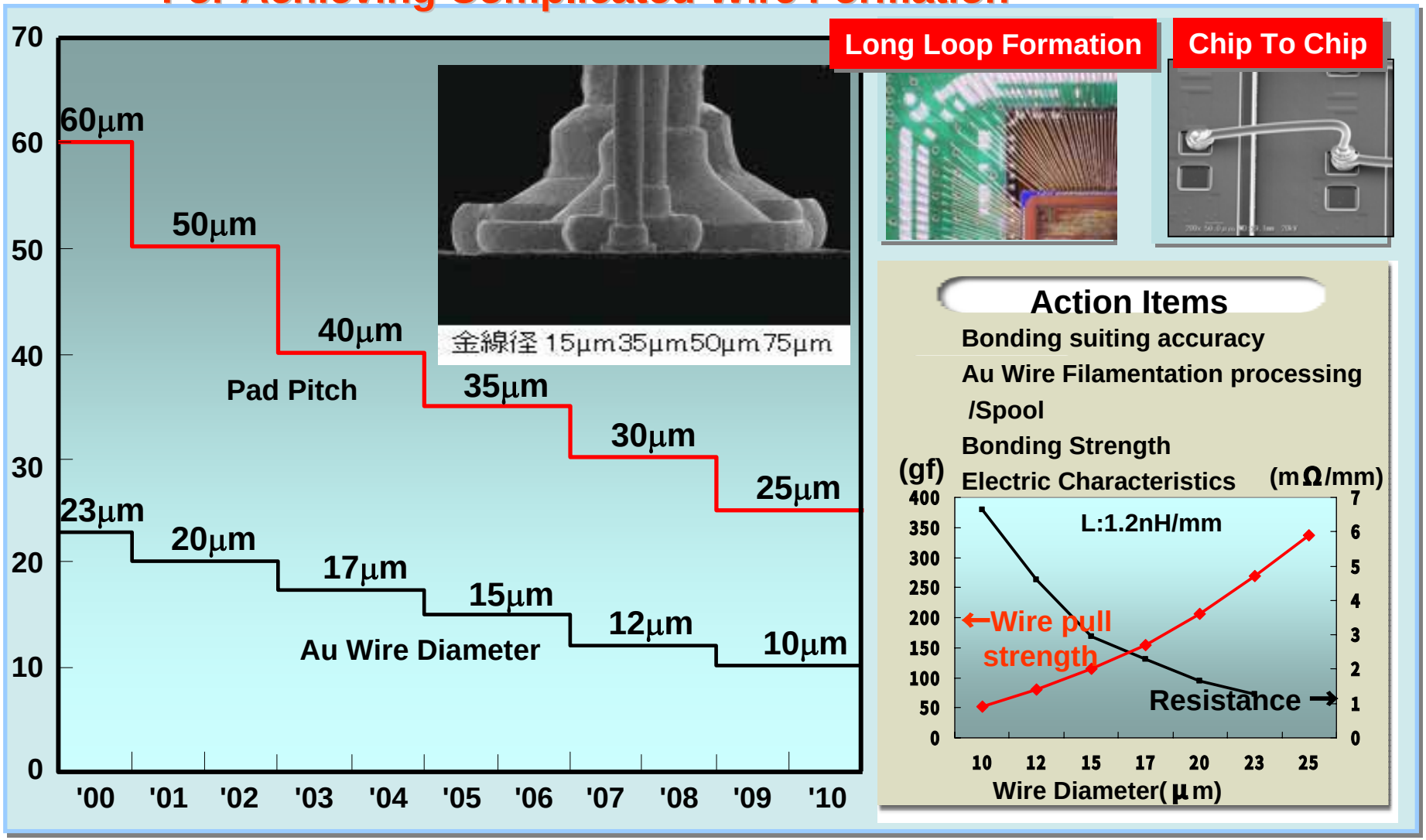
Road Map of Wire Bonding Technology Development

～ For Achieving Complicated Wire Formation ～



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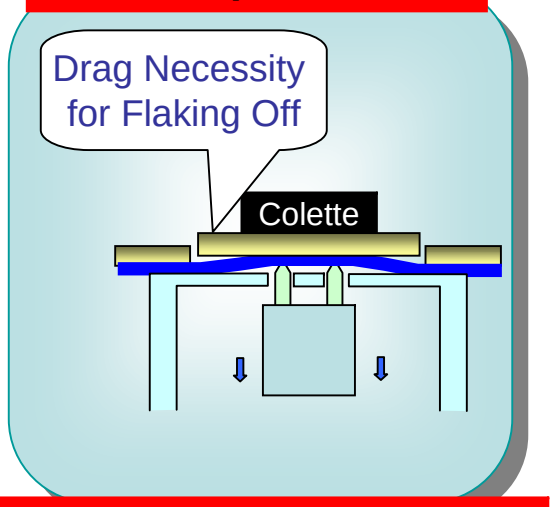
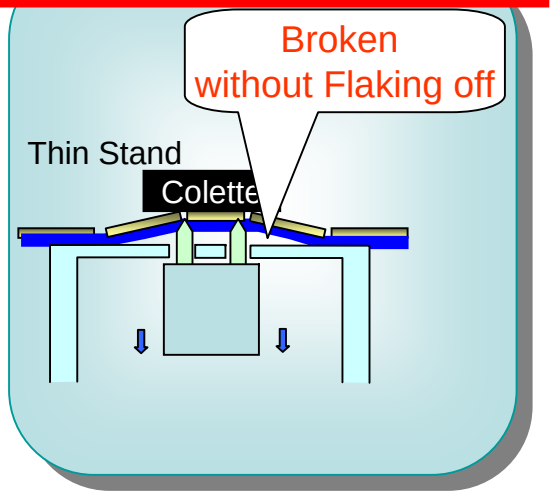
Thin Wafer Pick-Up Technology

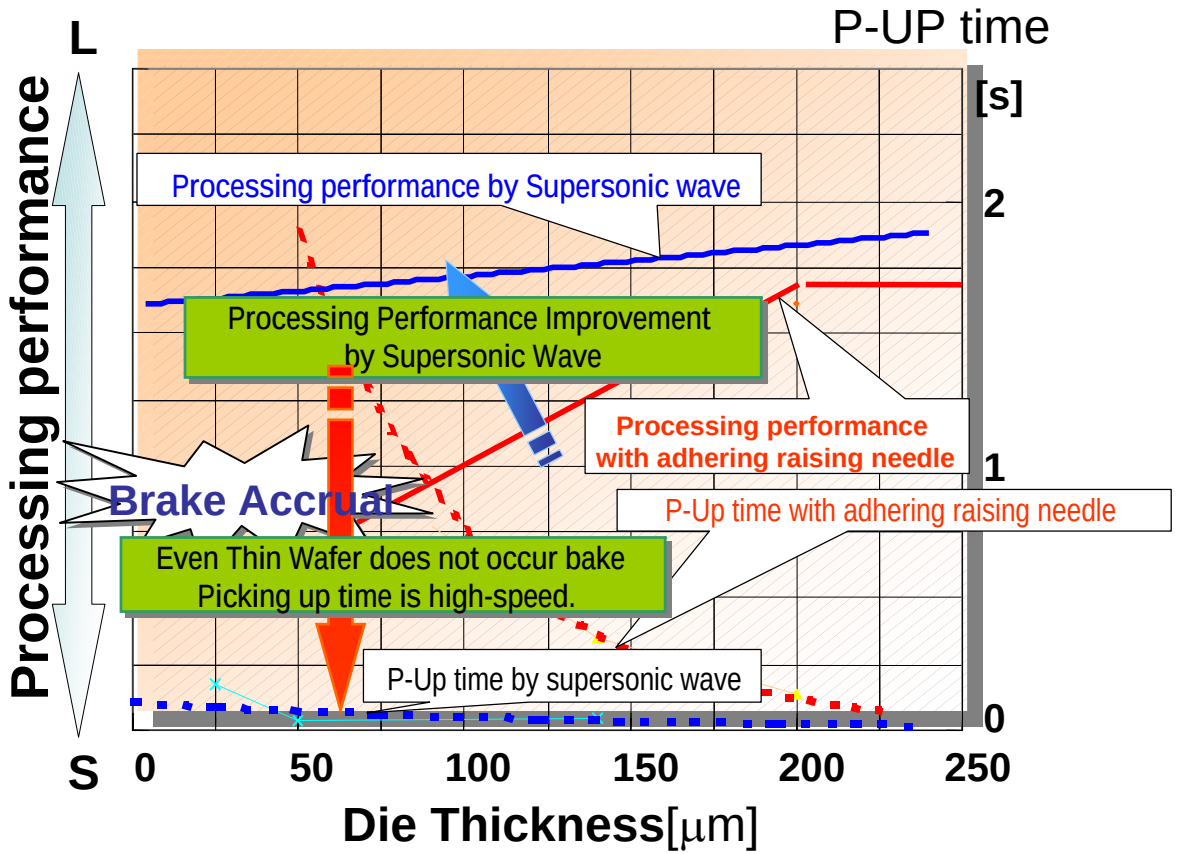
～ Examination of picking up technology with supersonic wave ～

Before Optimization



Chip Thickness t≦ 50μm





【Benefit of Supersonic Wave】
Even Thin Chip can be effective to produce
⇒Good for Super-thin type Stack technology

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9. Stack SiP Development Trend

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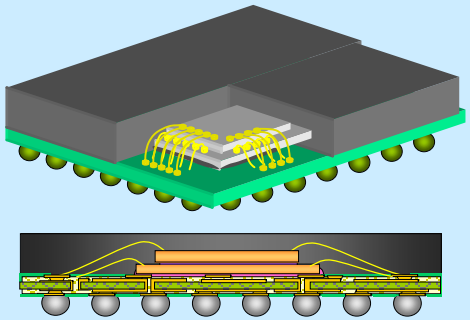
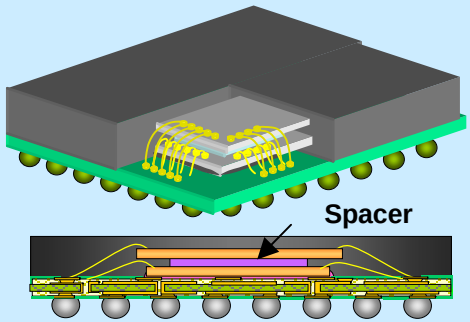
Spacer less Technology**



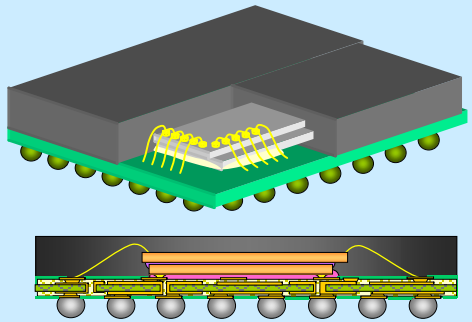
(No Spacer)
WB+WB

Large chip size constraint



(Need Spacer)
WB+WB

- Need chip size constraint (Overhang constraint)
- Increase spacer additional work
- No-need Center pad parts

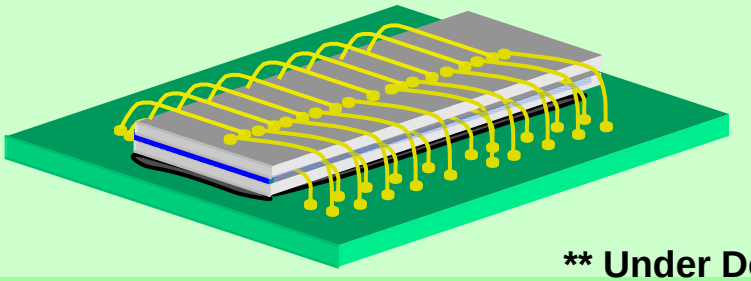


FC+WB

Required substrate such as Built-up for a high density small size/mounting

Decrease Mounting Constraint and Multi Stack Technology by increased Stack LSI

Spacer less technology



** Under Development

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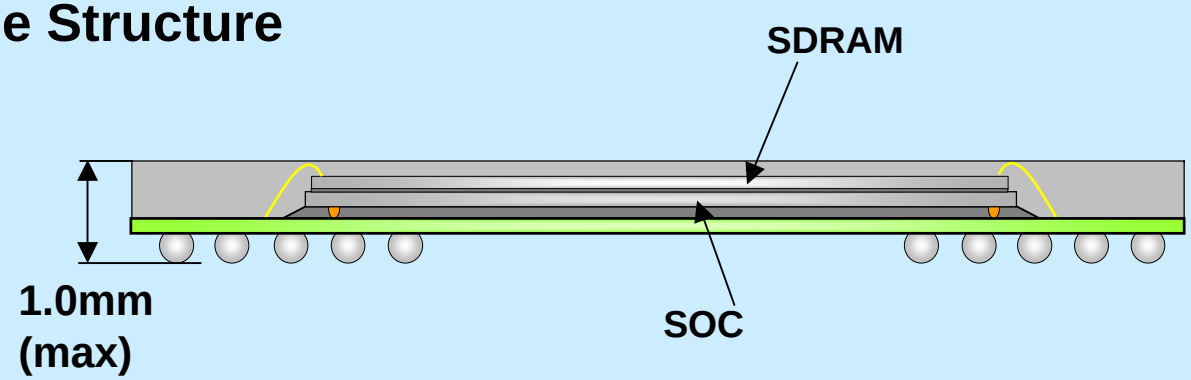
Thin SiP substrate**

Sample Structure



Coreless substrate: Thickness less than 0.1~0.2mm
(Current Products 0.4mm)

** Under Development

Advantage

- Suitable for thin/small products such as mobile or HDD/ODD

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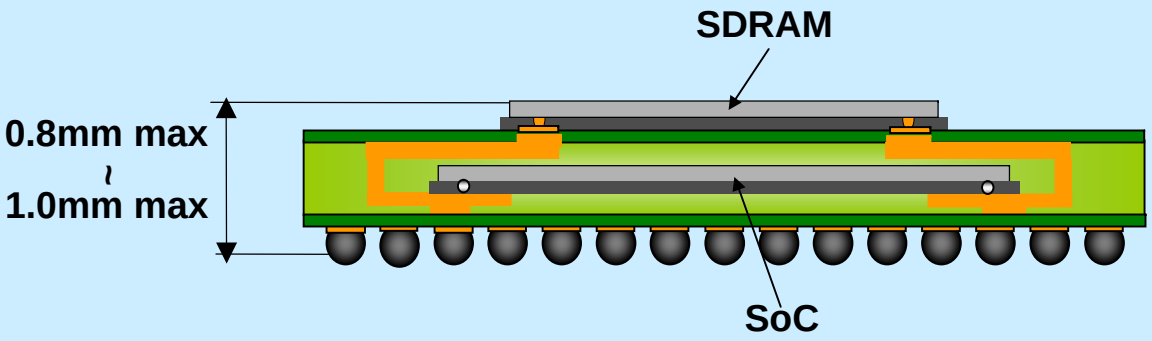
LSI embedded substrate SiP**

Sample Structure



Realize thin type by embedded SoC in the substrate and FC connected SDRAM

** Under Development

Advantage

- Available for system black box such as security field
- Possible to make high density memory

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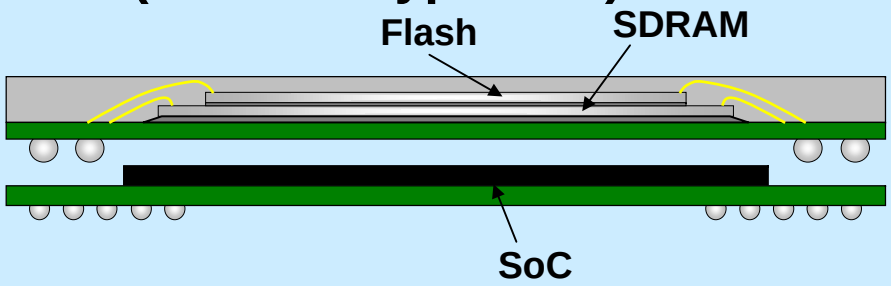
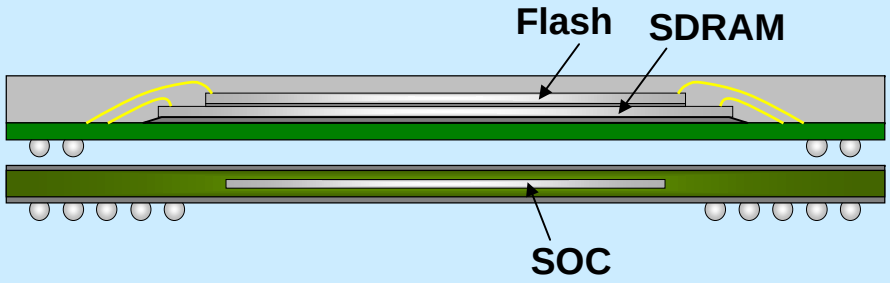
PoP(Package on Package) Technology**

Sample Structure (mold/FC type PoP)



Sample Structure (substrate LSI buried type PoP)



Using LSI embedded technology for lower substrate

** Under Development

Advantage

Variable memory capacity/supplier
Possible for memory shrink

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10. Next Generation SiP Technology (CoC Technology)

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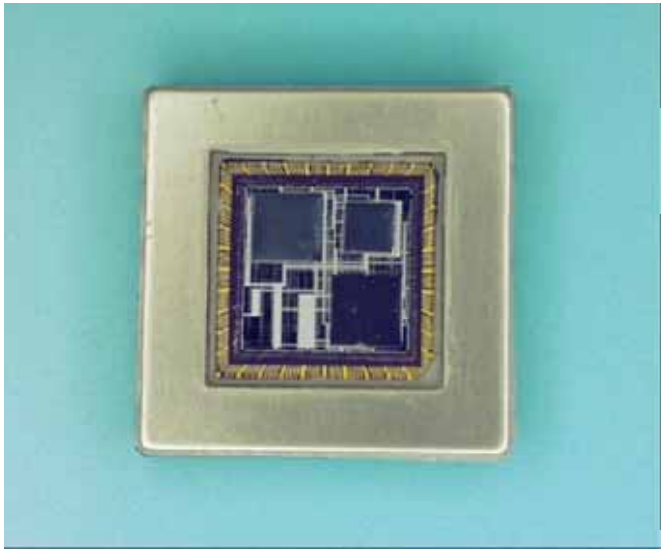
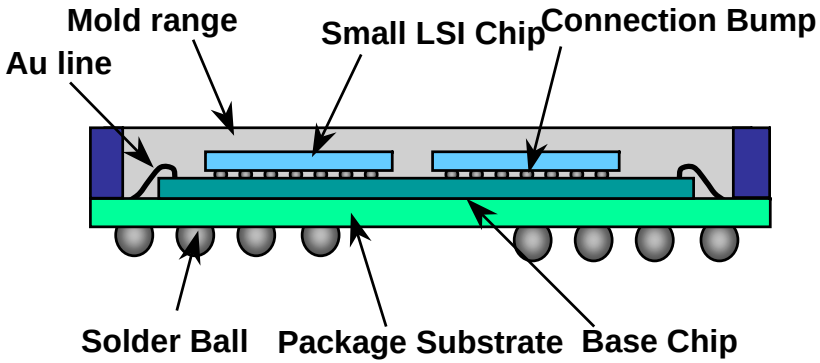
Benefits of CoC Technology(Chip on Chip)

- Interchip High-Speed Data Transfer
  (CPU-Memory etc.)
- Various kinds device consolidation SiP
- Process Consolidation of Various generation
  (maturity + point)
- High density mounting
- Thin making multi chip accumulating PKG



★ When Base Chip is global wiring Chip
- Minute wiring is unnecessary
  ⇒ Low Cost and Low resisted.

★ When Base Chip is LSI Chip
- mass memory installable
- Global wiring short able
  ⇒Improved Switching Characteristics
- Unnecessary output buffer
  ⇒Reduced Power consumption
- After installed Base Chip, it can be tested.



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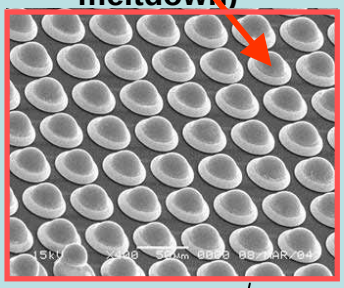
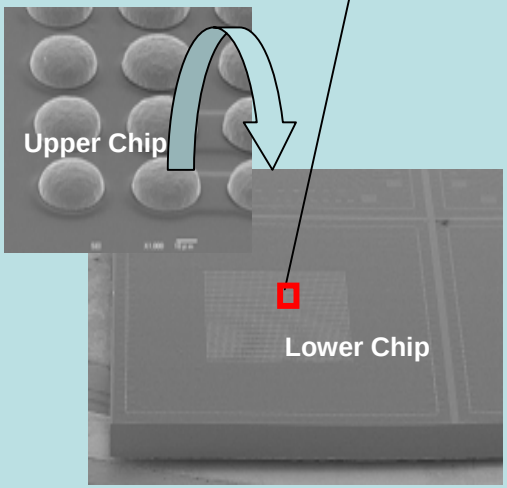
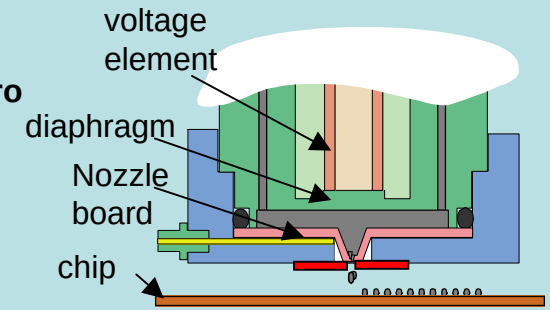
Minute pitch connection for CoC Technology

Solder bump formation

(Exhalation method of Micro meltdown)

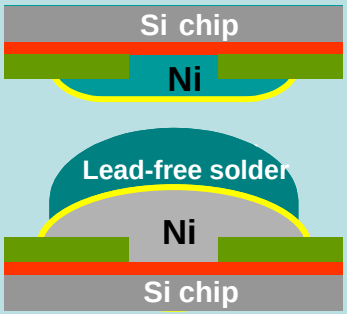




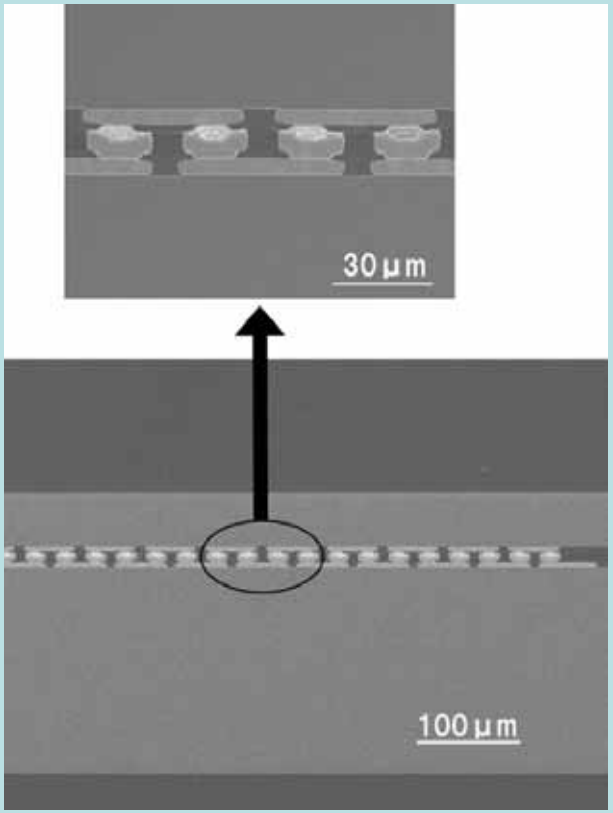


Macro Meltdown Solder exhalation device outline

(Solder Shoot)



Connection part model



Cross section after connected (30µm pitch connection)

CoC (Chip on Chip) Connection COC(10,000bump)

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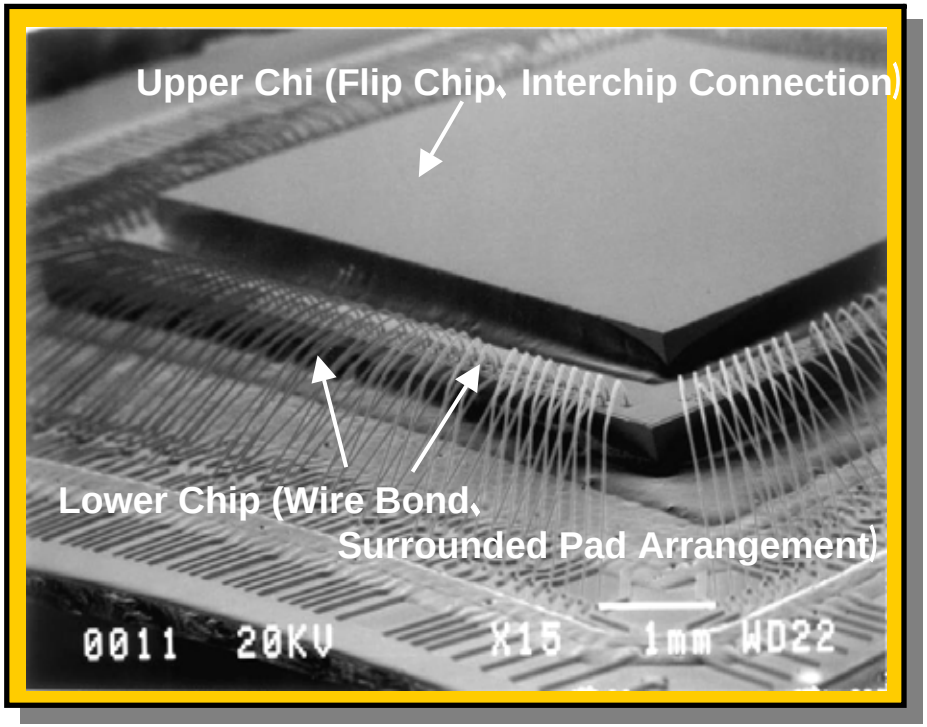
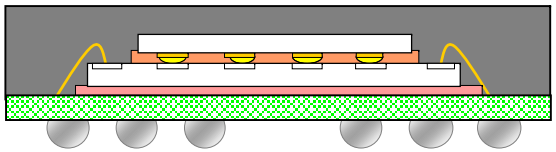
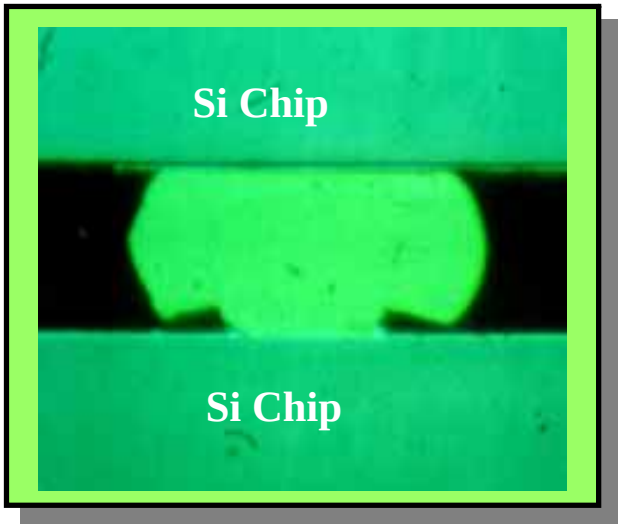
Technology of Chip to Chip

- Substrate NET Reduction by LSI Development only for SiP
- For High-speed Operation
  (Improvement of data Transfer rate)
- Digital and Analog Separation (Point SoC
  Achievement by SiP)



SiPWhole general view observation Ex.





Chip On Chip Connection

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11. Next Generation SiP Technology (Si Hole-through Technology)

~ Technology for Ultra thin multi stack SiP ~

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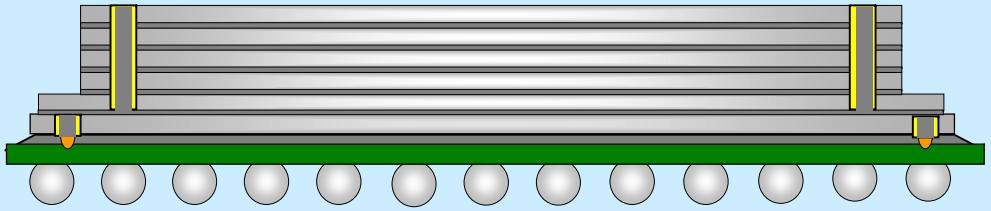
Development of Si Hole-through connection Technology**

3-D SiP by Si hole-through Connection Technology



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Advantage

- Connect chip interconnection at standard temperature by caulking technique
- Thickness of Stack SiP PKG is reduced by half

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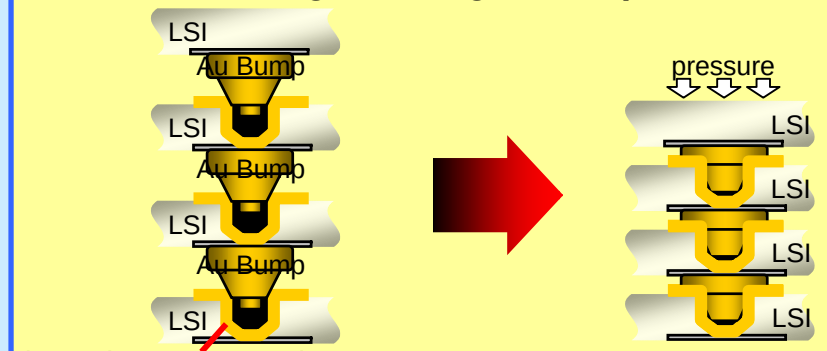
SiP Product TEG with Si hole-through Connection**

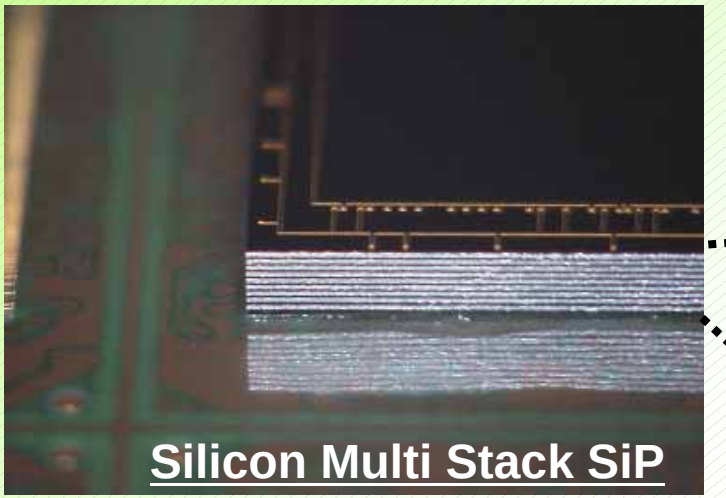
~ High Density SiP Technology by 3D Multi Stack ~

- **Low Cost 3D Silicon Multi SiP Process**

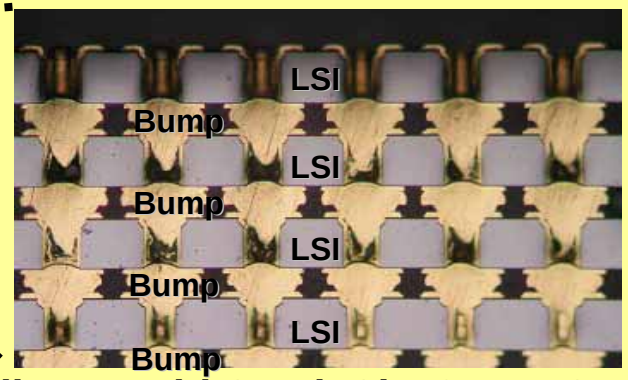
  Cost for Through Electrode Formation with Standard Temperature Chip interconnection with Caulking Method -> 70%

Room temperature chip to chip interconnection using caulking technique





Silicon Multi Stack SiP



Silicon Multi Stack SiP Cross Section

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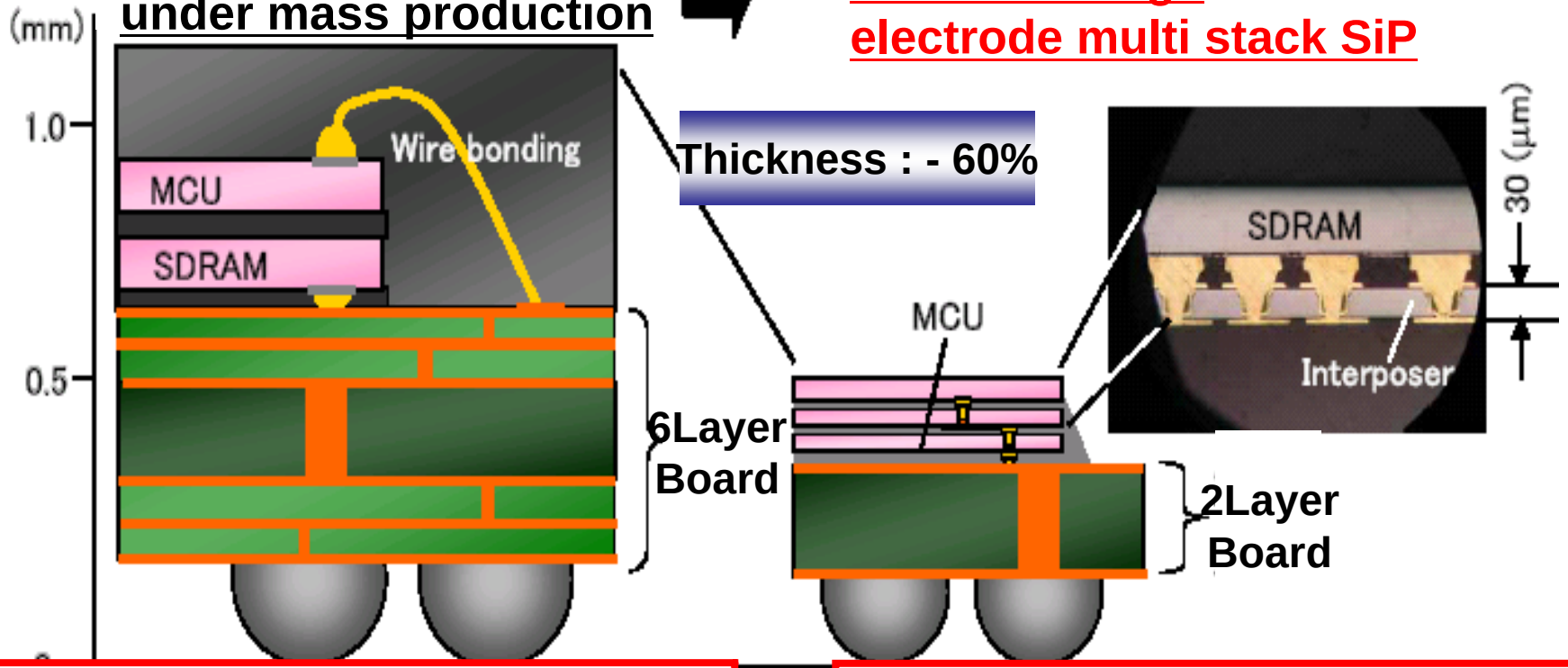
Realize Small/Think making with Si hole-through connection**

WB Multi Stack SiP under mass production

Si hole-through electrode multi stack SiP



- Package Thickness : 1.25mm
- Package Board : 6 layer (t=0.46 mm)
- Wire Length : Long
- Resin-sealed Required

- Package Thickness : 0.5mm
- Package Board : 2 Layer(t=0.2 mm)
- Wire Length : Shortest (WB-less)
- Resin-sealed Not-required

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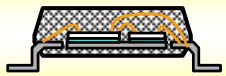
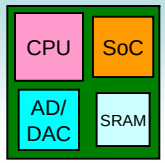
SiP Roadmap

QFP Type

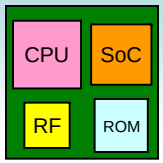


Existing Package Support

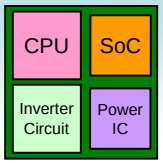
Support for New Application Fields



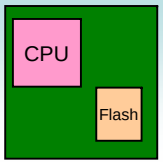
Analog Application
Graphic, Sound Equipment



High Frequency
Bluetooth
Wireless LAN



High Voltage Tolerance Application
Motor Driver



Micon Area
Security Area

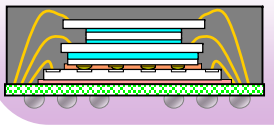
Under Development

Next-generation Technology

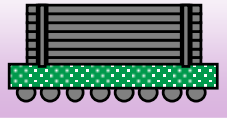
Next-generation ultra small 3D Mounting Technology

Under Development

Chip on Chip Technology



Through Hole Electrode Technology



IC included

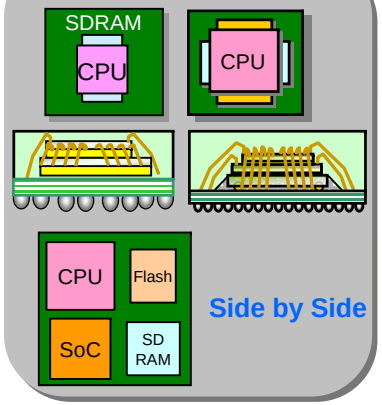
Stack Type

5 Layer/Multi Layer

Super-small, Ultra-thin Type

Miniaturization for Digital Consumer Cellular Phone, DSC, DVC, etc.

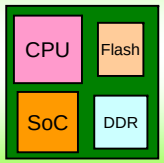
2 or 3 Layer Stack



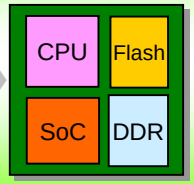
Side by Side

High-performance High Speed I/F

Side by Side



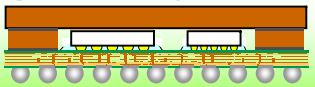
WTR



- CIS
- Telematics
- Network

H.S Side by Side

High Reliability/Radiation



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