– Trend of Advanced SiP –
– Technology Development –

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System Solution Business Group
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   - Si Hole-Through Technology-
1. Semiconductor Needs for Ubiquitous Network Era
Macro trend of growth rate at Semiconductor Market

The rate of market growth is tend to become slow
Action item is Determination of
The Next Generation Growth Market and Resource Concentration

* CAGR is calculated after it approximates in order to decrease influence to Silicon Cycle.

Ref. : WSTS(2005.10)
Classification of Application and Convergence

Developing function convergence such as Multimedia Processing and Network. Continuity and development of Excellent Hard IP and Software IP become Important.

Multimedia Processing
• High speed Graphic Processing
• MPEG Extension Technology etc.
Huge Expansion of Application Software Development
Progressing Expansion of Software Development
in Ubiquitous Network Equipment

Source: PA Information Processing System Society of Japan embedded system research Gr establishment commemoration symposium (July, '05)
Action item of Semiconductor System Solution

“Diversification”, which is Action item of Ubiquitous Network Equipment Semiconductor is required revenge of “Convergence”, “Development Expansion of Software”, “Short-term Development Cycle”
Device Innovation which realizes semiconductor needs in the ubiquitous generation

SoC Platform and **Advanced SiP** get more important

**Semiconductor Needs**
- Response to Diversification
- Function/Technology Convergence
- Software Development
- Short Development Cycle

**Device Innovation**
- Reconfigurable Device
- SoC Platform
- **Advanced SiP**
  - Standard MCU/DSP
  - Analog, High Frequency Technology
  - Sensor Technology, etc.
2. Approach toward System Solution
More Difficult Needs for SoC to Realize

- Larger Capacity Memory, High Frequency Bus and High Performance Analog Circuit are Required to Realize Ubiquitous Equipment
- Realize the best solution with SiP to combine High Powered SoC, Mass Memory and Highly Accurate Ubiquitous Equipment Needs

Ubiquitous Equipment Needs
- Larger Analog Circuit
- Larger Density Memory
- High Performance Analog Circuit
- I/F High Voltage Tolerance
- High Speed Memory Bus/I/F
- Noise Reduction

Expanding Needs of SiP
- Optimum Processes can be mounted
  - Advanced Capacity Memory Process
  - Larger Capacity Memory Process
  - High Voltage Tolerance Process
- Realizing System Design on High Frequency Bus and High Frequent Operation

Achieving various needs is difficult in function/cost

Existing SoC Process
System LSI Business Trend

SiP can drive Maximum Performance for SoC

2000 ~

180 nm to 130 nm Generation

~’90

Combination of Multi Memory

SoC

CPU

ASIC

Analog

Memory

SiP

USB

1394

Card

SDRAM

I/F

I/F

Flash

SoC

SiP

QTAT, Smaller High Frequency Bus Noise/EMI Reduction Large Density Memory

Business Scale Expansion

2004 ~

90 nm to 65 nm Generation

SoC

CPU

USB

1394

Card

SDRAM

I/F

I/F

Flash

SoC

SiP

• High Frequency Interface
• Low Density Memory
• Low Noise (Vcc/Signal)
• High Performance Analog
• Low Vcc

Including Peripheral System
SiP Technology Realizes Various Application Needs

~ SiP Realizes Various Advanced Applications ~

**SiP Advantages**

- Small, Thin, Lightweight
- EMI Noise Reduction
- Easy Design for High Frequency Bus
- Standardization for Customer System Board and Cost Saving
- Low Cost, QTAT Development
- Easy for Purchasing Products And Improve a Productivity at the Overseas Production Line
- System Confidential Affairs

**Applications**

- Mobile
- DSC
- ODD
- Printer
- Navigation Graphic
- DTV
- Security
Advancing SiP Technology to realize Multi Function and High Powered

Request to SiP

- High-Powered System, Multi Function
- Achievement of Best and Low Cost SiP
- Small, Thin, Higher Heatproof inclination
- Large Capacity, High Speed Memory
- Remain High reliability as single chip

Corresponding SiP technology and approach

- High-Speed I/F (DDR), Noise Reduction, Analog
- Design for SiP (DFS)
- High Density SiP Mounting Technology
- KGD, Multi Bit Bus Memory, Tie-up with Memory Supplier
- Optimization of test process

* KGD-Known Good Die
Renesas Leading SiP Market

Making to high performance and the SiP technology of the application alternately pull the market growth.

Achieved Total SiP Production
100 M pieces in 2005!!

Scheduled Total SiP Production
100 M pieces in 2006!!

DSC required Small and Large Density Memory expanse Business Scale

Mobile which required smaller size accelerates Business Scale Expansion

Contribute High Speed I/F and High reliability of SiP to growth of CIS and Ubiquitous Equipment

Appear new SiP Needs for noise reduction for Printer etc...

Printer, ODD, HDD

DSC, DVC

Mobile

Renesas SiP Production Quantity
5. Renesas SiP Consistent Design System
SiP Consistent Design System

- SiP Test Design
  - SiP Test Pattern

- SiP Substrate Design
  1. Reflection, Cross Talk
     Simultaneous Switching Noise
  2. Thermal Register
  3. High-frequency Substrate Design

- SiP Functional Validation
  1. SiP Characteristics
  2. Production Reliability etc.

Total Support from System Design to Test Design

System Design → SiP Spec → SiP Design → Trial/Evaluation → Functional Validation → Mass Production

Design For SiP Configuration
- Side by Side Type
  - CPU
  - DRAM
  - SoC
  - Flash
- Stacked Type
  - FPGA
  - SoC
  - SRAM
  - Discrete

or

- CPU
- Flash
SiP integration design environment

- Design Quality Improvement
  by Electrical Characteristics Check and Verification

- Thermal Analysis
- 3D Mounting Design
- Interposer Verification
- Electrical Characteristics

SiP Floor Plan

Design DB

Common GUI

Electrical Characteristics Check

Interposer Pattern Verification

Thermal Analysis

3D Mounting
SiP Floor Plan

Our Goal:
SiP Design Which Fulfills the Performance, Power, Cost, PKG Size and Pin Numbers

- SiP Floor Plan
  1. Decision on Mounting Type (Stack Type or Side by Side Type)
  2. Decision on Chip Alignment with Considerations of Simple Substrate Pattern

Chip Alignment Inspection
- Stack Type
- Side by Side Type

Examination of Simple Substrate Pattern (1)

Examination of Simple Substrate Pattern (2)
Example of chip interconnection SI analysis result
**IR-drop Analysis Enhancing Technique**

**Examination for SiP**

- **Achievement means**
  Making Macro Model From Non-Attention Chip (RLCG+Equivalent circuit by current)

- **Action Item**
  - Chip Power Supply: Means of Making GND of Macro Model
  - Chip Power Supply: Analyzing Means of including GND of Macro Model

- **Effect**
  - Grasp achievement of chip interconnection noise spread for which Interposer is used
  - Reduction in power supply and number of GND balls in SiP PKG
SiP Simulation Cases

- Thermal Analysis Simulation
  - Analysis Model View
    - SiP (SoC + Memory)
    - Second Substrate (100 x 100 x 1.6)
  - Analysis Result (Thermal Distribution)
  - Ta: 40°C

- 3D Wire Bonding Design and Verification
  - Verification Wire Clearance by 3D Model
  - Wire
  - Upper Chip Spacer
  - Under Chip Board

- Evaluation of SiP Stress Simulation
  - SiP Simulation Model
  - Extracted BGA Specific Balls
6. Design for SiP
SoC design to consider SiP (Design For SiP)
- Realize Suitable SiP Structure ⇒ Consideration cost for SiP Design Technology -

[1] Optimization of Chip Configuration

Before Optimization

After Optimization

Spacer Needed

Spacer is no longer Needed

[2] Optimization of I/O Pad Arrangement

Before Optimization

After Optimization

Many SiP Substrate Layers
More Layers, Must use B/U Substrate

Less SiP Substrate Layers
4 or Less Layers, Able to use Glass Epoxy


Wiring on the Substrate
Long/Short Wire
⇒ Less Parasitic Components

Increase Noise
Difficulty with SI Management

• Lower I/O Electric Power
• Reduce Simultaneous Switching Noise

Better SI Management by Optimizing Buffer Drivability

[4] Embedded Test Circuit Saves the Number of External Terminals

Conventional

Embed a Test Circuit on Chips under Development

Signal Terminals Used Only in SiP
(Ex. Memory Bus)

Output Test Results
Reduce External Terminals
Input Special BIST Circuit

Output All signals
**Design for SiP**

### QFP Type SiP
- **Side by Side QFP**
- **Stack-QFP**

**<Advantage>**
- Possible to reduce assembly cost for using standard lead frame

**<Disadvantage>**
- Required SoC design for embedded memory
- Limited Quantity of Embedded Chip (about 2 chip)
- Low Wiring Flexibility

### BGA Type SiP
- **Side by Side**
- **Chip-Stack**

**<Advantage>**
- Possible to improve free wiring by multi-Substrate and electrical characteristics improvement
- Possible to optimize wiring high speed bus and power supply/GND wiring

**<Disadvantage>**
- Cost higher compared to QFP type

### <Strategy of total SiP cost reduction>
- Reduction of number of signal
  => Reduction of number of layers
- Reduction of external terminals by adopting test circuit test
- Customized SoC design for optimizing SiP structure

### <Advantage with SiP>
- Reduce design load by high-speed bus unnecessary design
- Reduce quantity of system board, size and substrate quantity
- Part arrangements simplification
SiP Test Strategy

Quality Guaranteed by RENESAS Original Testing Method

SiP System Test with Test Terminal

Test Terminal

- CPU
- ASIC
- Internal Bus
- SDRAM
- FLASH
- Renesas LSIs
- Other LSIs

Logic
- BIST for SiP

Memory
- Wafer Test
- Assembly
- Memory Test
- Logic Test
- Appearance Inspection
- Shipment
7. SiP Design Technology for High Speed I/F
Noise Problem of Speed-up and Mounting System

- **High Speed Devices**: Higher frequency operation
- **Signal System**: <Reflection / Cross Talk>
  - SI (Signal Integrity)
  - PI (Power Integrity)
- **Power Supply**: <Simultaneous switch noise>
  - EMI (Electromagnetic Interference)
- **Power Supply**: <No-need electromagnetic radiation>

Diagram:
- Driver
- Receiver
- Inter Connect
- Active bus (Simultaneous switch)
- Low Fixed Bus
- SDRAM Vth
- Voltage (V)
- Time (sec)
SiP Product Roadmap for High Speed

- SH7751R
  - 512Mbit SDRAM (x32bit) CSP 2pcs
  - Outline: 27mm x 27mm, 408pin BGA, 1.27mm Pitch, 20x20 (5row)
  - Outline: 133MHz SDRAM

- SH7780
  - 512Mbit DDR333 (x16bit) CSP 2pcs
  - Outline: 23mm x 23mm, 484pin BGA, 0.8mm Pitch, 26x26 (5row) + 10x10 (2row)
  - Outline: 333MHz DDR1

- SH-Navi
  - 512Mbit DDR667 (x16bit) CSP 2pcs
  - Outline: 29mm x 29mm, 640pin BGA, 1.0mm Pitch, 27x27 (7row) + 9x9
  - Outline: 667MHz DDR2
SiP Solution for High Frequency System

DDR System Solution Business Proposal by Renesas Original Technology

Customer’s Development Term Reduction for Complicated DDR I/F Design
Reducing Mounting C/R Number and Customer Board Size

EMI Noise Reduction
Switching Noise Reduction

Renesas Supports Memory

Reduce System Power Consumption

Total Cost Reduction, Improve Performance
Easy DDR System Design by SiP

Renesas SiP makes customer free from the design of complicated DDR I/F

Almost all devices can be removed with SiP solution. Then, customer does NOT need to care about:
- Complicated design of DDR I/F
- Device count and board size reduction
- Power dissipation on each resistor and regulator

Discrete System

SiP System
Total System Cost Advantage of SiP DDR

- Substrate Cost
- Board Size
- Cost
- Performance

CPU SDRAM
- DDR System
- SiP Solution
- PCB 10 Layers!!
- 250 cm² Reduction

Customer’s Board
- PCB 12 Layers

SDRAM System
- SDRAM
- DDR
- C/R

PKG Solution
- PCB 14 Layers

SiP
- Cost
- Performance
The strengths based on DDR-System

- Reduction of Resistance of DDR IF Series and Terminate Resistance
  * The Optimization Design of SiP Reduces series resistance and the terminator.
  * A high-speed design of DDR IF is unnecessary.

- Effect of electric power decrease
  * The power consumption of DDR IF can be decreased.
  * Half the output electric power of DDR can be decreased by the drivability control.
  * The power consumption of the regulator of VTT can also be decreased.

Power Comparison

![Diagram showing Discrete System vs. SiP System]

- Reduce Power Consumption of DDR I/F Power
- Celler - DSC Field
- Graphic - DTV Field
- CIS Field
SiP can save Customer's Total System Cost

Discrete Solution
- CPU
- Memory
- Customer’s Board
  - Board Cost
  - Assembly Cost
  - Manpower Cost
  - Procurement Cost
  - Development Term … etc.

SiP Solution
- Assembly
- CPU (Bare Die)
- Memory (Bare Die)
- Customer’s Board

System Components Cost

Customer’s Total Cost

SiP can save Customer’s Total System Cost
8. SiP Mounting Technology
Required Memory size by Application

- **Stack Type**
  - Miniaturization
  - High density mounting

- **Side by side**
  - High reliability
  - High radiation
  - Low noise
  - High Frequency

- **Number of Memory**
  - 4 chip
  - 2 chip
  - 1 chip

- **SDRAM Capacity**
  - 2 G
  - 1 G
  - 512 M
  - 256 M
  - 128 M
  - 64 M
  - 32 M
  - 16 M

- **Package External Dimensions (mm)**
  - 10 12 14
  - 16 18 20 22 24 26 28 30 32 34

- **Applications**
  - Mobile
  - DSC
  - DVC
  - Amusement
  - PRINTER
  - DTV/DVD
  - ODD/HDD

- **QFP**
Technology to realize miniaturize and high quality

- Applied the result of the top-level world research to the mounting technology.
- Support from design to mass production by mounting technology as the ITDM manufacturer.

~ Realization of small size/high density SiP by FC technology + WB technology ~

**Wafer super thin grinding technology**
- 300mm wafer super thin processing technology
  - 90 µm mass production
  - 50~70 µm under development
  - Same processing level as 200mm wafer

**Wire bonding connection**
- Long wire formation
- Super low loop wire formation
- Narrow pitch wire bonding tech.
  - 50 µm pitch under mass production

**Board Technique**
- Thin board technique, low warpage substrate technology

5 layer solution for DSC
The Trend of FC (flip chip) Technology

Au Solder connection technology

Effect of FC mounting technology development road map

Structure of SiP

View of Connected section

- 256MSDRAM
- 256MFLASH
- ASIC

Chip
Resin
Solder
Substrate Electrode

Au Stud Bump

Pad Pitch (µm)

- 60 µmPitch
- 50 µmPitch
- 40 µmPitch
- 35 µmPitch
- 40 µmPitch (Stagger '06)
- 35 µmPitch (Stagger '07)
- 40 µmPitch

Narrow Pitch FC Tech.

- 90 µmPitch
- 80 µmPitch
- 70 µmPitch
- 60 µmPitch
- 50 µmPitch
- 40 µmPitch
- 30 µmPitch
- 20 µmPitch

Year:
- '03
- '04
- '05
- '06
- '07

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Renesas SiP Highly Reliable Flip-Chip Connection Technology

~ RENESAS Original Highly Reliable Technology by WPP Technology ~

WPP (Wafer Process Package) Technology

- Realized Real Chip Size Package
- Reduced Resistance \(\text{Inductance, the best for High-Speed Device}\)
- Improvement of Connected Reliability with soldered joint
- Executed Test/Burn In to each chip, and make possible The High Reliability Guarantee

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QFP
- 28mm x 40mm
- 65% Down

P-BGA
- 21mm x 21mm
- 75% Down

WPP
- 10.7mm x 10.32mm

SiP For CIS

Renesas SiP Highly Reliable Flip-Chip Connection Technology
Super Thin Stack SiP Trend

Trend of Package Height

~ For Large Capacity, High-Density Mounting ~

<table>
<thead>
<tr>
<th>Year</th>
<th>2004</th>
<th>2005</th>
<th>2006</th>
<th>2007</th>
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</thead>
<tbody>
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<td>Unit (mm)</td>
<td>2.0</td>
<td>1.5</td>
<td>1.0</td>
<td>0.5</td>
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</tbody>
</table>

Required Technology Development

300 mm wafer ultra thin processing technology, thin substrate technology, and super-low loop wire bonding technology, narrow pitch FC die-attach technology

Development of thinness substrate**
Si hole-through electrode technology

*Under Development
BG(Back Grind) Processing Technology and DB Technology Development Roadmap

~ To Realize high density multiple memories, miniaturization ~

Action Item

- Chip flexure strength
- Gettering effect

Graph showing trends in chip thickness and flexure strength, with various technologies highlighted:
- Edge Trimming Technology
- Wafer Support Technology
- Laser Dicing Technology
- Film DB Technology

Formula:

\[ M = \frac{3P}{bh^2} \]

Polish Finish
- Poli Graind
- B.G(#2000)

Graph scales:
- Chip Thickness: 50, 100, 150, 200 µm
- Flexure strength: 0, 50, 100, 150, 200, 300, 400, 500 gf
Road Map of Wire Bonding Technology

~ For Achieving Complicated Wire Formation ~

Action Items
- Bonding suiting accuracy
- Au Wire Filamentation processing
- Bonding Strength
- Electric Characteristics

Wire Diameter (µm)
- 60 µm
- 50 µm
- 40 µm
- 35 µm
- 30 µm
- 25 µm
- 20 µm
- 17 µm
- 15 µm
- 12 µm
- 10 µm

Pad Pitch
- '00
- '01
- '02
- '03
- '04
- '05
- '06
- '07
- '08
- '09
- '10

Chip To Chip Development

Long Loop Formation

Resistance
- Wire pull strength
- L: 1.2nH/mm

Au Wire Diameter (µm)
- 60 µm
- 50 µm
- 40 µm
- 35 µm
- 30 µm
- 25 µm
- 20 µm
- 17 µm
- 15 µm
- 12 µm
- 10 µm

Bonding Strength (gf)

Electric Characteristics (mΩ/mm)

Road Map of Wire Bonding Technology Development

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**Thin Wafer Pick-Up Technology**

~ Examination of picking up technology with supersonic wave ~

**Benefit of Supersonic Wave**

Even Thin Chip can be effective to produce

*Good for Super-thin type Stack technology*
9. Stack SiP Development Trend
Spacer less Technology**

** Under Development

Decrease Mounting Constraint and Multi Stack Technology by increased Stack LSI

Spacer less technology

(No Spacer)
WB+WB

(Large chip size constraint)

(Need Spacer)
WB+WB

• Need chip size constraint
  (Overhang constraint)
• Increase spacer additional work
• No-need Center pad parts

FC+WB

Required substrate such as Built-up for a high density small size/mounting
Thin SiP substrate**

Sample Structure

Coreless substrate: Thickness less than 0.1~0.2mm (Current Products 0.4mm)

Advantage

- Suitable for thin/small products such as mobile or HDD/ODD

** Under Development
LSI embedded substrate SiP**

Sample Structure

Realize thin type by embedded SoC in the substrate and FC connected SDRAM

Advantage

- Available for system black box such as security field
- Possible to make high density memory

** Under Development
PoP (Package on Package) Technology**

- **Sample Structure (mold/FC type PoP)**

- **Sample Structure (substrate LSI buried type PoP)**

Using LSI embedded technology for lower substrate

**Under Development**

- **Advantage**
  - Variable memory capacity/supplier
  - Possible for memory shrink
10. Next Generation SiP Technology (CoC Technology)
Benefits of CoC Technology (Chip on Chip)

- Interchip High-Speed Data Transfer
  (CPU-Memory etc.)
- Various kinds device consolidation SiP
- Process Consolidation of Various generation
  (maturity + point)
- High density mounting
- Thin making multi chip accumulating PKG

- When Base Chip is global wiring Chip
  - Minute wiring is unnecessary
    - Low Cost and Low resisted.
- When Base Chip is LSI Chip
  - mass memory installable
  - Global wiring short able
    - Improved Switching Characteristics
  - Unnecessary output buffer
    - Reduced Power consumption
  - After installed Base Chip, it can be tested.
Minute pitch connection for CoC Technology

Solder bump formation
(Exhalation method of Micro meltdown)

Macro Meltdown Solder exhalation device outline
(Solder Shoot)

Cross section after connected
(30\(\mu\)m pitch connection)

CoC (Chip on Chip) Connection COC(10,000bump)
Technology of Chip to Chip

- Substrate NET Reduction by LSI Development only for SiP
- For High-speed Operation
  (Improvement of data Transfer rate)
- Digital and Analog Separation (Point SoC Achievement by SiP)
11. Next Generation SiP Technology (Si Hole-through Technology) ~ Technology for Ultra thin multi stack SiP ~
Development of Si Hole-through connection Technology**

- 3-D SiP by Si hole-through Connection Technology

**Under Development**

- Advantage
  - Connect chip interconnection at standard temperature by caulking technique
  - Thickness of Stack SiP PKG is reduced by half
SiP Product TEG with Si hole-through Connection**
~ High Density SiP Technology by 3D Multi Stack ~

- Low Cost 3D Silicon Multi SiP Process
  Cost for Through Electrode Formation with Standard
  Temperature Chip interconnection with Caulking Method -> 70%

Room temperature chip to chip interconnection
using caulking technique

**Under Development

Silicon Multi Stack SiP

Silicon Multi Stack SiP Cross Section
Realize Small/Think making
with Si hole-through connection**

WB Multi Stack SiP
under mass production

Si hole-through
electrode multi stack SiP

- Package Thickness: 1.25mm
- Package Board: 6 layer (t=0.46 mm)
- Wire Length: Long
- Resin-sealed Required

- Package Thickness: 0.5mm
- Package Board: 2 Layer (t=0.2 mm)
- Wire Length: Shortest (WB-less)
- Resin-sealed Not-required

**Under Development
SiP Roadmap

**QFP Type**

- Existing Package Support
- Support for New Application Fields

**2 or 3 Layer Stack**

- Super-small, Ultra-thin Type
- Miniaturization for Digital Consumer Cellular Phone, DSC, DVC, etc.

**Stack Type**

- 5 Layer/Multi Layer

**Side by Side**

- High-performance High Speed I/F

**Next-generation ultra small 3D Mounting Technology**

- Chip on Chip Technology
- Through Hole Electrode Technology

- IC included

**Side by Side High Speed (H.S Side by Side)**

- H.S Side by Side
- CIS
- Telematics
- Network

- High Reliability/Radiation

- Under Development