「低電力CMOS設計の秘訣とテクニック」

Tips and Techniques for Low Power CMOS Design

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Optimize and control V_{DD} and V_{TH}

Means to Maintain Throughput at Low V_{DD}

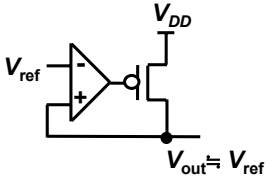
- **Parallel / Pipeline (circuit can be slow)**
  - Good for signal processing, but at the cost of area penalty
- **Lowering V_{TH} to recover circuit speed (circuit should be fast)**
  - Speed requirement changes from time to time
  - Variable V_{DD}, Variable V_{TH}
- **Utilizing surplus timing (some circuit should be fast, others can be slow)**
  - Speed requirement differs from circuits to circuits
  - Multiple V_{DD}, Multiple V_{TH}

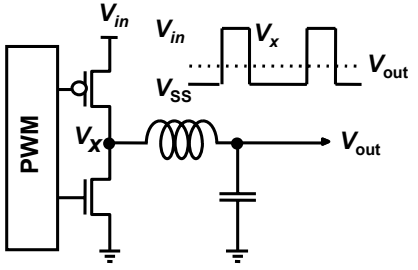
➢ **It is essential to control V_{DD} and V_{TH} for low-power, high-speed circuit design.**

Ref. [1]

Controlling V_{DD} by Circuit

- **Series regulator**
  - + easy to integrate
  - - low efficiency ($\eta < V_{out}/V_{DD}$)
- **DC-DC converter (switching regulator)**
  - + high efficiency ($\eta = \sim 0.9$)
  - - off-chip L, more pads

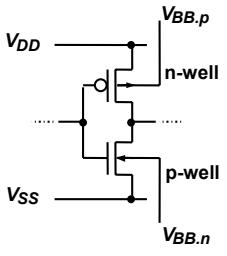


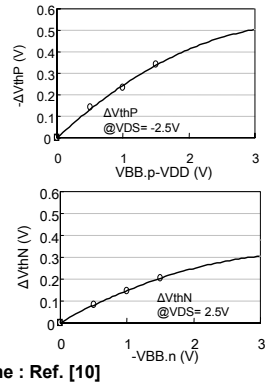


η=0.95: Ref. [2]
Switching noise: Ref. [3][4]

Controlling V_{TH} by Circuit

■ **Substrate bias (body effect)**

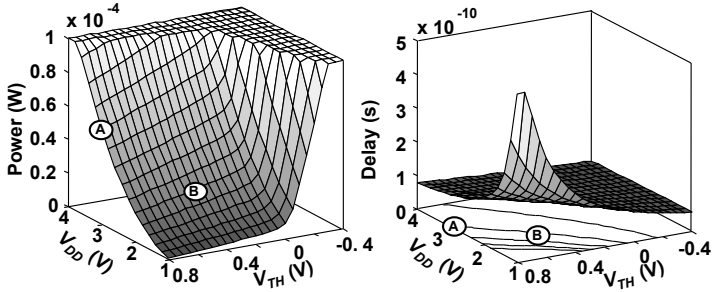




VTCMOS : Ref. [5]-[8]
FTCMOS : Ref. [9]
Switched Substrate-Impedance Scheme : Ref. [10]
Sa-VT CMOS : Ref. [11]

Trade-offs between Power and Delay

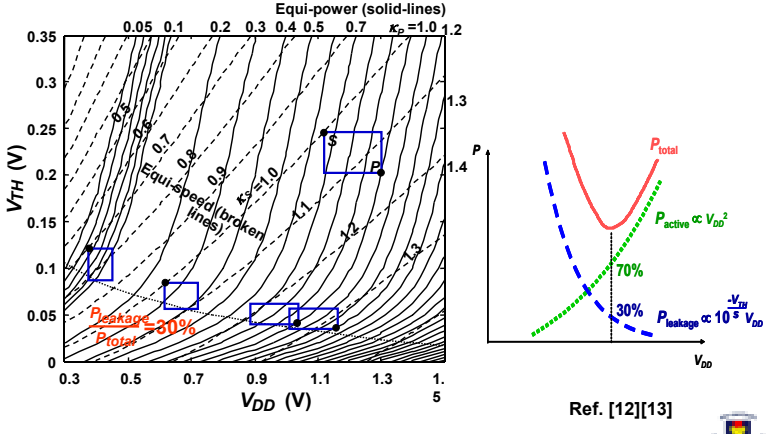
Power : $P = p_t \cdot f_{CLK} \cdot C_L \cdot V_{DD}^2 + I_0 \cdot 10^{-\frac{V_{TH}}{S}} \cdot V_{DD}$ **Delay :** $D = \frac{k \cdot C_L \cdot V_{DD}}{(V_{DD} - V_{TH})^{1.3}}$



■ **Power is reduced while delay is unchanged if both V_{DD} and V_{TH} are lowered such as from A to B.**

Ref. [1]

Total Power is Min. When $P_{leakage}/P_{active}$ = 30/70



Ref. [12][13]

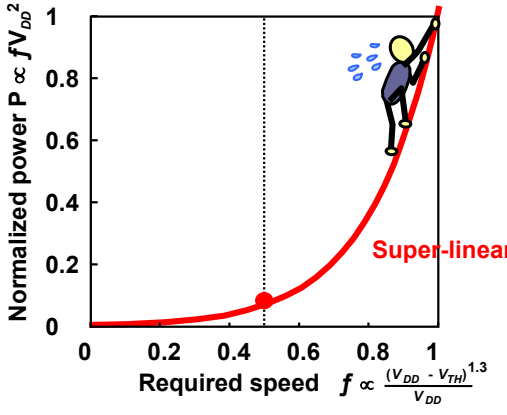
Tip 2

Total power is minimum when $P_{leakage}/P_{active}$ is 30/70.

Tip 3

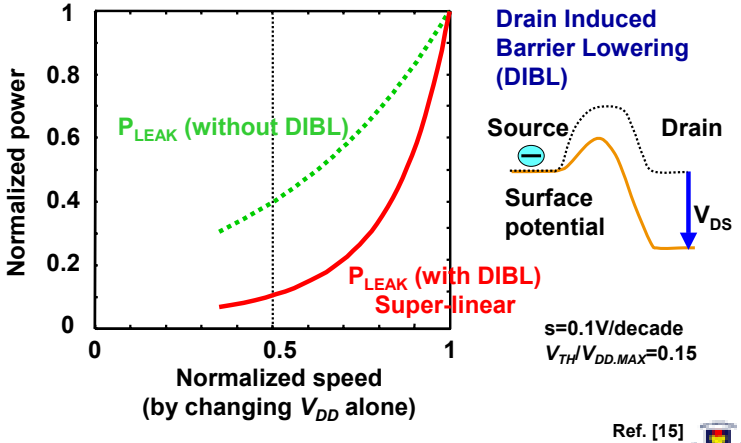
If you don't need to hustle, relax and save power.

Dynamic Power Reduction



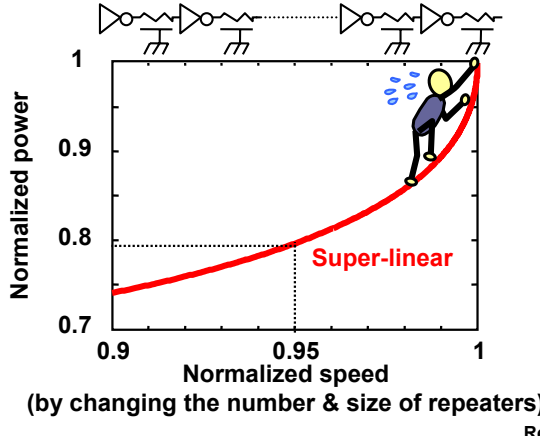
Ref. [14]
Courtesy Prof. T. Sakurai, U. of Tokyo

Active Leakage Power Reduction



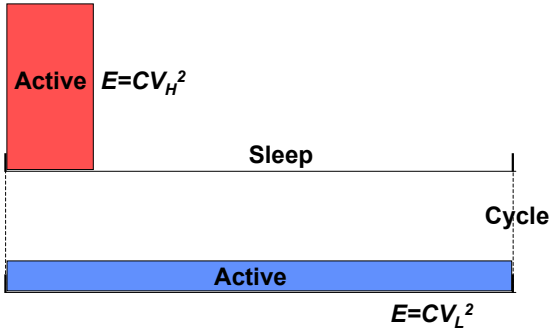
Ref. [15]
Courtesy Prof. T. Sakurai, U. of Tokyo

Power-Delay Optimization for Interconnects



Ref. [16]
Courtesy Prof. T. Sakurai, U. of Tokyo

Work As Slowly As Possible before Working Hastily for Taking A Break

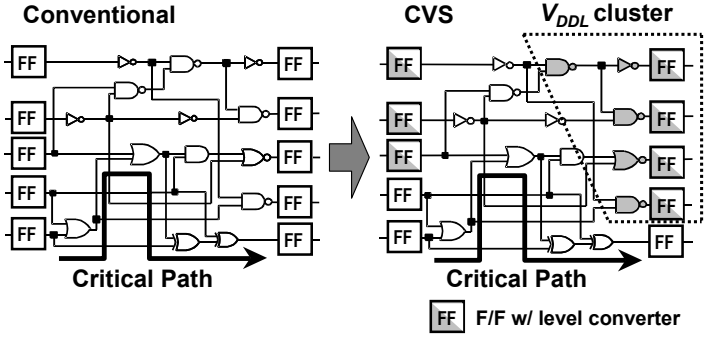


Tip 4

Utilize surplus timing

with multiple V_{DD}'s and V_{TH}'s

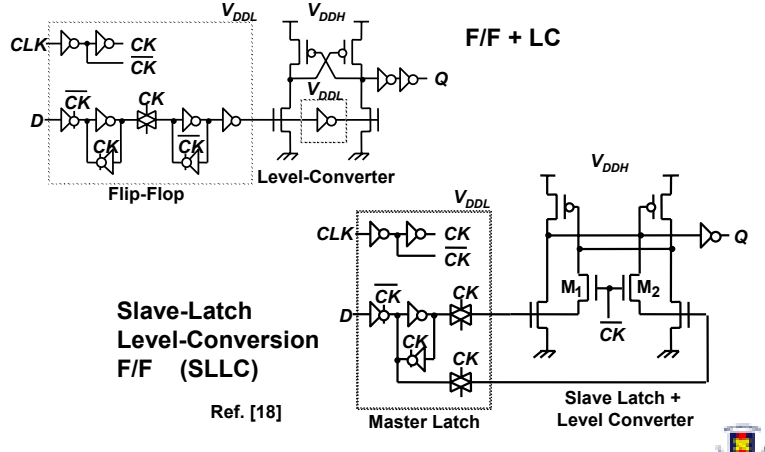
Clustered Voltage Scaling



- Minimize penalties associated with level converters.

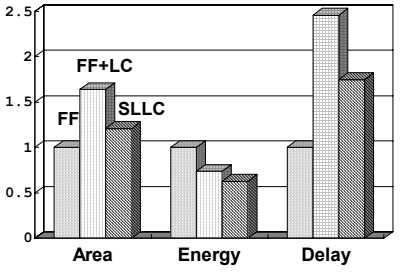
Ref. [17]

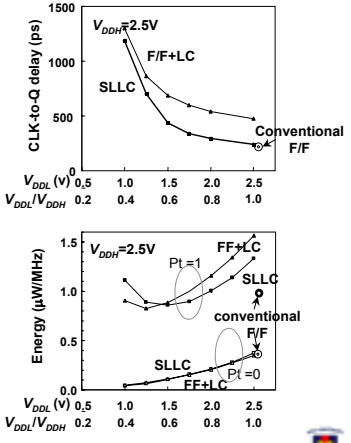
Flip-Flop with Level Converter



Ref. [18]

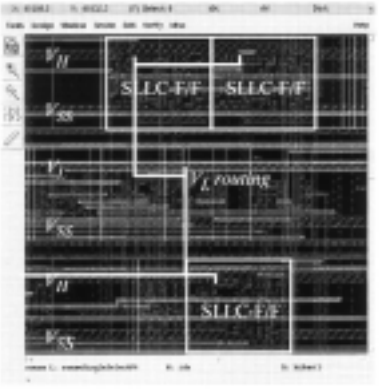
Area, Energy, Delay Comparison





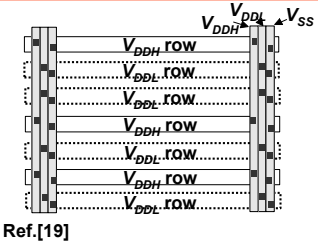
SLLC Layout

- SLLC is placed in V_{DDH} row.
- V_{DDL} is provided from an adjacent V_{DDL} row by a signal interconnection.
- Clock trees are placed in V_{DDL} to reduce power for clock distribution.



Row-by-Row V_{DD} Assignment

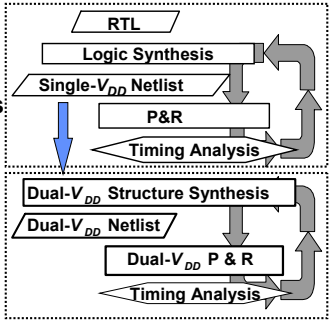
- Mostly compatible with conventional layout, and hence, no penalty.
  1) A single pair of power supply lines for each cell row.
  2) Existing cell layout in a library can be utilized for both V_{DDH}- and V_{DDL}-cells without modification.



- Row assignment algorithm for EDA ... Ref.[19]
  1) Conventional P&R for single V_{DD}.
  2) Total area of V_{DDL}-cells is computed and accumulated on the downward path in the cell rows.
  3) When the accumulated V_{DDL}-cell area exceeds an average total cell area per row, one of the rows is selected as the V_{DDL} row such that the total distance of cell movement is minimized.
  4) Steps (2)-(3) are carried out repeatedly from top to bottom.

Design Flow

- Design flow:
  1) Conventional design for V_{DDH}
  2) Partition circuits for V_{DDH} and V_{DDL}
  3) Modify P&R for non-critical circuits (Floorplan and critical path design are preserved.)
- Advantages:
  1) Small penalty in design time
  2) Minimum addition to the conventional design methodology

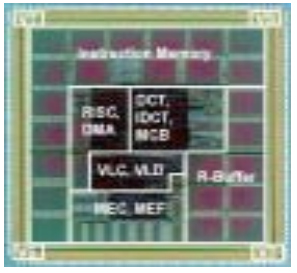


Ref. [19]

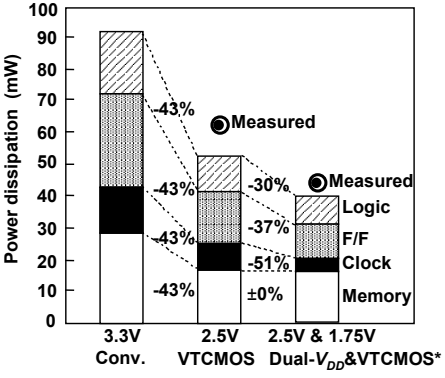
Design Example

MPEG-4 Video Core

- QCIF 10fps Codec @ 30MHz
- 0.3μm CMOS
- 3 million transistors
- 9mm x 9mm
- Three designs
  1) Conventional design at 3.3V
  2) 2.5V design with V_{TH} control by VTCMOS ... Ref. [6]
     0.2V ± 0.05V @ active
     0.5V ± 0.05V @ standby
  3) Dual-V_{DD} (2.5V, 1.75V) design in VTCMOS ... Ref. [18]

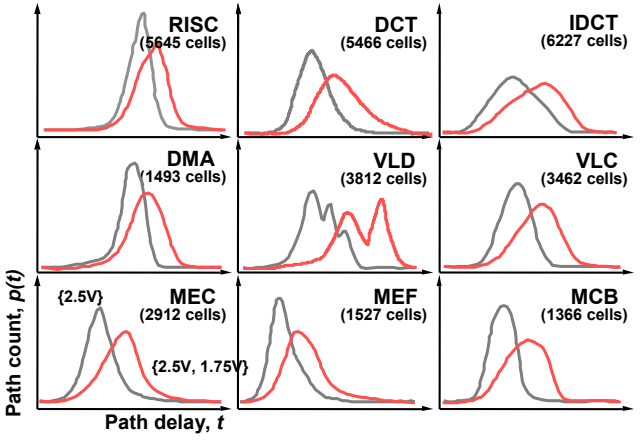


Design Results

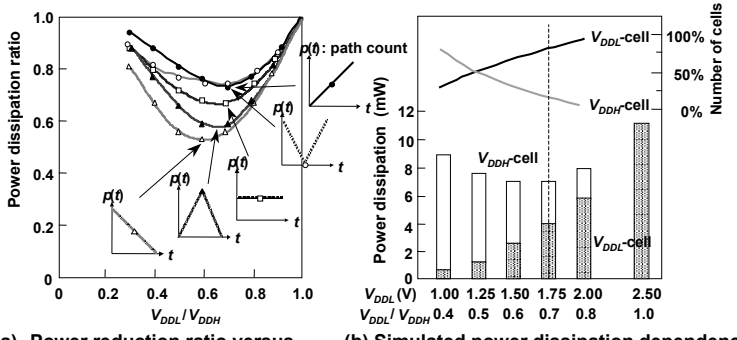


* Additional 3 weeks in design time
* <5% area increase for logic circuits

Path-Delay Distribution



Optimum V_{DDL}/V_{DDH}



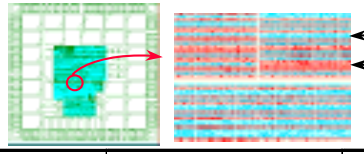
(a) Power reduction ratio versus V_{DDL}/V_{DDH} calculated from theory.

(b) Simulated power dissipation dependence on V_{DDL}/V_{DDH} in DCT block (5466 cells) .

- Rule of thumb: V_{DDL}/V_{DDH}=0.6~0.7 minimizes P_{total}.

Ref. [20]

Dual-V_{DD} Layout Results



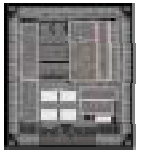
F/F: SLLC-F/F, LC: Level-Converter

	Cell number				Cell area (mm^2)		Row number	
	V_{DDH}-row V_{DDH}-cell	F/F	LC	V_{DDL}-row V_{DDL}-cell	V_{DDH}-row	V_{DDL}-row	V_{DDH}-row	V_{DDL}-row
RISC, DMA	2451	1247	251	4687	0.70	0.42	67	41
DCT, IDCT, MCB	2364	1767	148	10695	0.85	0.89	53	55
VLD, VLC	1389	634	85	5885	0.50	0.73	21	31
MEC, MEF	845	723	6	3594	0.37	0.39	22	24
Total (%)	7049 (19%)	4371 (12%)	490 (1%)	24861 (68%)	2.42 (50%)	2.43 (50%)	163 (52%)	151 (48%)

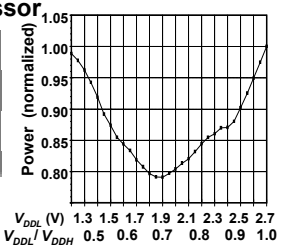
- V_{DDL}/V_{DDH}=0.7 balances numbers of V_{DDL}/V_{DDH} rows.

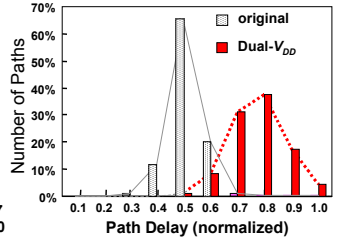
Another Example

Media Processor



Ref. [19]





- **Original design :**
  V_{DD}=2.7V
  75MHz
- **Dual-V_{DD} design :**
  V_{DDL}/V_{DDH} = 1.9V / 2.7V (= 0.7)
  75MHz
  Power reduced by 47% (76% cells at V_{DDL})

Tip 5

Total power is minimum when V_{DDL} / V_{DDH} =0.7

Multiple V_{DD} Theory

Ref. [21]

For single power supply (V_1)

$$P_1 = f \cdot C_1 \cdot V_1^2 \quad (1)$$

For multiple power supplies (V_1> V_2 >…> V_n)

$$P_n = f \cdot \left\{ \left(C_1 - \sum_{i=2}^{n} C_i \right) \cdot V_1^2 + \sum_{i=2}^{n} C_i \cdot V_i^2 \right\} \quad (2)$$

where C_i is total capacitance of gates that operate under V_i.

Power ratio is

$$R \equiv \frac{P_n}{P_1} = 1 - \sum_{i=2}^{n} \left[\left(\frac{C_i}{C_1} \right) \cdot \left\{ 1 - \left(\frac{V_i}{V_1} \right)^2 \right\} \right] \quad (3)$$

Delay and capacitance is mostly in proportion (evidence is in the next two foils),

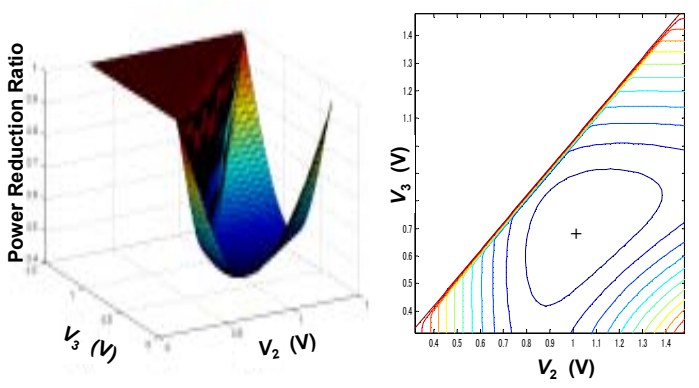
$$\frac{C_i}{C_1} = \frac{\int_0^1 p(t) \cdot t_i \cdot dt}{\int_0^1 p(t) \cdot t \cdot dt} \quad (4)$$

where $p(t)$ is a path-delay distribution function

$$\int_0^1 p(t) \cdot dt = 1 \quad (5)$$

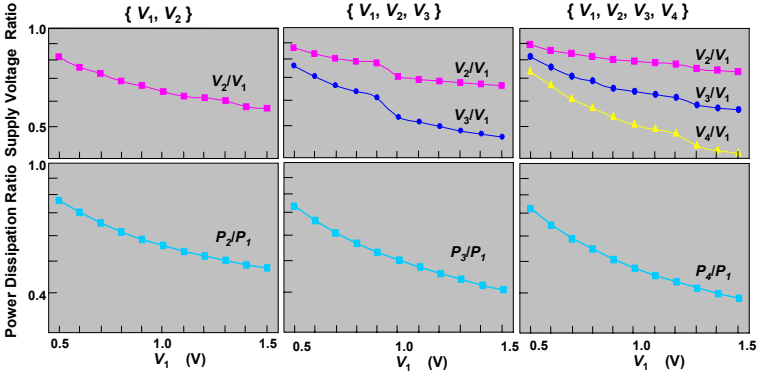
and t_i is total delay of gates at V_1 that will operate under V_i.

Three V_{DD}'s



V_1 = 1.5V, V_{TH} = 0.3V, $p(t)$:lambda

Optimum Numbers of Supplies



- The more V_{DD}'s, the less power, but the effect will be saturated.
- Power reduction effect will be decreased as V_{DD}'s are scaled.
- Optimum V_2/V_1 is around 0.7.

Multiple V_{TH} Theory

Ref. [21]

For single V_{TH} ($V_{TH.1}$), chip leakage current is

$$I_1 = \left(\frac{I_0}{W_0}\right)\cdot W_1 \cdot 10^{-\frac{V_{TH.1}}{S}} \quad (1)$$

For multiple V_{TH} ($V_{TH.1} < V_{TH.2} < \ldots < V_{TH.n}$)

$$I_n = \left(\frac{I_0}{W_0}\right)\cdot\left\{\left(W_1 - \sum_{i=2}^{n} W_i\right)\cdot 10^{-\frac{V_{TH.1}}{S}} + \sum_{i=2}^{n} W_i \cdot 10^{-\frac{V_{TH.i}}{S}}\right\} \quad (2)$$

where W_i is equivalent total gate width under V_i.

Chip leakage current ratio is

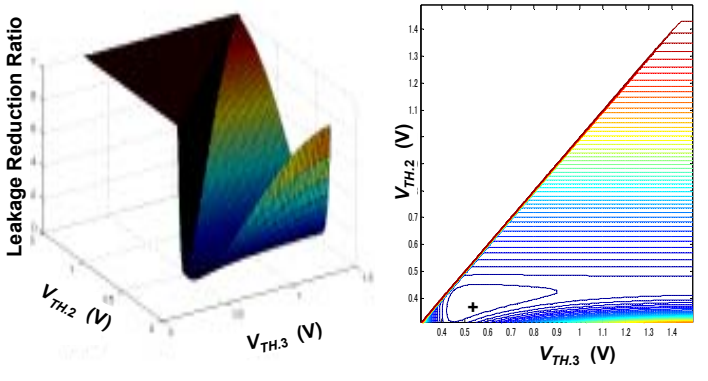
$$R \equiv \frac{I_n}{I_1} = 1 - \sum_{i=2}^{n}\left[\left(\frac{W_i}{W_1}\right)\cdot\left\{1 - 10^{-\frac{V_{TH.i}-V_{TH.1}}{S}}\right\}\right] \quad (3)$$

Delay and the equivalent total gate width is mostly in proportion (evidence in the next foil)

$$\frac{W_i}{W_1} = \frac{\int_0^1 p(t)\cdot t_i \cdot dt}{\int_0^1 p(t)\cdot t \cdot dt} \quad (4)$$

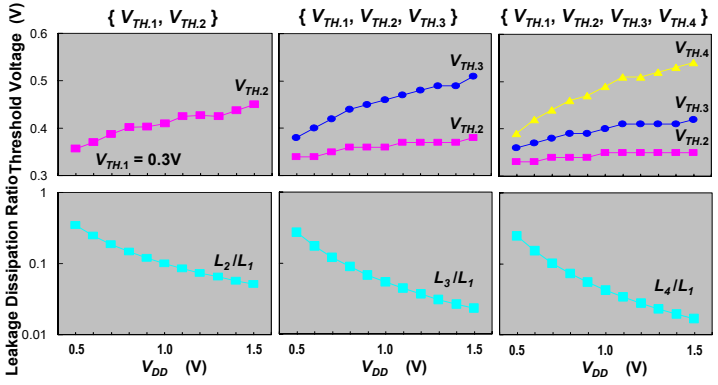
The chip leakage ratio can be computed in the same way as in the power dissipation under multiple V_{DD}.

Three V_{TH}'s



V_{DD} = 1.5V, $V_{TH.1}$ = 0.3V, $p(t)$:lambda

Optimum Numbers of Thresholds



- At V_{DD}=1.5V, % of circuits in $V_{TH.1}$, …, $V_{TH.4}$ is 0.4%, 3%, 11%, 85%.
- The more V_{TH}'s, the less leakage, but the effect will be saturated.
- Leakage reduction effect will be decreased as V_{DD} are scaled.

Tip 6

Two types are sufficient

(Dual V_{DD}'s, dual V_{TH}'s)

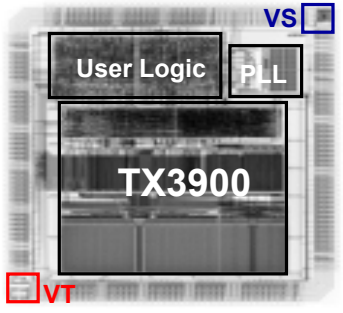
Tip 7

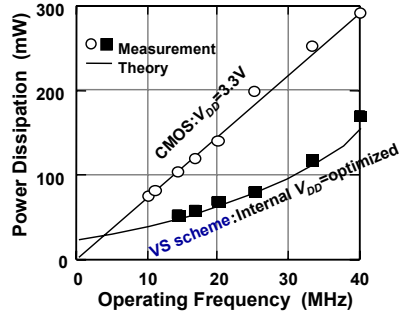
Adapt to the change

with variable V_{DD} and V_{TH}

Dynamic Voltage Scaled Microprocessor

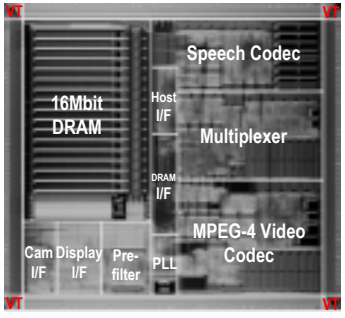
External V_{DD} 3.3V±10%
Internal V_{DDL} 0.8V~2.9V ±5%

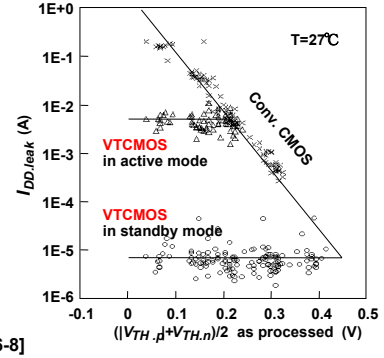




Variable Supply-voltage scheme : Ref [22]
MIPS3900 ('97) : Ref [22]
ARM8 ('00) : Ref [23]

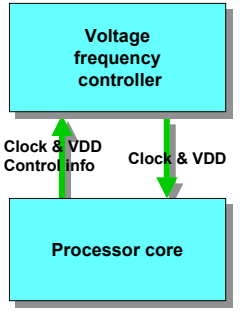
Body Bias Controlled Processor

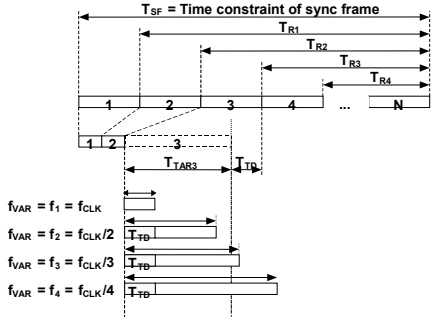




Variable Threshold-voltage CMOS : Ref [6-8]
MPEG-4 Codec : Ref [18][24]
SH-4 : Ref [10]

V_{DD}-Hopping in Real-Time Applications

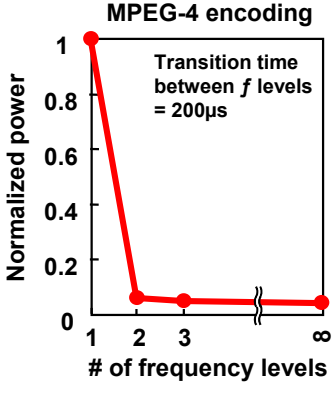


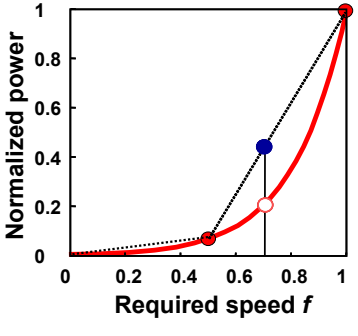


- **Application slicing and software feedback guarantee real-time operation.**

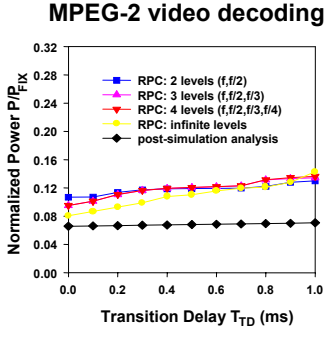
Ref [25][26]
Courtesy Prof. T. Sakurai, U. of Tokyo

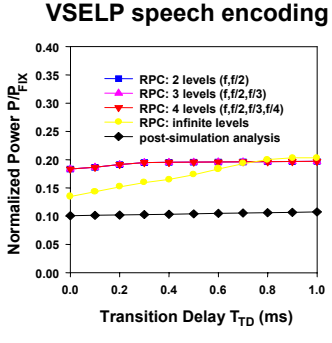
Two Hopping Levels Are Sufficient





Changeover Time Makes No Difference



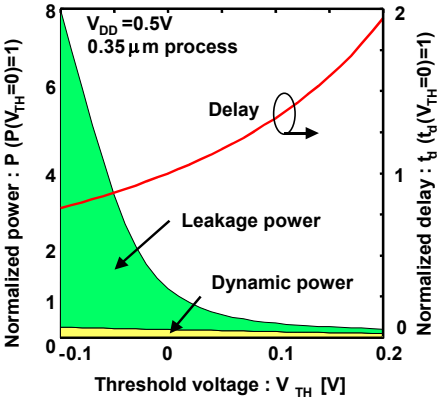


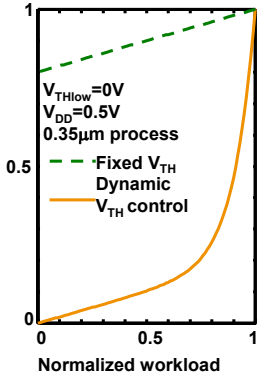
Tip 8

Two hopping levels are sufficient

(*f*, *f*/2)

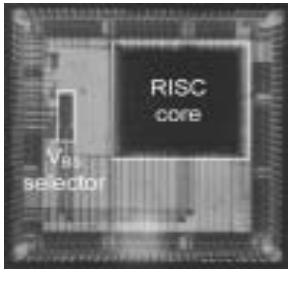
V_{TH}-Hopping



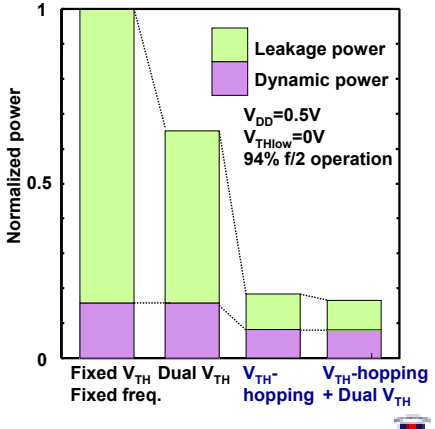


Ref [29]
Courtesy Prof. T. Sakurai, U. of Tokyo

Experimental Results with RISC Processor



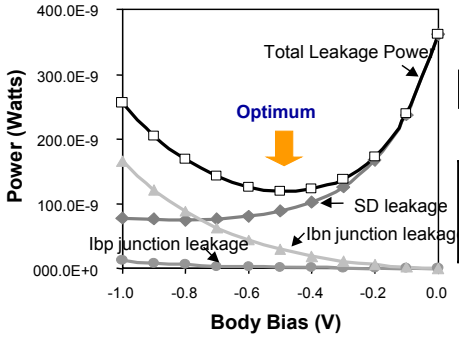
0.6μm process
Overhead of V_{TH}-hopping : 14%
RISC core : 2.1mm x 2.0mm
V_{BS} selector : 0.2mm x 0.6mm



Tip 9

Cooperate across various levels of design hierarchy

Scalability of Reverse Body Bias



Total Leakage Power Measured on Test Chip

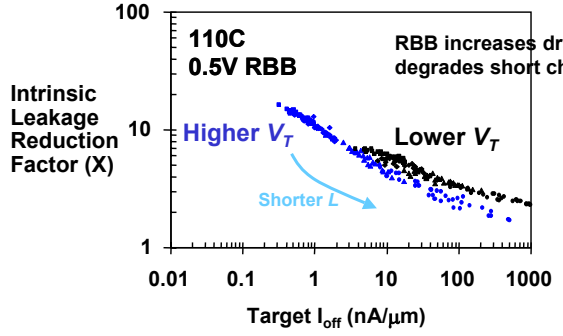
0.18 μm

Tech	0.35 μm	0.18 μm
Opt. RBB	2V	0.5V
Ioff Red.	1000X	10X

■ **RBB less effective with technology scaling**

Ref [30]
Courtesy Intel Labs.

Effectiveness of Reverse Body Bias

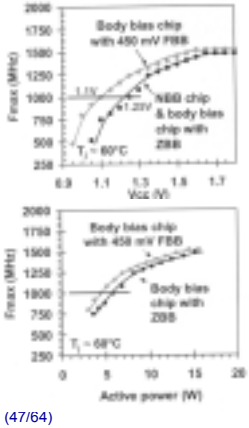


■ **RBB less effective at shorter *L* and lower V_{TH}**

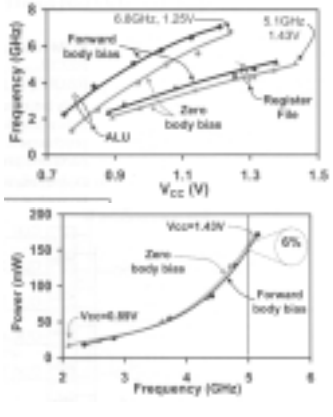
Ref [31]
Courtesy Intel Labs.

Forward Body Bias

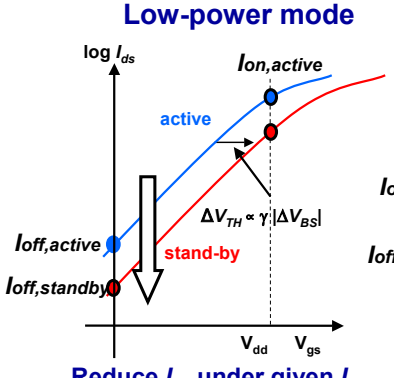
■ **1GHz Router Chip** Ref [32]

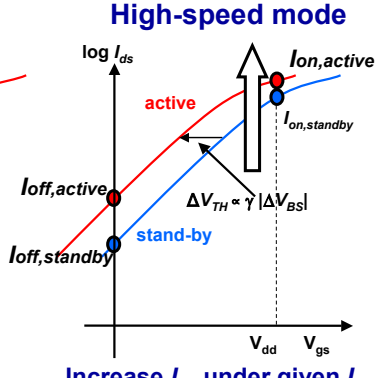


■ **5GHz 32b Integer-Execution Core** Ref [33]



Two Modes in VTCMOS





Tradeoff Associated with γ

given I_{off}

$\gamma \uparrow$ ($N_A \uparrow$)

- $\Delta V_{TH} \uparrow$ (body effect) → $I_{on} \uparrow$ → $|V_{BB}|>V_O$
- S-factor $\uparrow$ ($C_{ox}/C_D \downarrow$), $g_m \downarrow$ → $I_{on} \downarrow$ → $|V_{BB}|<V_O$

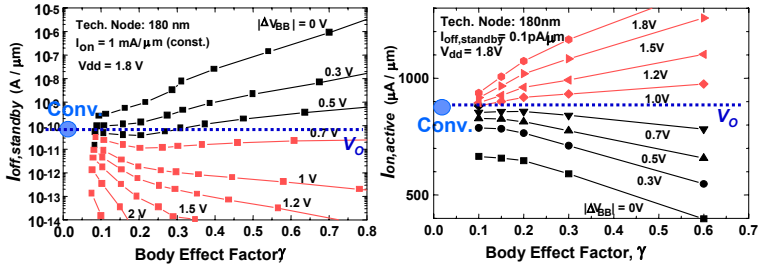
tradeoff … V_O

■ Larger γ is better as long as $|V_{BB}|>V_O$

180nm node

Low-power mode (constant $I_{on,active}$)

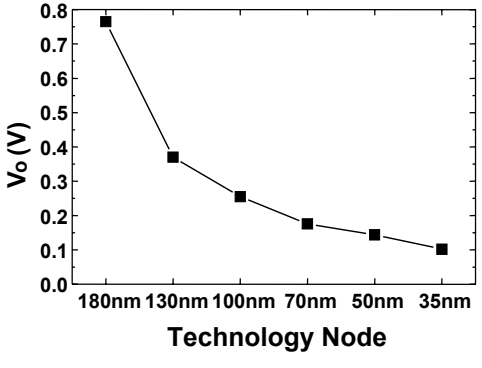
High-speed mode (constant $I_{off,standby}$)



■ VTCMOS is effective as long as $|\Delta V_{BB}| > V_O$ (V_O = 0.5 ~ 1V < V_{DD})

Ref. [34][35]
Courtesy Prof. T. Hiramoto, U. of Tokyo

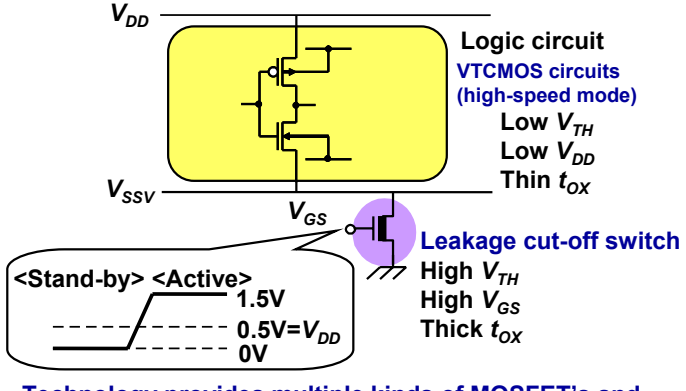
V_o Scaling in High-Speed Mode



■ VTCMOS will be effective in high-speed mode

Ref [36]

Technology-Circuit Cooperation



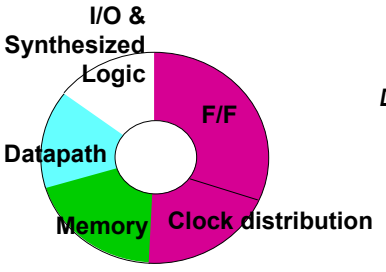
■ Technology provides multiple kinds of MOSFET's and designers make use of the gift.

Ref [37]

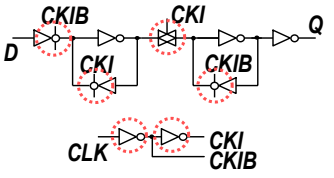
Tip 10

Right circuit for the right job

Clock Induced Power Dissipation in F/F



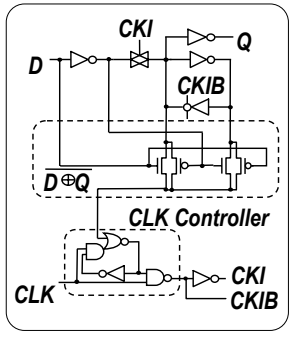
High-end μP

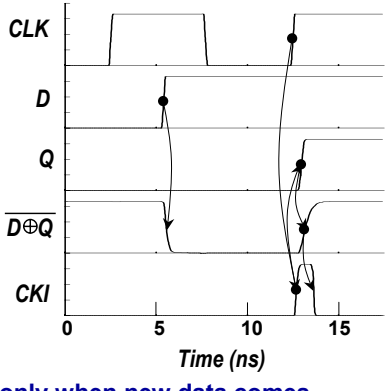


12 / 24 transistors dissipate power for clocking even without no new data

Conditional Flip-Flop

Clock-on-Demand (COD) F/F

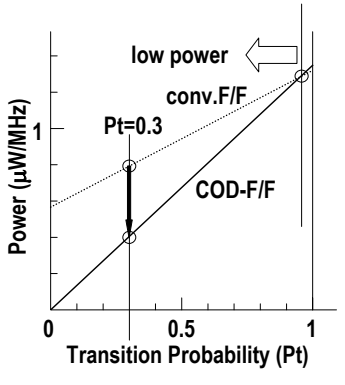




- **Clock is provided to F/F only when new data comes.**

Ref [41]

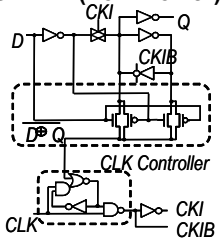
COD-F/F: Low Power



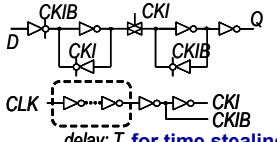
- **Advantage**
  + Low power
- **Penalty**
  - Area increase by 12%
  - Set-up time increase

Highlight One's Good Point

COD-F/F (Low Power)



NS-F/F (High Speed)



delay: T for time stealing

	Power (μW/MHz)	C-to-Q (ns)	Setup (ns)	Hold (ns)	Area (μm²)
Conventional	0.78 (1.0)	0.35 (1.0)	0.14	-0.12	202 (1.0)
COD-F/F	0.34 (0.4)	0.49 (1.4)	0.90	0.46	202 (1.0)
NS-F/F#1	1.21 (1.6)	0.81 (2.3)	-0.32	0.34	259 (1.3)
NS-F/F#2	1.90 (2.4)	1.55 (4.4)	-1.06	1.08	274 (1.4)
NS-F/F#3	1.68 (2.2)	1.69 (4.8)	-1.20	1.22	288 (1.4)
NS-F/F#4	1.72 (2.2)	1.99 (5.7)	-1.50	1.52	302 (1.5)

F/F Blending : Create A Best Mix of the Advantages

DCT design	Conv.	Low Power	High Speed
Power (mW/MHz)			
random picture	1.18 (1.0)	0.88 (0.8)	1.47 (1.2)
still picture	0.68 (1.0)	0.33 (0.5)	1.01 (1.5)
Min. cycle time (ns)	12.46 (1.0)	12.46 (1.0)	9.99 (0.8)
Area (mm²)	0.61 (1.0)	0.69 (1.1)	0.71 (1.2)

F/F type	Conv.	Low Power	High Speed
Conv.	711	158	270
COD-F/F	-	553	-
NS-FF : setup time			
#1 : -0.32	-	-	49
#2 : -1.06	-	-	143
#3 : -1.20	-	-	71
#4 : -1.50	-	-	178

Ref [41]

Summary

Tip 1: Optimize and control V_{DD} and V_{TH}.
- Trade-offs between power and delay are given by V_{DD} and V_{TH}.

Tip 2: Total power is minimum when $P_{leakage}/P_{active}$ = 30/70.
- Optimum V_{DD} and V_{TH} are given by this condition.

Tip 3: If you don't need to hustle, relax and save power.
- Squeezing out last 10% of performance is very costly in dynamic & leakage power consumption due to super-linearity.
- Last 5% of performance increase demands 20% more power in repeater insertion in a long interconnect due to super-linearity.

Tip 4: Utilize surplus timing with multiple V_{DD}'s and V_{TH}'s.
- Employ lower V_{DD}, higher V_{TH}, in non-critical circuits to reduce power dissipation, leakage current, without degrading chip performance.

Tip 5: Total power is minimum when V_{DDL}/V_{DDH} =0.7.
- This rule almost applies to any design in any technology.

Summary (cont.)

Tip 6: Two types are sufficient.
- Dual V_{DD}'s, dual V_{TH}'s are enough in design with multiple voltage planes.

Tip 7: Adapt to the change with variable V_{DD} and V_{TH}.
- V_{DD}, V_{TH} can be optimally controlled by circuit.

Tip 8: Two levels are sufficient.
- f and $f/2$ are good enough in V_{DD}, V_{TH} hopping.

Tip 9: Cooperate across various levels of design hierarchy.
- System knows when you can cut a corner. Circuit knows how to make it.
- Technology provides multiple kinds of MOSFET's and designers make use of the gift.

Tip 10: Right circuit for the right job.
- Employ different circuits with their own good points, and create a best mix of the advantages rather than employing a single best circuit.

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