

IMFEDK 2013 Awards

■ IEEE EDS Kansai Chapter IMFEDK Best Paper Award

Authors: **Yasufumi Kawai, Shuichi Nagai, Noboru Negoro, Takeshi Fukuda, Tetsuzo Ueda, Nobuyuki Otsuka and Daisuke Ueda** Paper ID: B-2
Title: "A Compact Isolated Gate Driver using GaN HFETs on Sapphire Substrate Integrated with a 5.8GHz Electro-Magnetic Resonant Coupler"
Affiliation: Panasonic Corporation

■ IEEE EDS Kansai Chapter IMFEDK Student Paper Award

Author: **Indra Nur Adisusilo**¹ Paper ID: PA-01
Title: "Monte Carlo Simulation of Seebeck Coefficient of Si Nanostructure with Barrier Layers"
Coauthors: Kentaro Kukita¹ and Yoshinari Kamakura^{1,2}
Affiliation: ¹Osaka University, ²CREST)

Author: **Daiki Sato** Paper ID: PA-02
Title: "Scaling Scheme Prospect of XCT-SOI MOSFET Aiming at Medical Implant Applications Showing a Long Lifetime with a Small Battery"
Coauthors: Yasuhisa Omura
Affiliation: Kansai University

Author: **Kazuya Mukai**¹ Paper ID: PB-01
Title: "Growth of a sputtered Ta₂O₅/ZnO film and its application to an ion-sensitive field-effect transistor"
Coauthors: Takayuki Onaka¹, Kazuto Koike¹, Toshihiko Maemoto¹, Shigehiko Sasa¹, Mitsuaki Yano¹, Sadao Kadokura² and Yutaka Nakamitsu²
Affiliation: ¹Osaka Institute of Technology, ²FTS Corporation)

Author: **Takayuki Kadonome** Paper ID: PC-01
Title: "Retinal Prosthesis of Frequency Modulation using Thin-Film Photo Transistors"
Coauthors: Atsushi Matsumura, Tsuyoshi Higashiyama, Shohei Oyama and Mutsumi Kimura
Affiliation: Ryukoku University

Author: **Satoru Sasaki** Paper ID: PC-02
Title: "Fabrication of zinc oxide transparent thin film transistors on glass substrates by sol-gel method"
Coauthors: Shigehiko Sasa, Ken-Ichi Ogata and Toshihiko Maemoto
Affiliation: Osaka Institute of Technology

Author: **Keisuke Kado**¹ Paper ID: C-4
Title: "Evaluation of TaOx Nanoparticles for Resistive Random Access Memory"
Coauthors: Takahiro Ban^{1,2}, Mutsunori Uenuma^{1,2} and Yasuaki Ishikawa^{1,2}
Affiliation: ¹NAIST, ²CREST

■ IEEE SSCS Kansai Chapter IMFEDK Student Paper Award

Author: **Shusuke Yoshimoto**¹

Paper ID: PS-01

Title: “Multiple-Cell-Upset Hardened 6T SRAM Using NMOS-Centered Layout”

Coauthors: Koji Nii², Hiroshi Kawaguchi¹ and Masahiko Yoshimoto^{1,3}

Affiliation: ¹Kobe University, ²Renesas Electronics Corporation, ³JST CREST

