

IEEE EDS Kansai Chapter の皆様

IEEE Kansai Section の皆様

2008年 10月 6日

IEEE EDS Kansai Chapter

Chair 西村 正

Vice Chair 大村 泰久

下記の通り、第8回「IEEE関西チャプタ、コロキウム・ワークショップ」を開催致します。会員の皆様のご参加をお待ち申し上げます。

記

会議名:第8回「IEEE関西チャプタ、コロキウム・ワークショップ」

主催: IEEE Electron Devices Society Kansai Chapter

日時: 平成20年10月17日(金)10:00~18:00

会場: 関西大学・100周年記念会館・第三会議室

場所: 〒564-8680 大阪府吹田市山手町3丁目3番35号

<http://www.kansai-u.ac.jp/index.html>

公用語:日本語

会費: 無料(事前登録不要)

IEEE EDS Kansai Chapter

第8回IEEE関西チャプタ、コロキウム・ワークショップ・プログラム

2008年10月17日

関西大学・100周年記念会館

第三会議室

開会挨拶

西村 正 (ルネサステクノロジ)

[10:00-10:10]

セッション I. **Silicon LSI Technology and Simulation** [10:10 -12:15]

座長：渡辺 博文 (リコー)

[10:10-10:35]

#1 Toward Variability-Aware Design

H. Onodera

Graduate School of Informatics, Kyoto University

[10:35-11:00]

#2 Influences of Elastic and Inelastic Scatterings on Ballistic Transport in MOSFETs

H. Tsuchiya¹ and S. Takagi^{2,3}

¹Graduate School of Engineering, Kobe University

²MIRAI-ASRC, AIST,

³Graduate School of Frontier Science, The University of Tokyo

[11:00-11:25]

#3 Gate-Controlled Bipolar Action in Ultrathin-Body Dynamic-Threshold SOI MOSFET

Y. Omura and T. Tochio

ORDIST, Faculty of Sci. & Eng., Kansai University

[11:25-11:50]

#4 Controllable Inverter Delay and Suppressing V_{th} Fluctuation Technology in Silicon on Thin BOX Featuring Dual Back-Gate Bias Architecture

R. Tsuchiya^{1,2}, T. Ishigaki², Y. Morita², M. Yamaoka², **T. Iwamatsu**¹, T. Ipposhi¹, H. Oda¹, N. Sugii², S. Kimura², K. Itoh² and Y. Inoue¹

¹Renesas Technology Corp.

²Central Research Laboratory, Hitachi, Ltd.

[11:50-12:15]

#5 Analysis of As, P Diffusion and Defect Evolution during Sub-millisecond Non-melt Laser Annealing based on an Atomistic Kinetic Monte Carlo Approach

T. Noda¹, W. Vandervorst^{2,3}, S. Felch⁴, V. Parihar⁴, A. Cuperus⁴, R. McIntosh⁴, C. Vrancken², E. Rosseel², H. Bender², B. Van Daele², M. Niwa¹, H. Umimoto¹, R. Schreutelkamp⁴, P. P. Absil², M. Jurczak², K. De Meyer^{2,3}, S. Biesemans² and T. Y. Hoffmann²

¹Matsushita Electric Industrial Co., Ltd.

²IMEC, ³K.U. Leuven, ⁴Applied Materials

—昼食 [12:15 - 13:15]—

セッション II. Power Device, Nano Device and Photo Device Technology [13:15 - 15:15]

座長：佐々 誠彦（大阪工業大学）

[13:15-14:00]

#1 8300V Blocking Voltage AlGaN/GaN Power HFET with Thick Poly-AlN Passivation

Y. Uemoto, **D. Shibata**, M. Yanagihara, H. Ishida, H. Matsuo, S. Nagai*, N. Batta*, M. Li*, T. Ueda, T. Tanaka and D. Ueda

Semiconductor Device Research Center, Semiconductor Company, Matsushita Electric – Panasonic

*Panasonic Boston Laboratory, Panasonic Technologies Company.

[14:00-14:25]

#2 4H-SiC Lateral Double RESURF MOSFETs With Low ON Resistance

M. Noborio, J. Suda and T. Kimoto

Department of Electronic Science and Engineering, Kyoto University.

[14:25-14:50]

#3 Single charge sensitivity of single-walled carbon nanotube single-hole transistor

T. Kamimura^{1, 2}, Y. Ohno^{1, 2} and K. Matsumoto^{1, 2, 3}

¹The Institute of Scientific and Industrial Research, Osaka University

²CREST/JST

³National Institute of Advanced Industrial Science and Technology

[14:50-15:15]

#4 Degradation Mode Analysis on Highly Reliable Guardring-Free Planar InAlAs Avalanche Photodiodes

E. Ishimura¹, E. Yagyu², M. Nakaji¹, S. Ihara¹, K. Yoshiara², T. Aoyagi¹, Y. Tokuda²
and T. Ishikawa¹

¹High Frequency and Optical Device Works, Mitsubishi Electric Corporation

²Advanced Technology R&D Center, Mitsubishi Electric Corporation

—休憩 [15:15 - 15:35]—

セッション III. MEMS, Memory, Sensor and Film formation Technology [15:35 - 17:40]

座長：小瀧 浩（シャープ）

[15:35-16:00]

#1 Fast switching and long retention Fe-O ReRAM and its switching mechanism

S. Muraoka, K. Osano, Y. Kanzawa, S. Mitani, S. Fujii, K. Katayama, Y. Katoh, Z. Wei, T. Mikawa,
K. Arita, Y. Kawashima, R. Azuma, K. Kawai, K. Shimakawa, A. Odagawa and T. Takagi
Advanced Devices Development Center, Matsushita Electric Ind. Co., Ltd.

[16:00-16:25]

#2 Large Grain Poly-crystalline Si Films by Carbon Dioxide Laser Assisted SLG Method

H. Tsunazawa¹, Y. Taniguchi¹, S. Okazaki¹, M. Seki¹, Y. Otsuka¹, H. Takeuchi¹, M. Okamoto¹
and J. Nakayama²

¹Production Technology Development Group, SHARP Corporation

²International Business Group, SHARP Laboratories of America Inc.

[16:25-16:50]

#3 3 D real-time CCD imager based on Background-Level-Subtraction scheme

Y. Hashimoto, F. Kurihara, F. Tsunesada, K. Imai, Y. Takada and K. Taniguchi¹

Information Equipment & Wiring Products Manufacturing Business Unit, Matsushita Electric
Works, Ltd.

¹Graduate School of Engineering, Osaka University

[16:50-17:15]

#4 Mechanical Characteristics of FIB Deposited Carbon Nanowires Using an Electrostatic Actuated Nano Tensile Testing Device

M. Kiuchi¹, S. Matsui² and Y. Isono³

¹ Graduate School of Science and Engineering, Ritsumeikan University

² Laboratory of Advanced Science and Technology for Industry, University of Hyogo

³ Department of Micro System Technology, Faculty of Science and Engineering, Ritsumeikan University

[17:15-17:40]

#5 Development of a multi-chip retinal stimulator for in vivo experiments toward retinal prosthesis

T. Tokuda¹, R. Asano¹, Y. Terasawa², M. Nunoshita¹, K. Nakauchi³, T. Fujikado³, Y. Tano³
and ***J. Ohta***¹

¹ Graduate School of Materials Science, Nara Institute of Science and Technology

² Vision Institute, R&D Div., NIDEK Co., Ltd.

³ Department of Ophthalmology, Osaka University Medical School

[17:40-18:00]

AWARD 授与

神澤 公 (ローム)

—閉会—

西村 正 (ルネサステクノロジ)

[お問い合わせ先]

IEEE EDS Kansai Chapter Secretary: 井上靖朗(inoue.yasuo@renesas.com)