IEEE EDS Kansai Chapter の皆様
IEEE Kansai Section の皆様

2008 年　10 月 6 日
IEEE EDS Kansai Chapter
Chair　西村 正
Vice Chair　大村 泰久

下記の通り、第 8 回「ＩＥＥＥ関西チャプタ、コロキウム・ワークショップ」を開催致します。会員の皆様のご参加をお待ち申し上げております。

記

会議名:第 8 回「ＩＥＥＥ関西チャプタ、コロキウム・ワークショップ」
主催: IEEE Electron Devices Society Kansai Chapter
日時: 平成 20 年 10 月 17 日(金)10:00～18:00
会場: 関西大学・１００周年記念会館・第三会議室
場所: 〒564-8680　大阪府吹田市山手町 3 丁目 3 番 35 号
http://www.kansai-u.ac.jp/index.html
公用語:日本語
会費: 無料(事前登録不要)

IEEE EDS Kansai Chapter

第８回ＩＥＥＥ関西チャプタ、コロキウム・ワークショップ・プログラム

2008 年 10 月 17 日

関西大学・１００周年記念会館

第三会議室

開会挨拶　　西村 正（ルネサステクノロジ）

[10:00-10:10]

セッション I. Silicon LSI Technology and Simulation [10:10 -12:15]

座長：渡辺 博文（リコー）

[10:10-10:35]

#1 **Toward Variability-Aware Design**

H. Onodera

Graduate School of Informatics, Kyoto University

[10:35-11:00]

#2 **Influences of Elastic and Inelastic Scatterings on Ballistic Transport in MOSFETs**

H. Tsuchiya[1] and S. Takagi[2,3]

[1]Graduate School of Engineering, Kobe University

[2]MIRAI-ASRC, AIST,

[3]Graduate School of Frontier Science, The University of Tokyo

[11:00-11:25]

#3 **Gate-Controlled Bipolar Action in Ultrathin-Body Dynamic-Threshold SOI MOSFET**

Y. Omura and T. Tochio

ORDIST, Faculty of Sci. & Eng., Kansai University

[11:25-11:50]

#4 **Controllable Inverter Delay and Suppressing V_{th} Fluctuation Technology in Silicon on Thin BOX Featuring Dual Back-Gate Bias Architecture**

R. Tsuchiya[1, 2], T. Ishigaki[2], Y. Morita[2], M. Yamaoka[2], ***T. Iwamatsu***[1], T. Ipposhi[1], H. Oda[1], N. Sugii[2], S. Kimura[2], K. Itoh[2] and Y. Inoue[1]

[1]Renesas Technology Corp.

[2]Central Research Laboratory, Hitachi, Ltd.

[11:50-12:15]

#5 **Analysis of As, P Diffusion and Defect Evolution during Sub-millisecond Non-melt Laser Annealing based on an Atomistic Kinetic Monte Carlo Approach**

T. Noda[1], W. Vandervorst[2,3], S. Felch[4], V. Parihar[4], A. Cuperus[4], R. Mcintosh[4], C. Vrancken[2], E. Rosseel[2], H. Bender[2], B. Van Daele[2], M. Niwa[1], H. Umimoto[1], R. Schreutelkamp[4], P. P. Absil[2], M. Jurczak[2], K. De Meyer[2,3], S. Biesemans[2] and T. Y. Hoffmann[2]

[1]Matsushita Electric Industrial Co., Ltd.

[2]IMEC, [3]K.U. Leuven, [4]Applied Materials

―昼食 [12:15 - 13:15]―

セッション II. Power Device, Nano Device and Photo Device Technology [13:15 - 15:15]

座長：佐々 誠彦（大阪工業大学）

[13:15-14:00]

#1 **8300V Blocking Voltage AlGaN/GaN Power HFET with Thick Poly-AlN Passivation**

Y. Uemoto, ***D. Shibata***, M. Yanagihara, H. Ishida, H. Matsuo, S. Nagai*, N. Batta*, M. Li*, T. Ueda, T. Tanaka and D. Ueda

Semiconductor Device Research Center, Semiconductor Company, Matsushita Electric – Panasonic

*Panasonic Boston Laboratory, Panasonic Technologies Company.

[14:00-14:25]

#2 **4H–SiC Lateral Double RESURF MOSFETs With Low ON Resistance**

M. Noborio, J. Suda and T. Kimoto

Department of Electronic Science and Engineering, Kyoto University.

[14:25-14:50]

#3 **Single charge sensitivity of single-walled carbon nanotube single-hole transistor**

T. Kamimura[1, 2], Y. Ohno[1, 2] and K. Matsumoto[1, 2, 3]

[1]The Institute of Scientific and Industrial Research, Osaka University

[2]CREST/JST

[3]National Institute of Advanced Industrial Science and Technology

[14:50-15:15]

#4 **Degradation Mode Analysis on Highly Reliable Guardring-Free Planar InAlAs Avalanche Photodiodes**

E. Ishimura[1], E. Yagyu[2], M. Nakaji[1], S. Ihara[1], K. Yoshiara[2], T. Aoyagi[1], Y. Tokuda[2] and T. Ishikawa[1]

[1]High Frequency and Optical Device Works, Mitsubishi Electric Corporation

[2]Advanced Technology R&D Center, Mitsubishi Electric Corporation

—休憩 [15:15 - 15:35]—

セッション III. MEMS, Memory, Sensor and Film formation Technology [15:35 - 17:40]

座長：小瀧　浩（シャープ）

[15:35-16:00]

#1 **Fast switching and long retention Fe-O ReRAM and its switching mechanism**

S. Muraoka, K. Osano, Y. Kanzawa, S. Mitani, S. Fujii, K.Katayama, Y. Katoh, Z. Wei, T. Mikawa, K. Arita, Y. Kawashima, R. Azuma, K. Kawai, K. Shimakawa, A. Odagawa and T. Takagi

Advanced Devices Development Center, Matsushita Electric Ind. Co., Ltd.

[16:00-16:25]

#2 **Large Grain Poly-crystalline Si Films by Carbon Dioxide Laser Assisted SLG Method**

H. Tsunazawa[1], Y. Taniguchi[1], S. Okazaki[1], M. Seki[1], Y. Otsuka[1], H. Takeuchi[1], M. Okamoto[1] and J. Nakayama[2]

[1]Production Technology Development Group, SHARP Corporation

[2]International Business Group, SHARP Laboratories of America Inc.

[16:25-16:50]

#3 **3 D real-time CCD imager based on Background-Level-Subtraction scheme**

Y. Hashimoto, F. Kurihara, F. Tsunesada, K. Imai, Y. Takada and K. Taniguchi[1]

Information Equipment & Wiring Products Manufacturing Business Unit, Matsushita Electric Works, Ltd.

[1]Graduate School of Engineering, Osaka University

[16:50-17:15]

#4 **Mechanical Characteristics of FIB Deposited Carbon Nanowires Using an Electrostatic Actuated Nano Tensile Testing Device**

M. Kiuchi[1], S. Matsui[2] and Y. Isono[3]

[1] Graduate School of Science and Engineering, Ritsumeikan University

[2] Laboratory of Advanced Science and Technology for Industry, University of Hyogo

[3] Department of Micro System Technology, Faculty of Science and Engineering, Ritsumeikan University

[17:15-17:40]

#5 **Development of a multi-chip retinal stimulator for in vivo experiments toward retinal prosthesis**

T. Tokuda[1], R. Asano[1], Y. Terasawa[2], M. Nunoshita[1], K. Nakauchi[3], T. Fujikado[3], Y. Tano[3] and ***J. Ohta***[1]

[1] Graduate School of Materials Science, Nara Institute of Science and Technology

[2] Vision Institute, R&D Div., NIDEK Co., Ltd.

[3] Department of Ophthalmology, Osaka University Medical School

[17:40-18:00]

AWARD 授与 神澤 公（ローム）

―閉会― 西村 正（ルネサステクノロジ）

[お問い合せ先]

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