



主催： IEEE Electron Devices Society Kansai Chapter
日時： 平成 14 年 1 月 16 日 (水) 午前 9 時 ~ 午後 5 時
会場： キャンパスプラザ京都, 第一会議室
場所： 京都市下京区西洞院通塩小路下る
定員： 63 名
公用語： 日本語
会費： IEEE 会員 (2,000 円) IEEE 学生会員 (無料)
使用機器： OHP および Projector 共に可
講演時間配分： 一件につき発表 20 分、質疑応答 5 分

Advance Program

Opening Session Chaired by Y. Yamamoto (*kyoto Univ.*)

- 9:00am** Opening Remark by A. Suzuki (*Sharp*)
- 9:05am** Award Presentation by T. Nishimura (*Mitsubishi*)

Technical Session A Chaired by D. Ueda (*Matsushita*)

- 9:10am** A-1 "Design and Analysis of Heterojunction Bipolar Transferred Electron Devices" J. K. Twynam, M. Yagura, N. Takahashi, E. Suematsu, K. Sakuno, and H. Sato, (*Sharp*)
- 9:35am** A-2 "Super Self-Aligned GaAs RF Switch IC with 0.25 dB Extremely Low Insertion Loss for Mobile Communication Systems " S. Makioka, Y. Anda, K. Miyatsiji, and D. Ueda (*Matsushita*)
- 10:00am** A-3 " Junction Capacitance Reduction Due to Self-Aligned Pocket Implantation in Elevated Source/Drain NMOSFETs," N. Miura, Y. Abe, K. Sigihara, T. Oishi, T. Furukawa, T. Nakahata, K. Shiozawa, S. Maruno, and Y. Tokuda, (*Mitsubishi*)
- 10:25am** A-4 "Novel GaN-based MOS HFETs with Thermally Oxidized Gate Insulator," K. Inoue, Y. Ikeda, H. Masato, T. Matsuno, and K. Nishii (*Matsushita*)
- 10:50am** A-5: Realization of Ultra-shallow Junction: Suppressed Boron Diffusion and Activation by Optimized Fluorine Co-implantation,"
T. Sano, R. Kim, T. Hirose, Y. Furuta, H. Tsuji, M. Furuhashi, and K. Taniguchi (*Osaka Univ.*)
- 11:15am** A-6 "Modeling of End-of-Range (EOR) Defects for Indium Channel Engineering,"
T. Noda (*Matsushita*)
- 11:40am** A-7: "Feasibility of 0.18um SOI CMOS Technology Using Hybrid Trench Isolation With High Resistivity Substrate for Embedded RF/Analog Applications,"
S. Maeda, Y. Wada, K. Yamamoto, H. Komurasaki, T. Matsumoto, Y. Hirano, T. Iwamatsu, Y.

Yamaguchi, T. Ipposhi, K. Ueda, K. Mashiko, S. Maegawa, and M. Inuishi (*Mitsubishi*)

Technical Session B Chaired by T. Otsuki (*Matsushita*)

- 1:00pm** B-1:"A Highly Reliable Ferroelectric Memory Technology with SrBi₂Ta₂O₉-Based Material and Metal Covering Cell Structure,"
E. Fujii, Y. Judai, T. Ito, T. Kutsunai, Y. Nagano, A. Noma, T. Nasu, Y. Izutsu, T. Mikawa, H. Yasuoka, M. Azuma, Y. Shimada, Y. Sasai, K. Sato, and T. Otsuki (*Matsushita*)
- 1:25pm** B-2: "Short Channel Characteristics of Quasi-Single-Drain MOSFETs,"
K.Sugihara, Y. Abe, T. Oishi, N. Miura, and Y. Tokuda (*Mitsubishi*)
- 1:50pm** B-3:"70nm SOI-CMOS of 135 GHz f_{max} with Dual Offset-Implanted Source-Drain Extension Structure for RF/Analog and Logic Applications,"
T. Matsumoto, S. Maeda, K. Ota, Y. Hirano, K. Eikyu, H. Sayama, T. Iwamatsu, K. Yamamoto, T. Katoh, Y. Yamaguchi, T. Ipposhi, H. Oda, S. Maegawa, Y. Inoue and M. Inuishi (*Mitsubishi*)
- 2:15pm** B-4:"SoC CMOS Technology for NBTI/HCL Immune I/O and Analog Circuits Implementing Surface and Buried Channel Structure,"
Y. Nishida, H. Sayama, K. Ota, H. Oda, M. Katayama, Y. Inoue, H. Morimoto and M. Inuishi (*Mitsubishi*)

Technical Session C Chaired by T. Shimazaki (*Rohm*)

- 2:40pm** C-1:" OFF-State Leakage Current Mechanisms in Bulk Si and SOI MOSFETs and Their Impact on CMOS ULSIs Standby Current,"
A.O. Adan, and K. Higashi, (*Sharp*)
- 3:05pm** C-2:"Reliability of Low Temperature Poly-Silicon TFTs Under Inverter Operation,"
Y. Uraoka, T. Hatayama, T. Fuyuki, T. Kawamura, and Y. Tsuchihashi* (*NAIST, *; Matsushita*)
- 3:30pm** C-3:"Ferroelectric Dielectric Technology,"
M. Takayama, S. Koyama, and H. Nozawa (*Kyoto Univ.*)
- 3:55pm** C-4:"A Model for Anomalous Leakage Current in Flash Memories and Its Application for the Prediction of Retention Characteristics,"
K. Okada, (*Matsushita*)
- 4:20pm** C-5:"An Artificial Fingerprint Device (AFD) Module using Poly-Si Thin Film Transistors with Logic LSI Compatible Process for Built-in Security,"
S. Maeda, H. Kuriyama, T. Ipposhi, S. Maegawa, and M. Inuishi (*Mitsubishi*)

General Meeting Chaired by M. Kazumura (*Matsushita*)

- 4:45pm** Report on Organization and Activities of ED Kansai Chapter by H. Nozawa (*Kyoto Univ.*)
Financial Report of ED Kansai Chapter by T. Otsuki (*Matsushita*)
- 5:00 pm** Closed