ED Japan Chapter

by Mitsumasa Koyanagi, Chair

On Nov. 14, 2008, the IEEE EDS Japan Chapter Technology Forum was held at Westin Hotel, Tokyo, which was sponsored by ED Japan Chapter and was also supported by Applied Materials. The title of technology forum was "The Reality of 32nm: Technology plus Manufacturability." The aim of the forum was to discuss both process/device technologies and manufacturability for 32-nm-node logic/memory LSIs. Nine distinguished speakers were invited from Japan and from abroad, and covered topics including NAND/NOR flash memory, lithography, advanced FEOL/BEOL technologies, and 3-D integration. All the speakers gave excellent talks and made fruitful discussions with the audience. The symposium attracted more than 200 people, and was a great success.

++++++++++++++++++++++++++++++++++++++++++++++++++++++++++++++++++++++++++++++

Photo caption:

the IEEE EDS Japan Chapter Technology Forum on Nov. 14, 2008. The Symposium was held at the Westin Hotel, Tokyo, Japan.

++++++++++++++++++++++++++++++++++++++++++++++++++++++++++++++++++++++++++++++