回路のばらつき解析を用いた
デバイスばらつきの抽出

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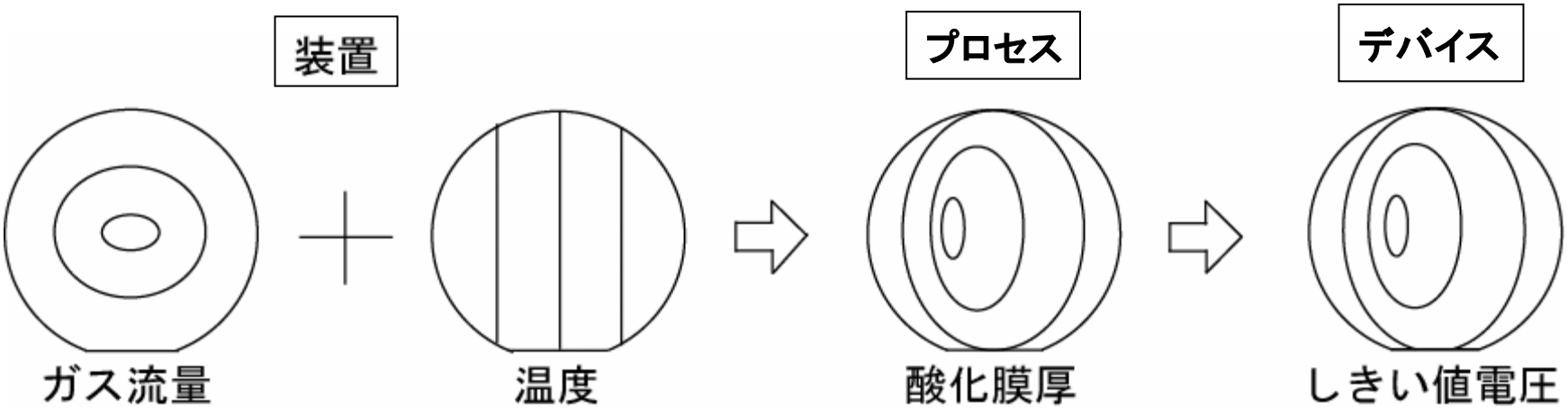
Outline

1. Conventional circuit-variation analysis based on device/process variation
   - Corner models from device-performance variation
   - Process models from process-variation analysis
2. Requirements for more accurate prediction of circuit-performance variation
3. Separation of inter-die and random intra-die variations with appropriate circuits
4. Prediction of circuit-performance variation

Typical variation effects

1. Systematic variation between processed lots: Inter-wafer

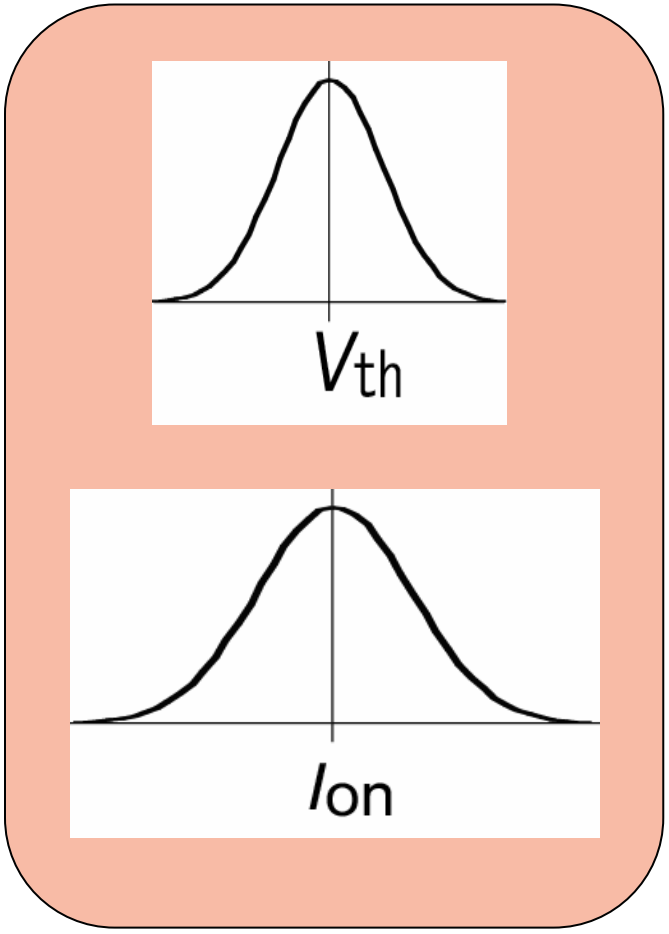
2. Parametric variation of process steps: Inter-die



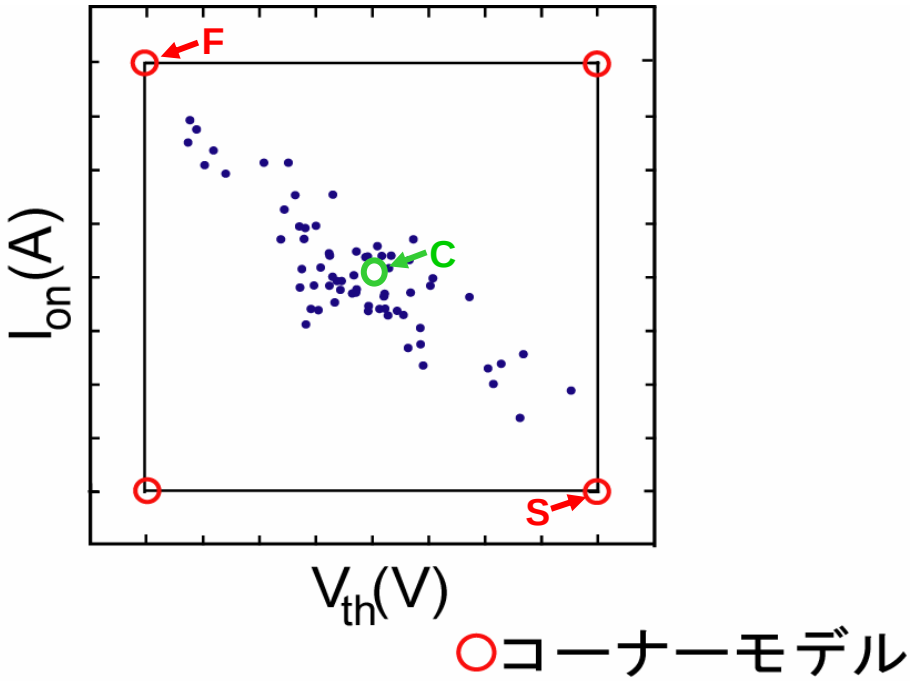
3. Random variation at close distances: Intra-die

Method of corner models (1)

Device variations



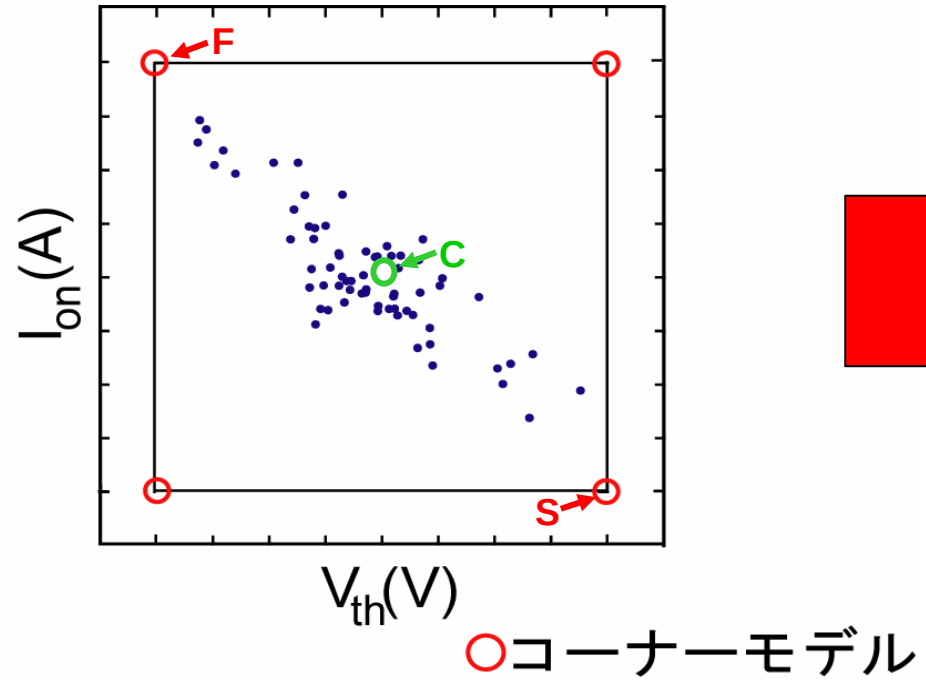
Models for variation extremes (Corner models)



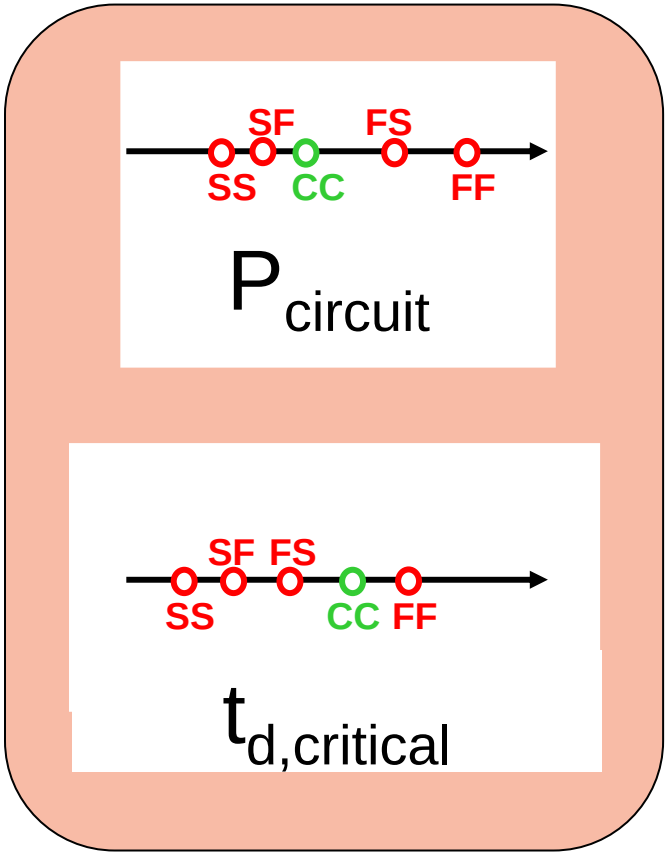
F = fast, S = slow, C = centric

Method of corner models (2)

Models for variation extremes (Corner Models)



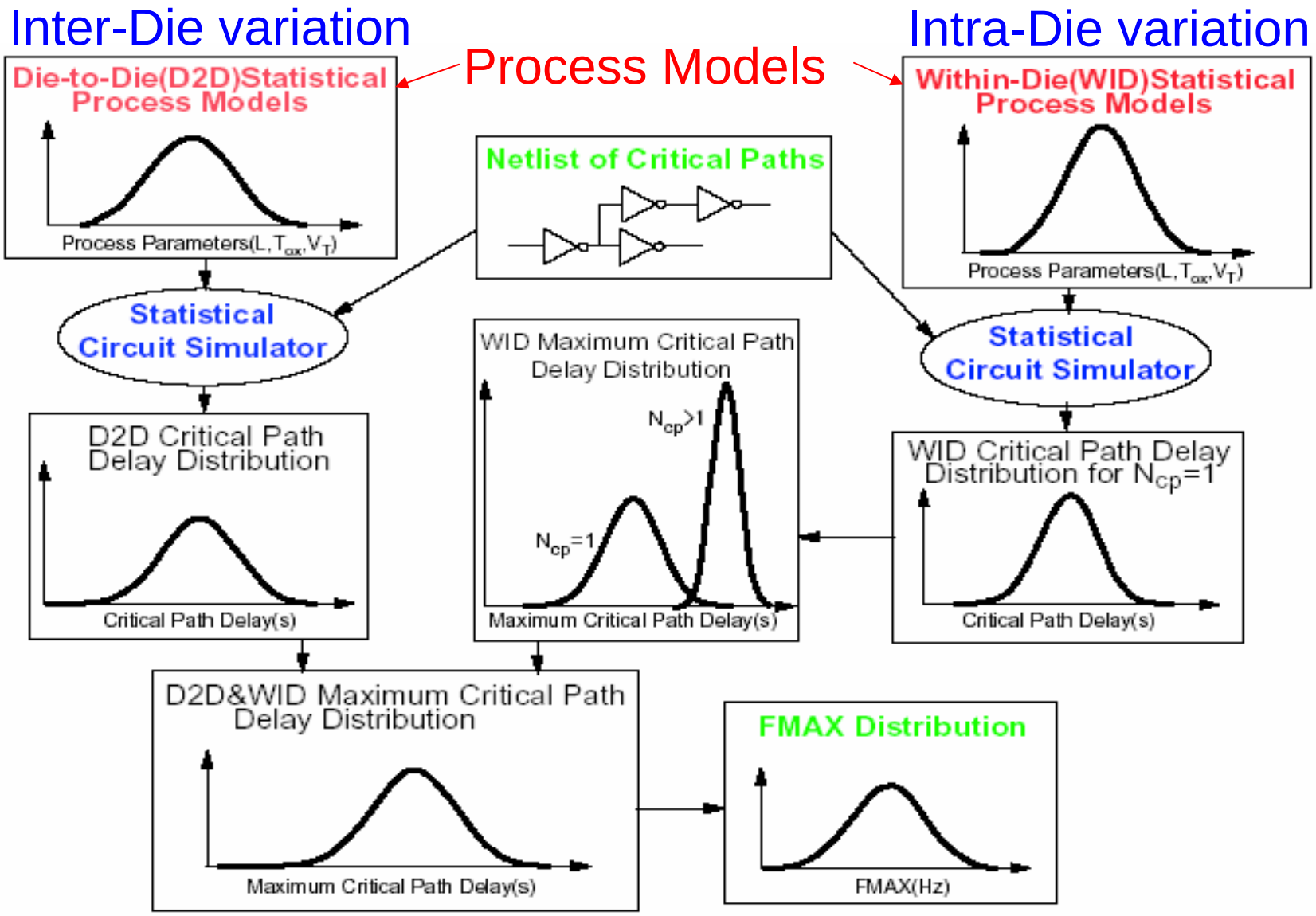
Circuit variations
(XX refers to nMOS and pMOS corner models)



F = fast, S = slow, C = centric

Conventional corner models cover mainly inter-wafer variations and overestimates circuit-performance variation.

Process-variation-based circuit analysis



K. A. Bowman et al., IEEE J. SSC, 37, 183, 2002.

Deficiencies process/device-based methods

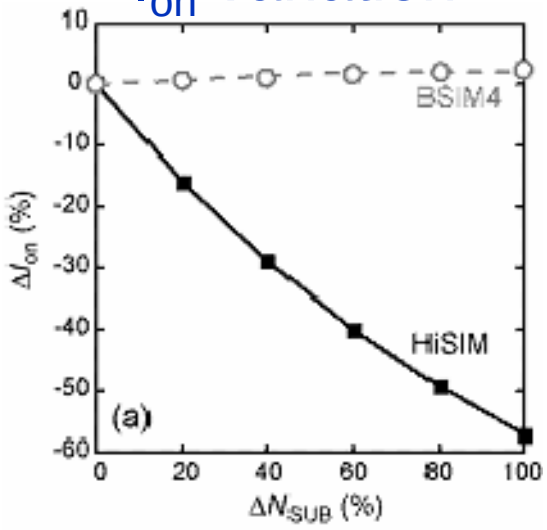
- Determination of probability distribution of circuit-performance variations from statistical process data is not really practical.
- Separation of inter-die and intra-die variations is difficult. Circuits relying on matching between transistors can help here.
- No practical reverse engineering possibility from desired circuit performance variation to necessary device-parameter variation requirements.

Outline

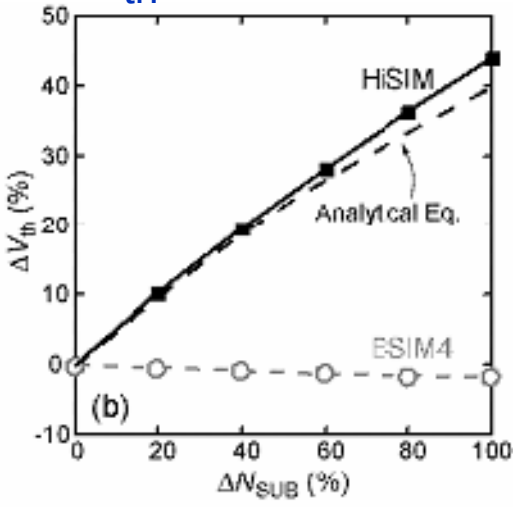
1. Conventional circuit-variation analysis based on device/process variation
2. Requirements for more accurate prediction of circuit-performance variation
   - Compact Model with accurate device-parameter correlation
   - Knowledge of inter-wafer, inter-die and random intra-die variations
3. Separation of inter-die and random intra-die variations with appropriate circuits
4. Prediction of circuit-performance variation

Variation modeling with compact models

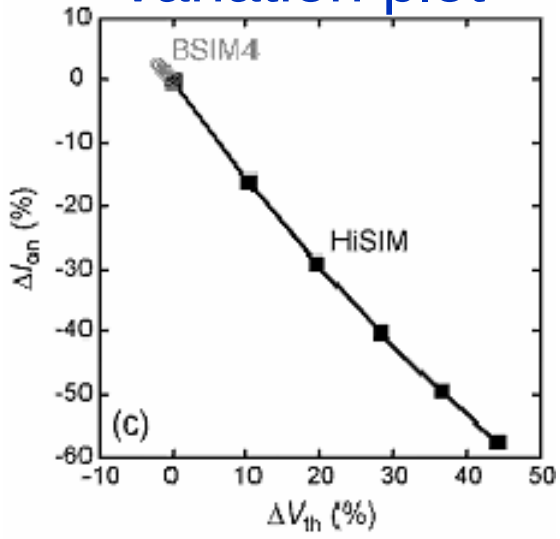
I_{on} variation



V_{th} variation



Combined I_{on}, V_{th} variation plot

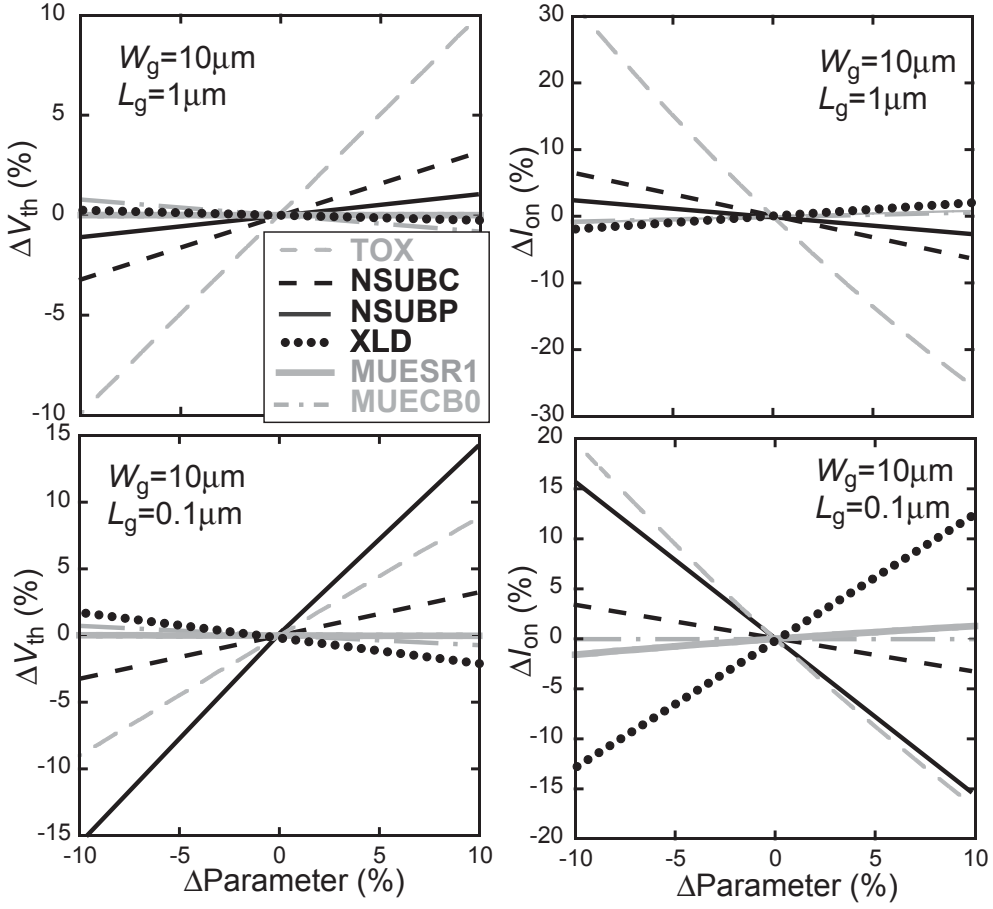


Correct correlation between device and process parameters is required.

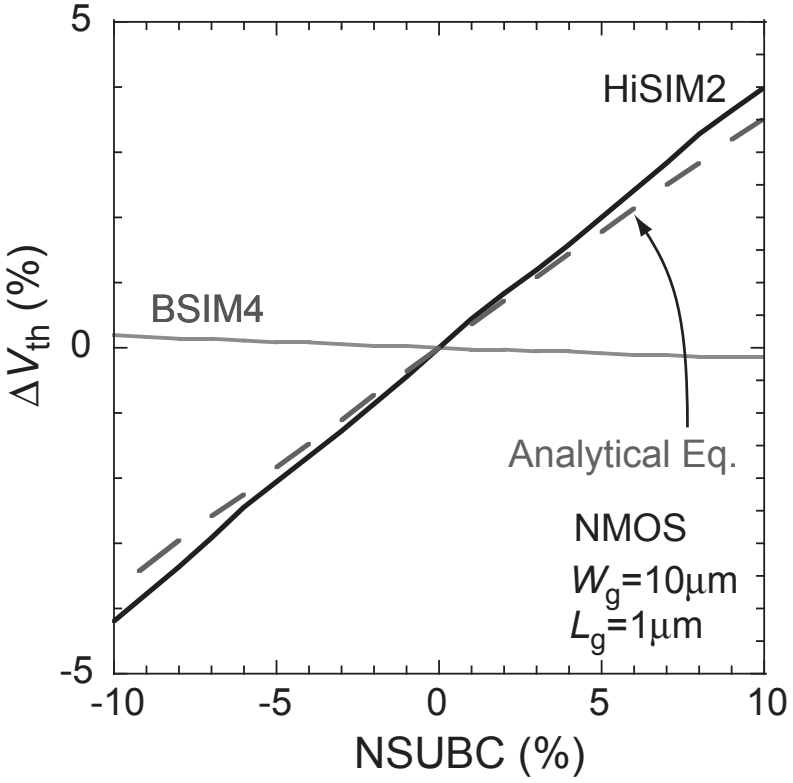
Surface-potential models like HiSIM needed.

Sensitivity analysis for process parameters

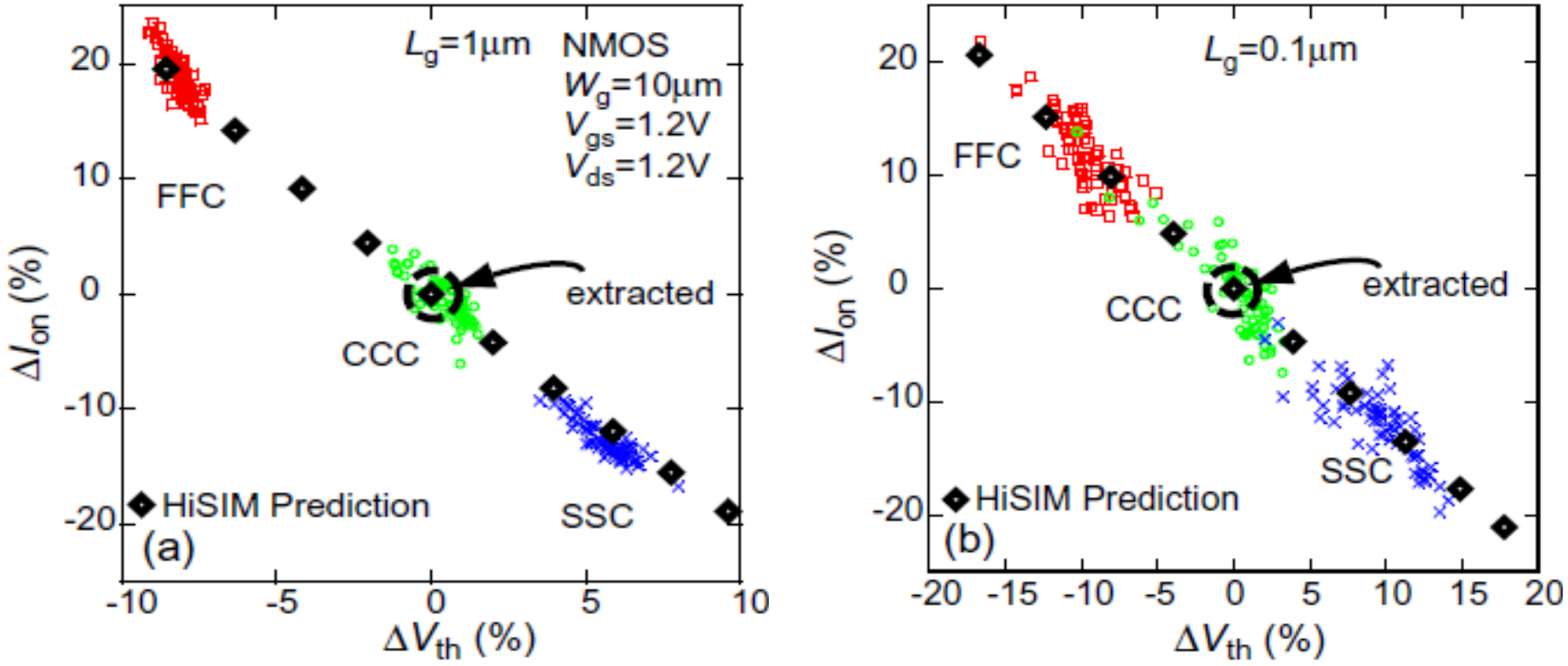
Prediction with HiSIM



Comparison with conventional model

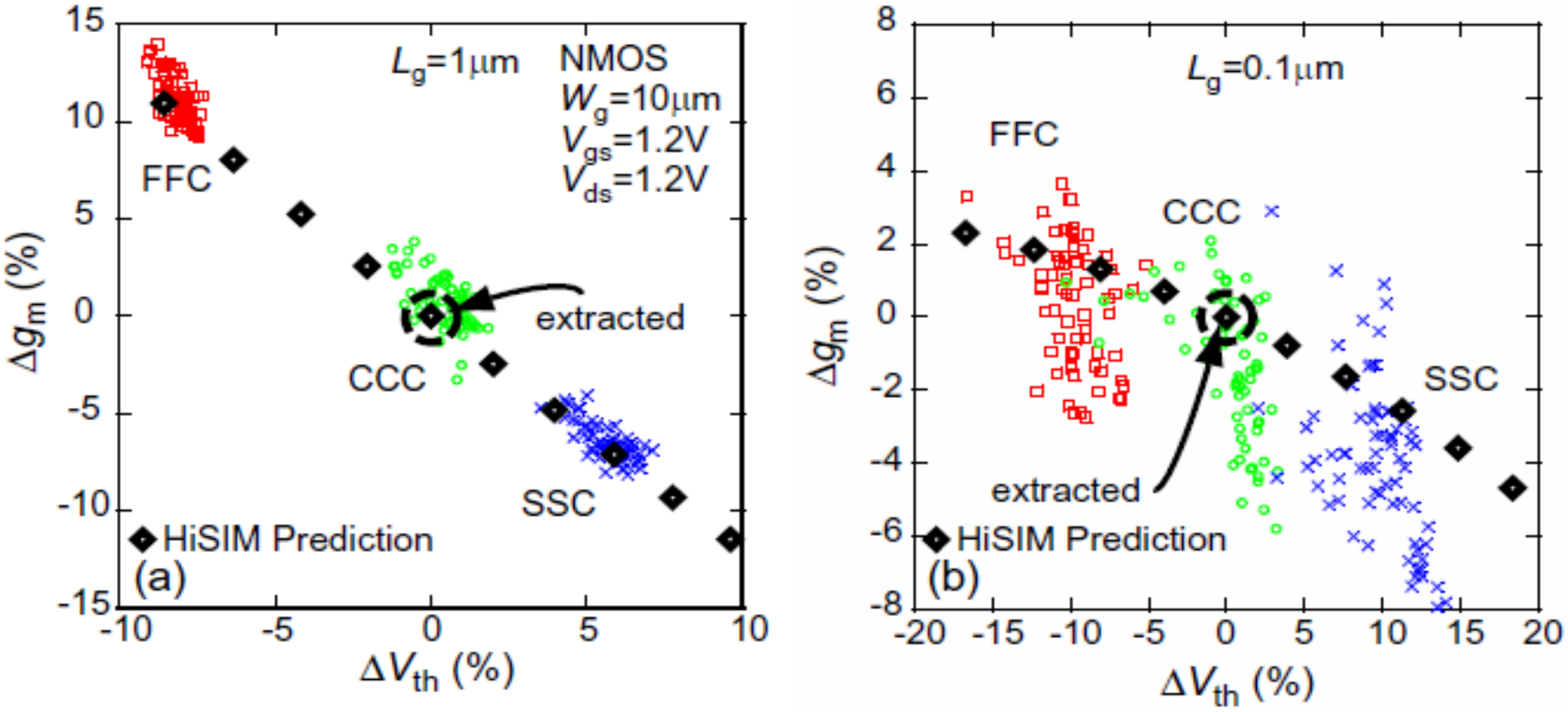


Inter-wafer variation prediction with HiSIM (1)



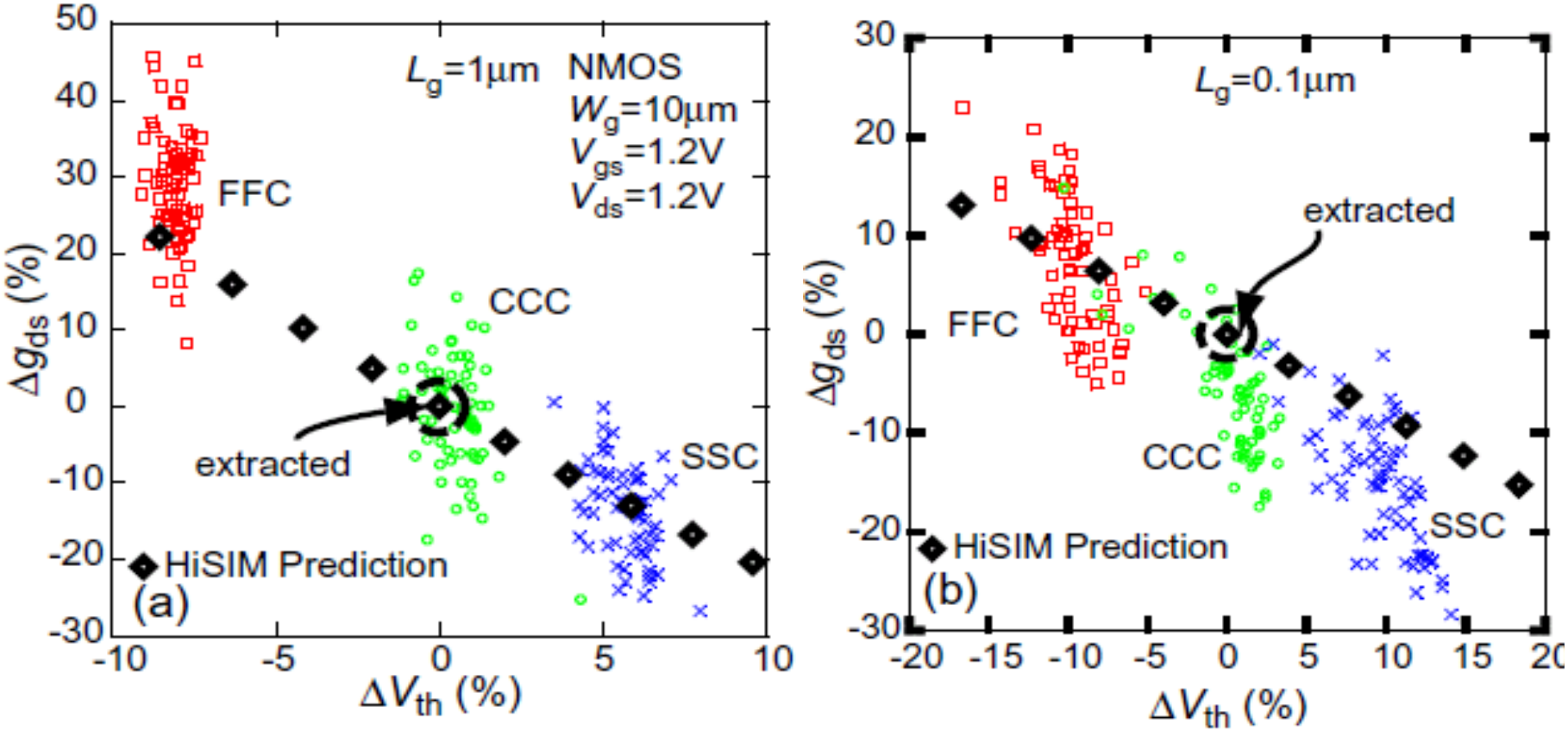
Prediction of inter-wafer variation for I_{on}, V_{th} possible

Inter-wafer variation prediction with HiSIM (2)



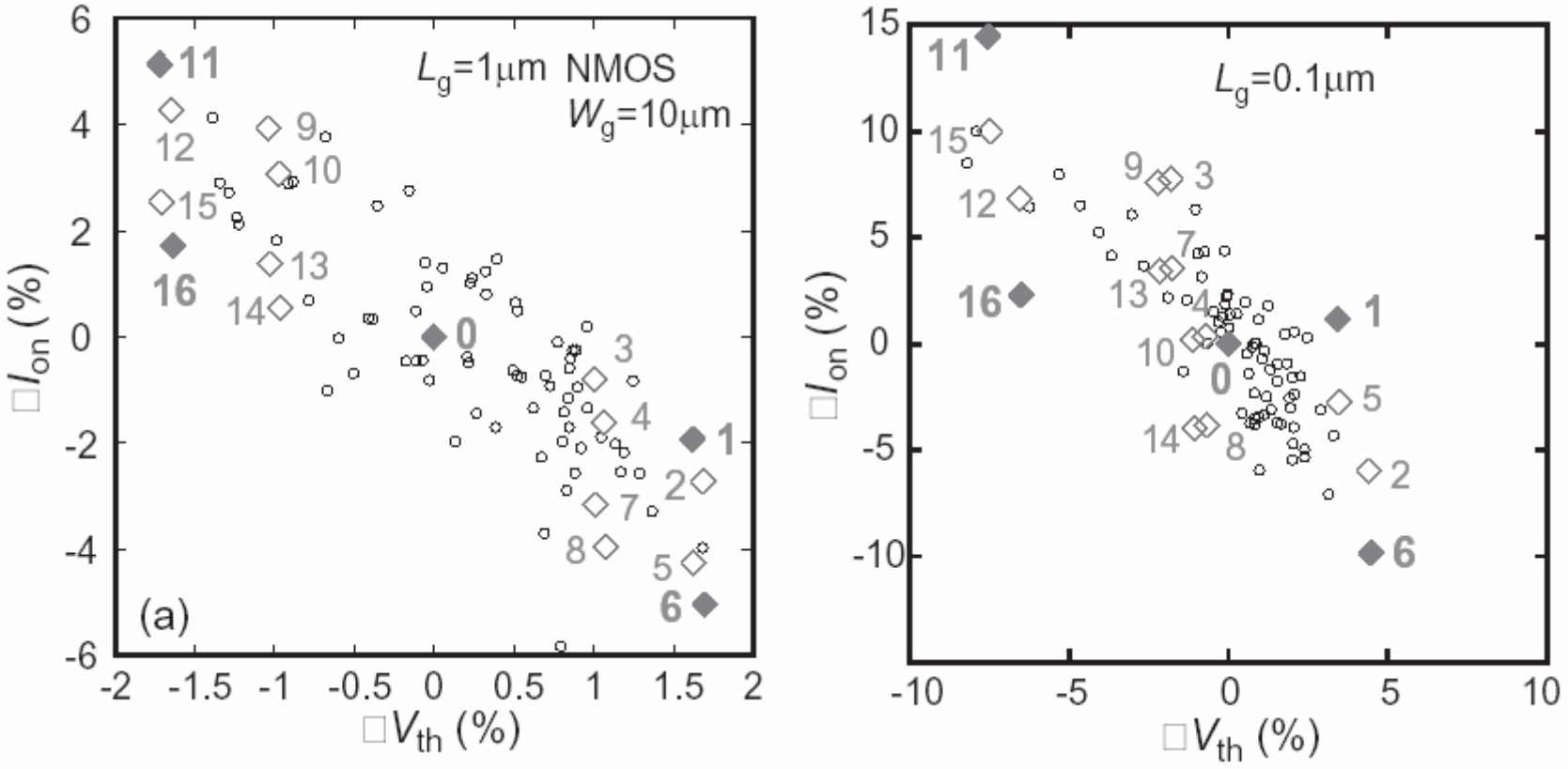
Prediction of derivative variation: Example g_m

Inter-wafer variation prediction with HiSIM (3)



Prediction of derivative variation: Example g_{ds}

Inter-die variation

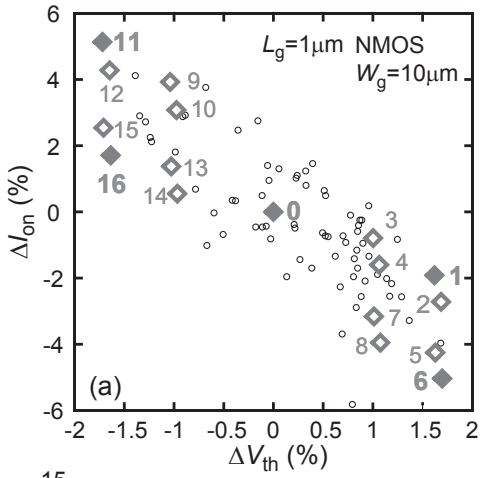


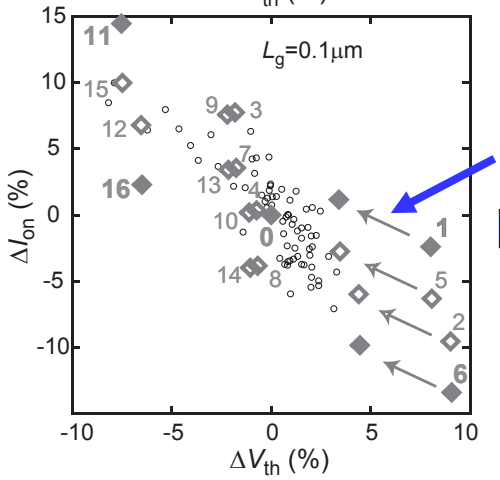
Consistent relation between inter-die device-performance variation and physical process-parameter variation can be established.

Extraction of inter-die process variation

Index	ΔNSUBC	ΔMUESR1	ΔNSUBP	ΔXLD
0	0	0	0	0
1	**+**	**+**	**+**	**+**
2	+	+	+	-
3	+	+	-	+
4	+	+	-	-
5	+	-	+	+
6	**+**	**-**	**+**	**-**
7	+	-	-	+
8	+	-	-	-
9	-	+	+	+
10	-	+	+	-
11	**-**	**+**	**-**	**+**
12	-	+	-	-
13	-	-	+	+
14	-	-	+	-
15	-	-	-	+
16	**-**	**-**	**-**	**-**

	ΔNSUBC	ΔMUESR1	ΔNSUBP	ΔXLD
Variation	±4%	±10%	−3% +1%	±3%

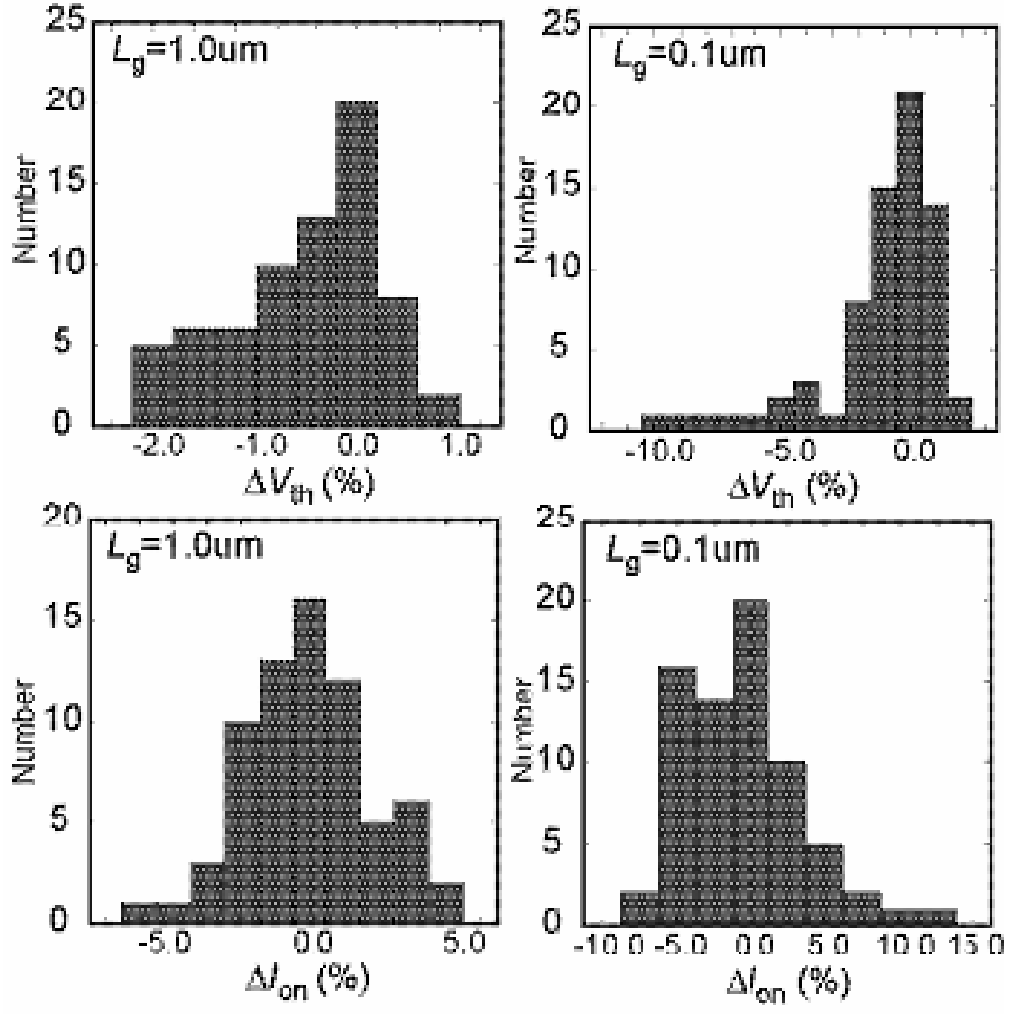




Indication for asymmetric pocket-implant variation.

HiSIM enables extraction of process-parameter variation from device-performance variation.

Asymmetric inter-die variation

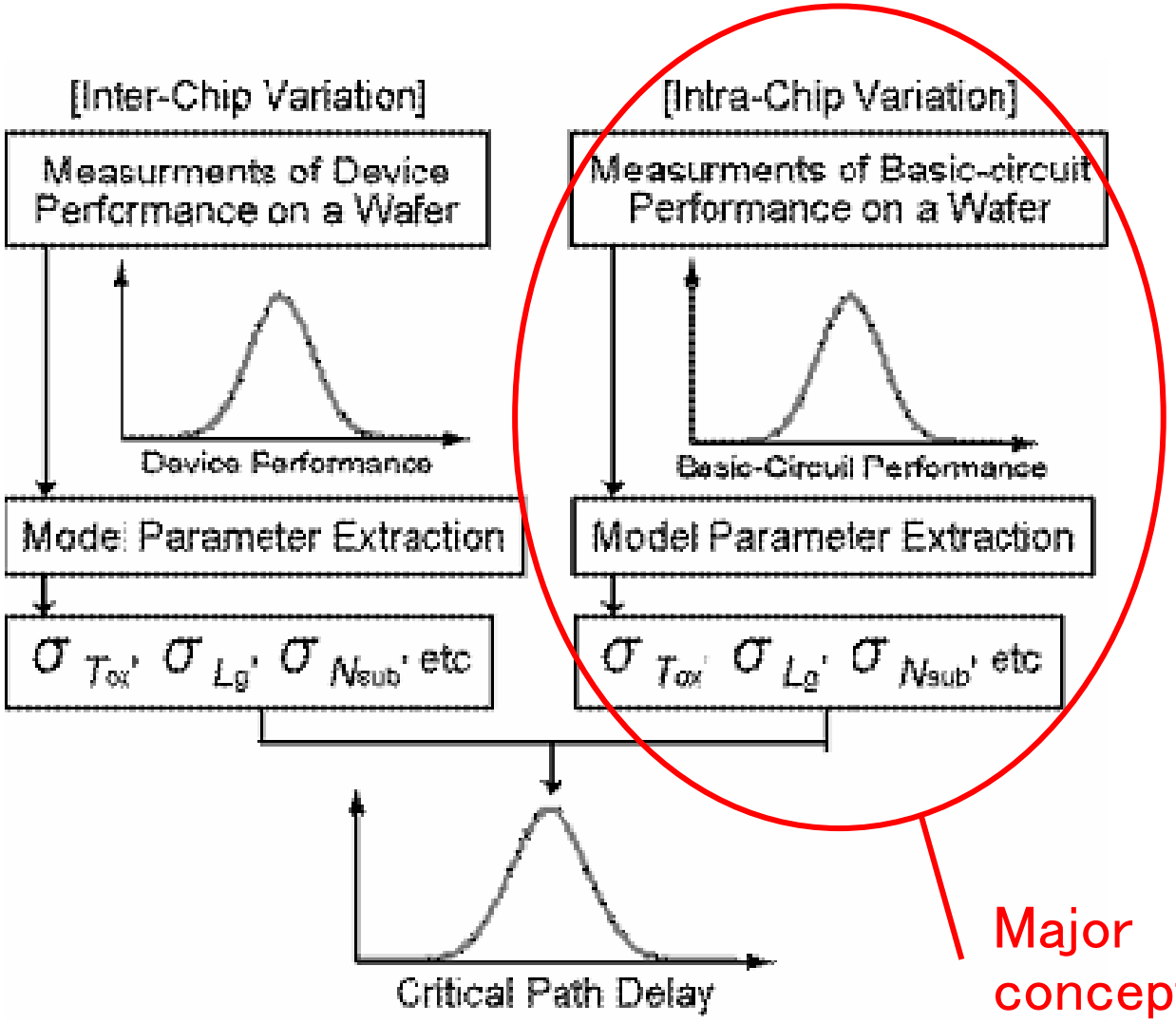


Short-channel devices show stronger asymmetry

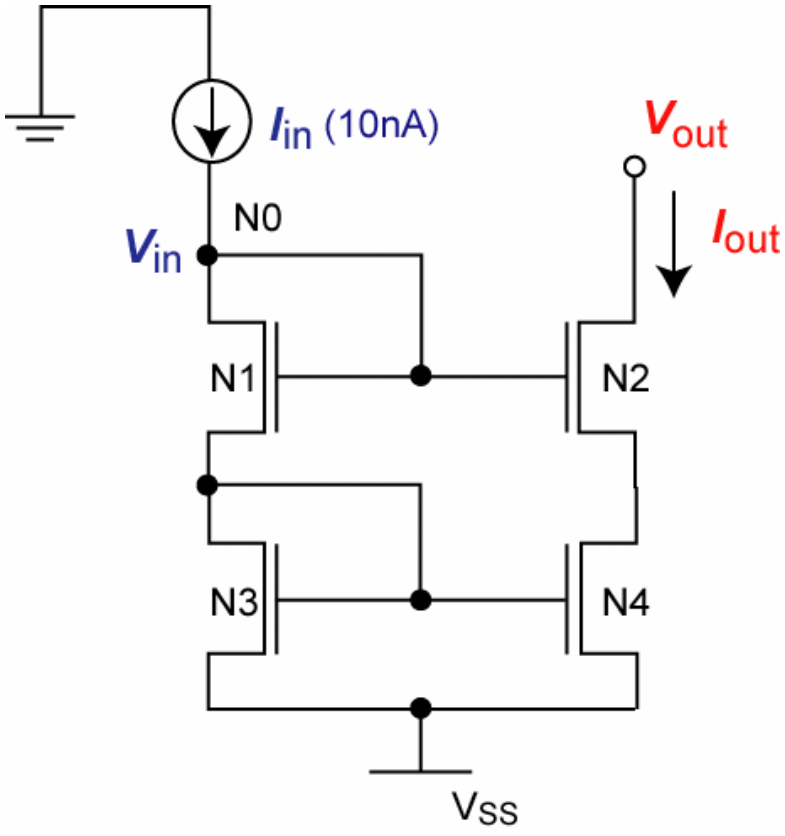
Outline

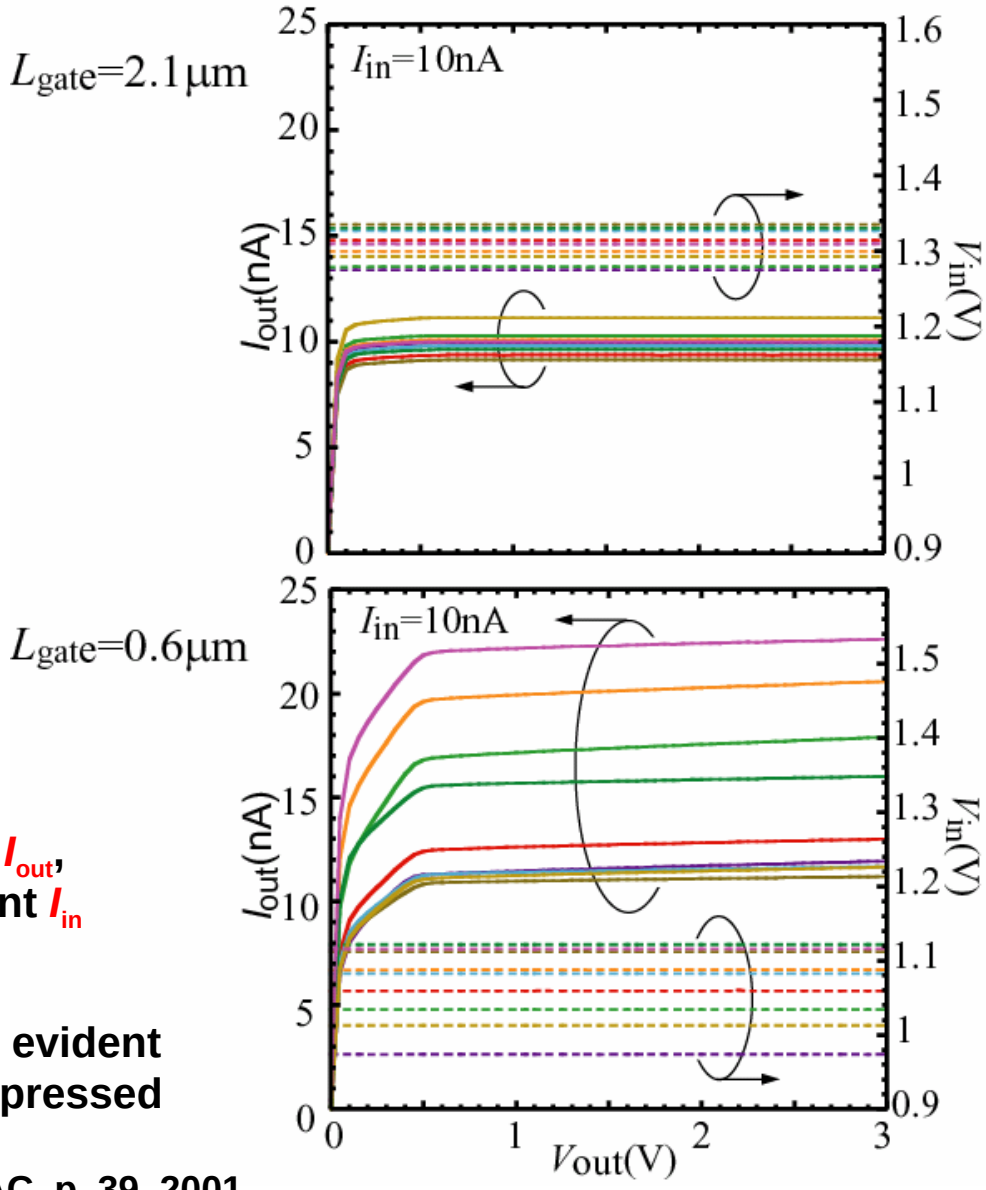
1. Conventional circuit-variation analysis based on device/process variation
2. Requirements for more accurate prediction of circuit-performance variation
3. Separation of inter-die and random intra-die variations with appropriate circuits
   - Cascode current source
   - Differential Amplifier Stage
4. Prediction of circuit-performance variation

Device and circuit based variation analysis



Cascode current source





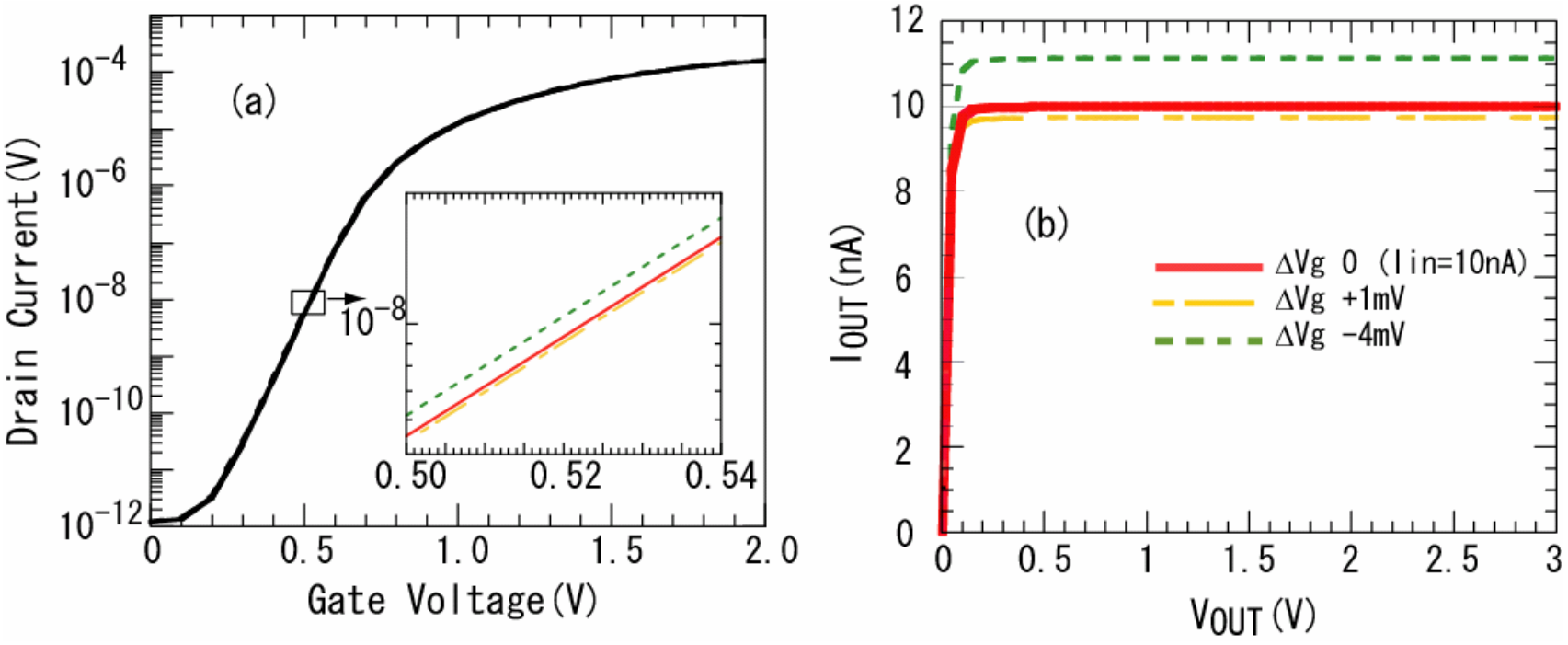
Function: to provide a constant current I_{out}, which is proportional to the given current I_{in} and independent of V_{out}.

I_{in}=10nA: technology variation becomes evident resistance effects etc. are suppressed

D. Miyawaki et al., APS-DAC, p. 39, 2001.

Variation of I_{out} result from N3/N4 mismatch

N3 is fixed and N4 is varied.



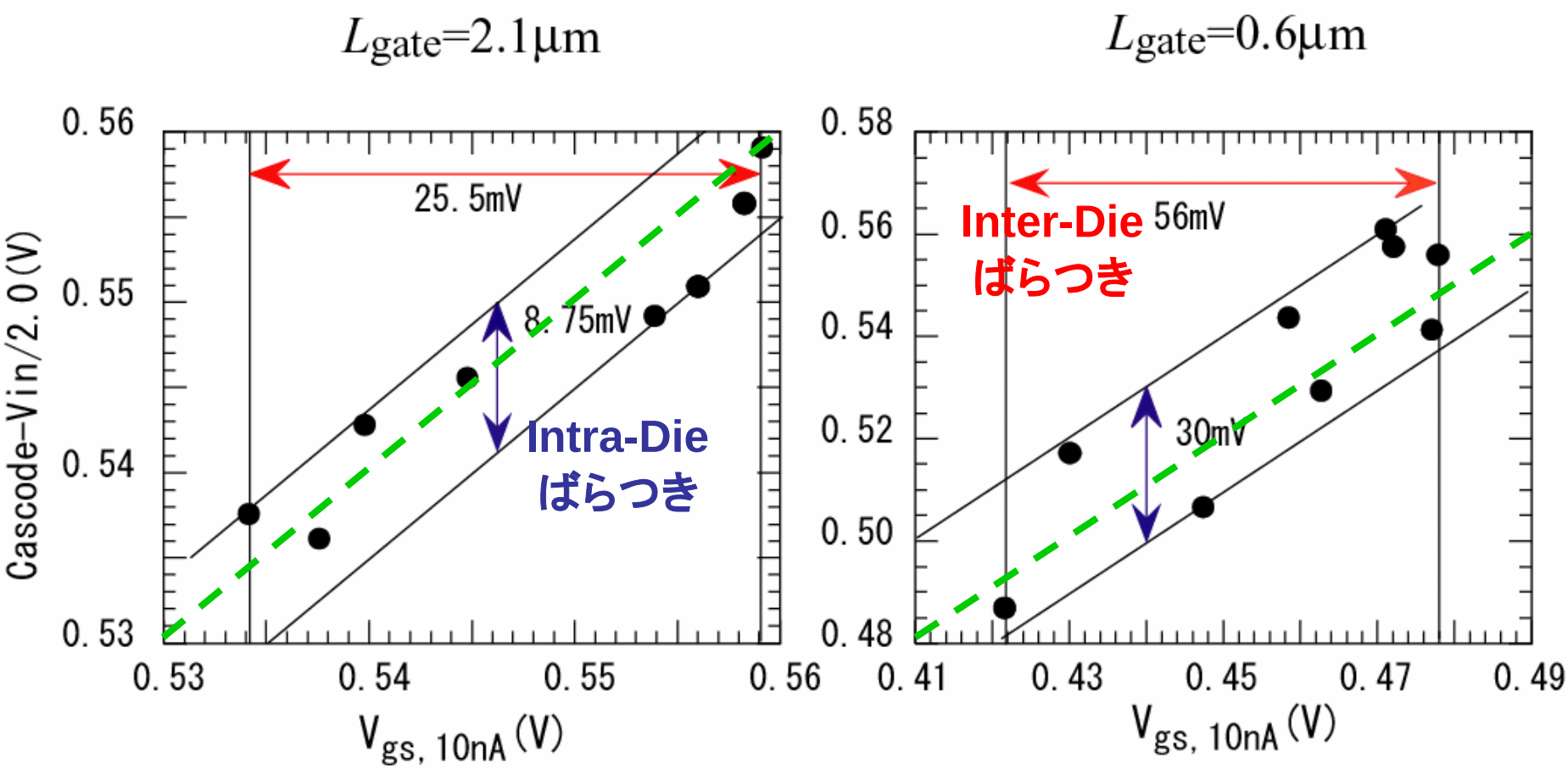
I_{out} variation allows to determine the ΔV_g mismatch.

Inter- and intra-die variation separation

V_{in} variation is determined by the combined variation of N1 and N3

Vin/2: Deviation from straight line determines intra-die variation

Vgs,10nA: Single MOSFET's inter-die variation



Connection to process-parameter variation

Deviation of process parameters from nominal values

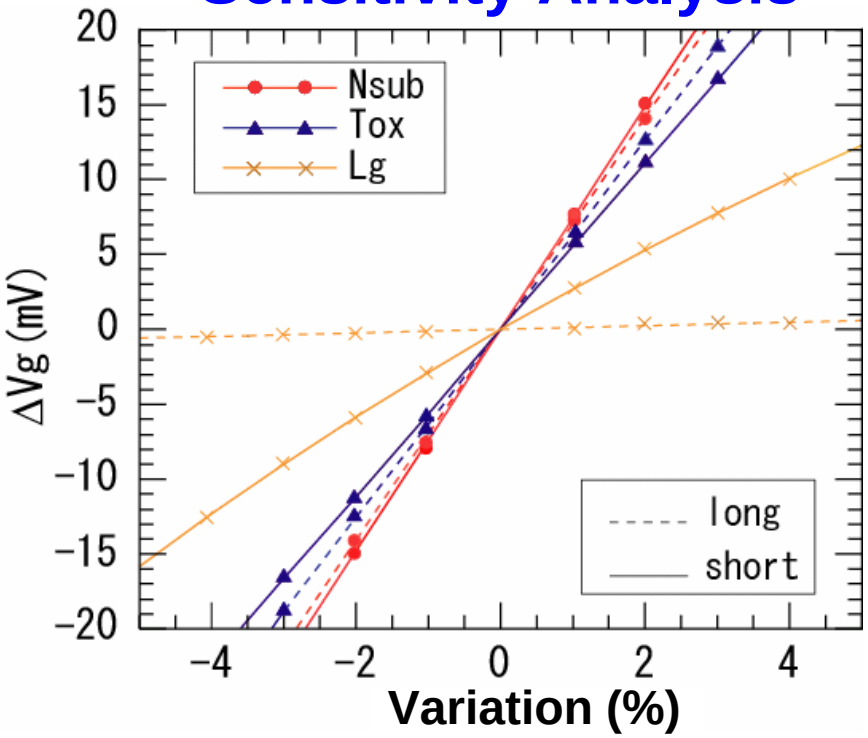
	ΔN_{sub}	ΔL_{gate}/0.6μm	T_{ox}
Inter	1.2% / -7%	6.7% / -3.3%	1.4% / 0.7%
Intra	1%	3.8%	0

ΔV_g variations determined with cascode current source

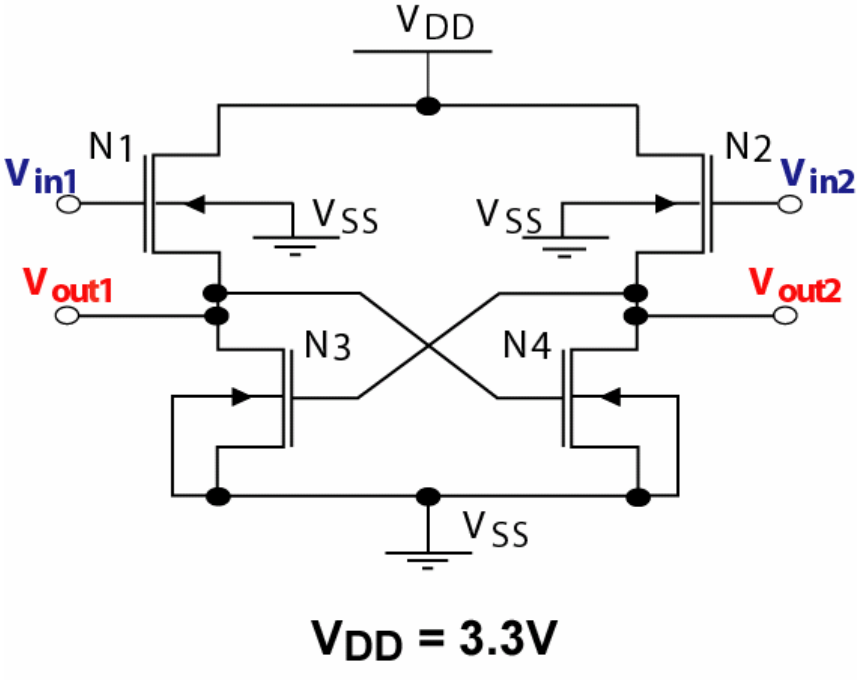
	2.1μm	0.6μm
Inter	25.5mV	56mV
Intra	8.75mV	30mV

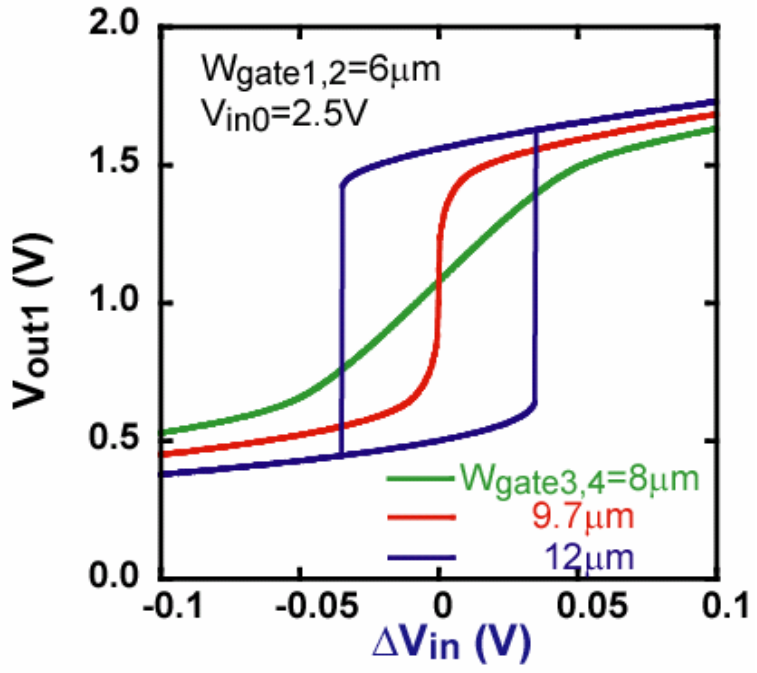
Sensitivity Analysis with HiSIM

Sensitivity Analysis



Differential amplifier stage





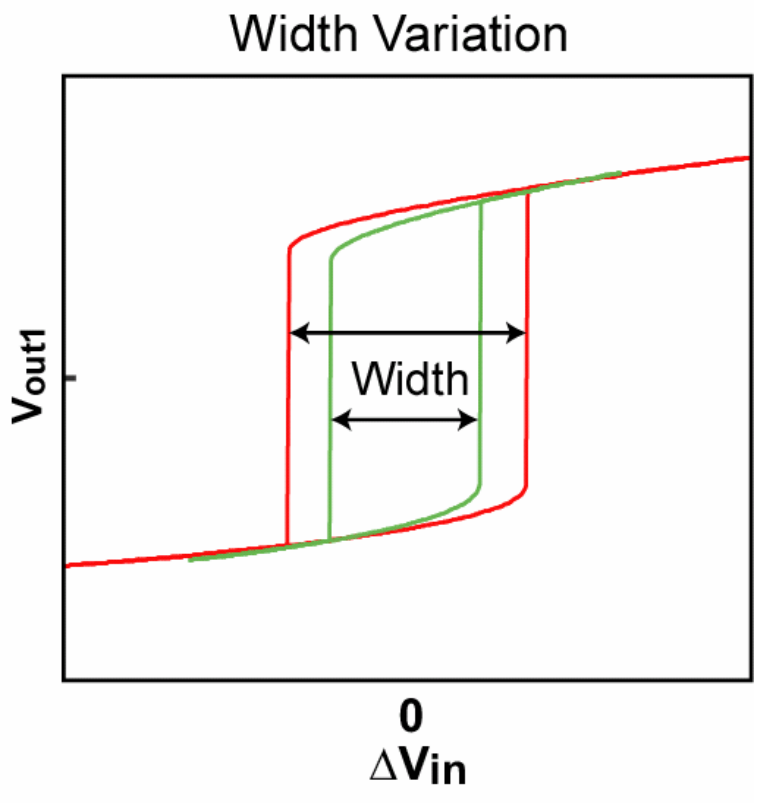
Function: to amplify V_{in} to V_{out}.

ΔVin= Vin1-Vin2

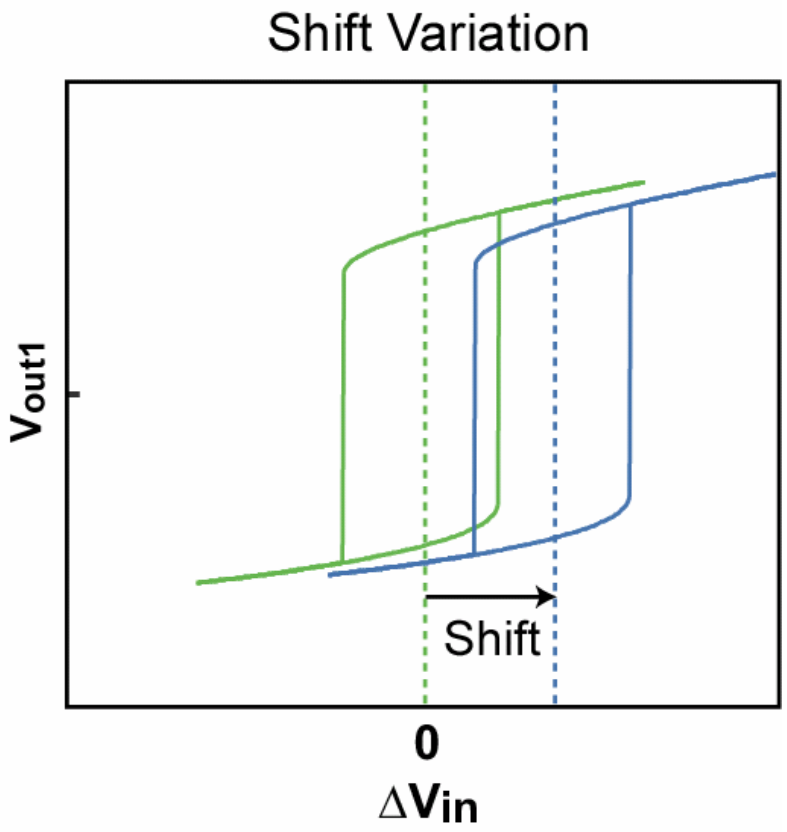
Appearance of a Hysteresis depends on the choice of channel width for N3 and N4

S. Matsumoto et al., CICC, p. 357, 2001.

Characteristic features of the hysteresis

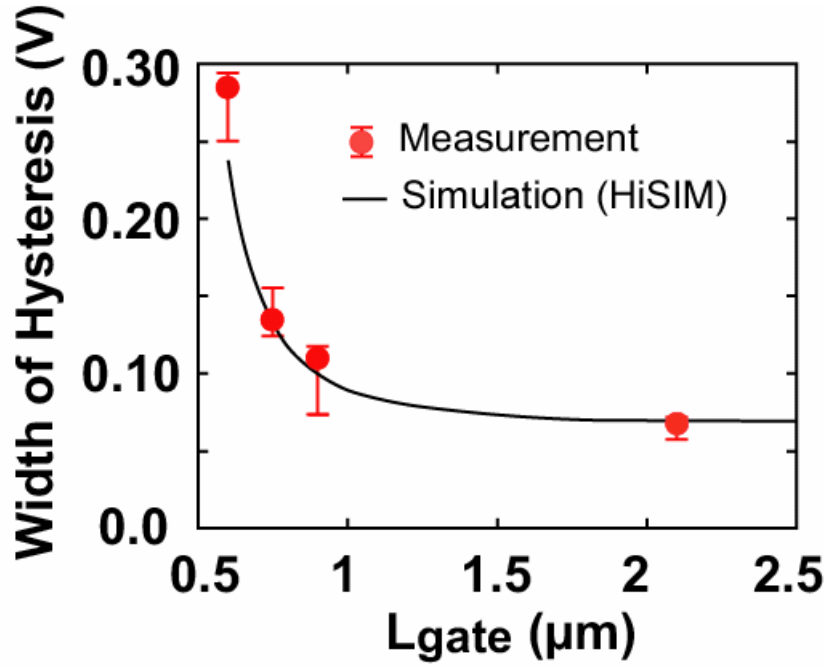


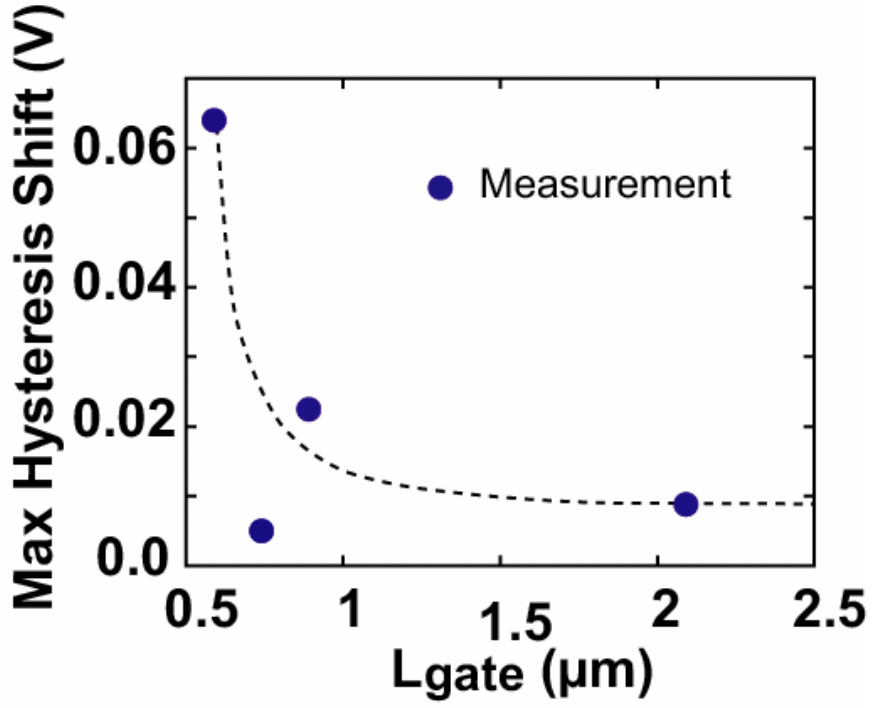
Same change of parameters for all 4 transistors



Difference in parameter change for the 4 transistors

Measured gate length dependence





Separation of inter-die and intra-die variation

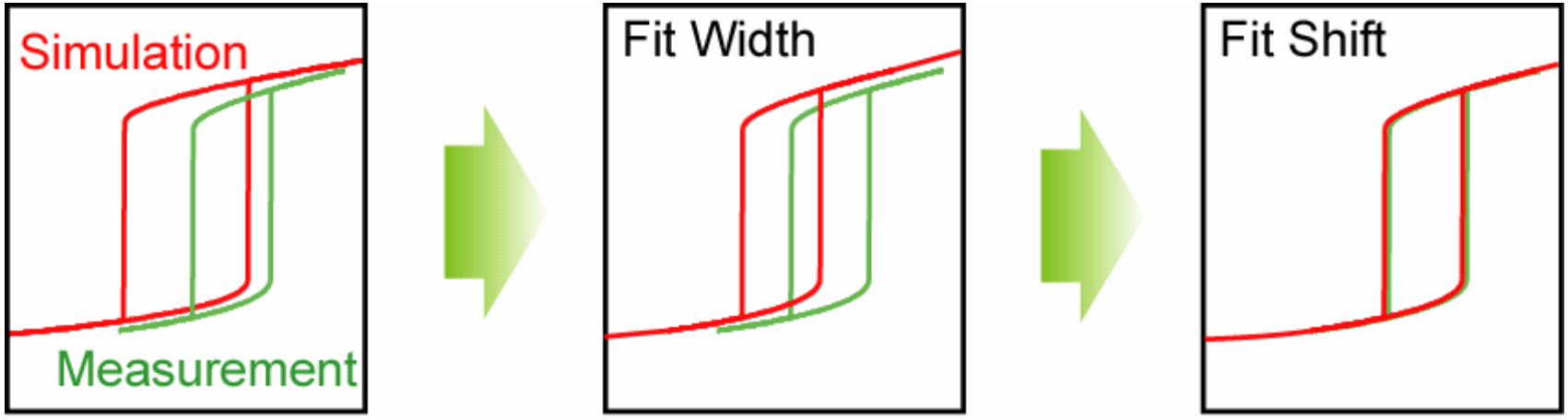
Case of same changes for all 4 transistors

Inter-Die Variation

Case of different changes for each transistor

Intra-Die Variation

Procedure for variation estimation



Inter-Die variation extraction

Intra-Die variation extraction

Results of variation estimation

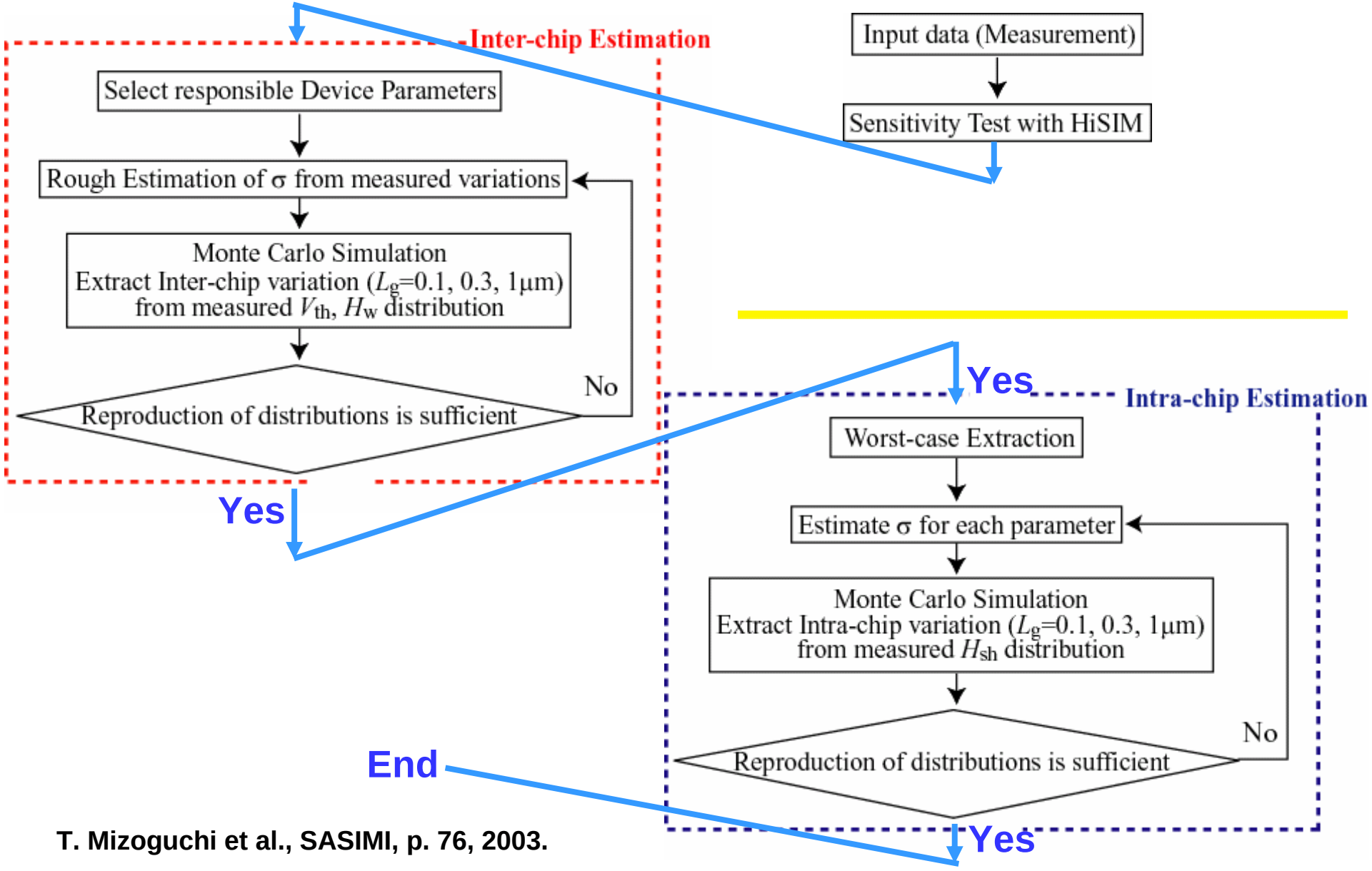
Cascode Current Source

	ΔN_{sub}	$\Delta L_{gate}/0.6\mu m$
Inter	7%	6.7%
Intra	1%	3.8%

Differential-Amplifier Stage

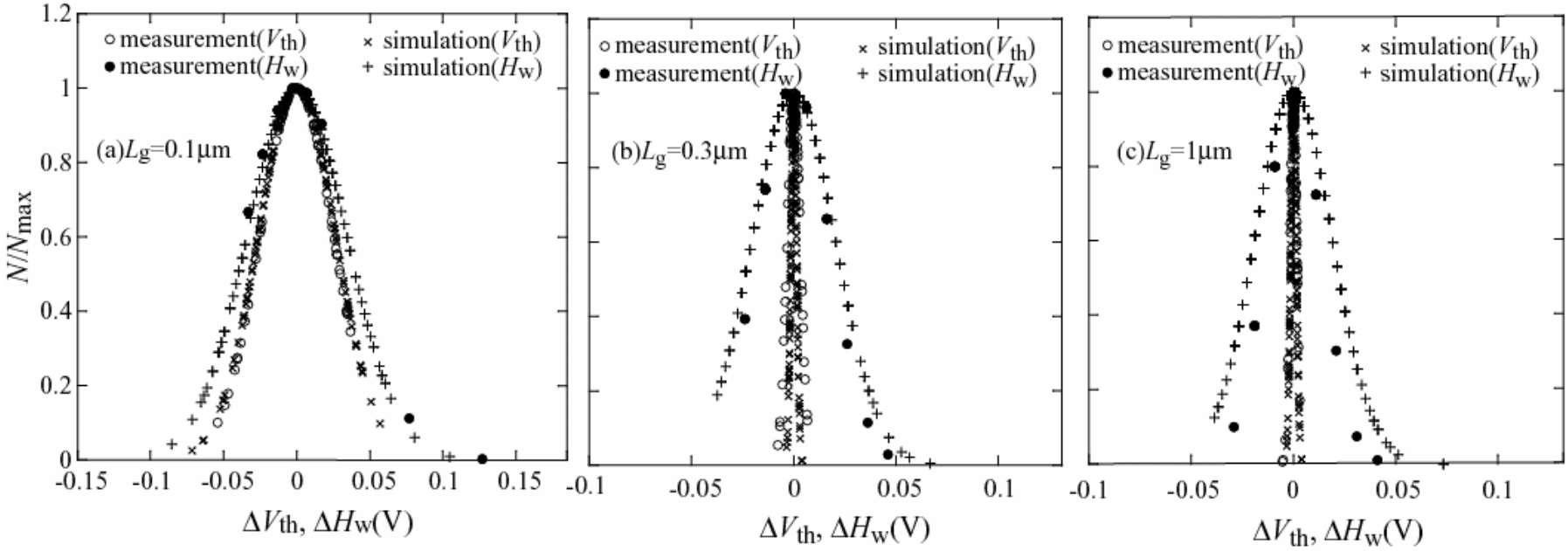
	ΔN_{sub}	$\Delta L_{gate}/0.6\mu m$
Inter	5.9%	6.2%
Intra	2.3%	3.2%

Extraction including distribution of variation



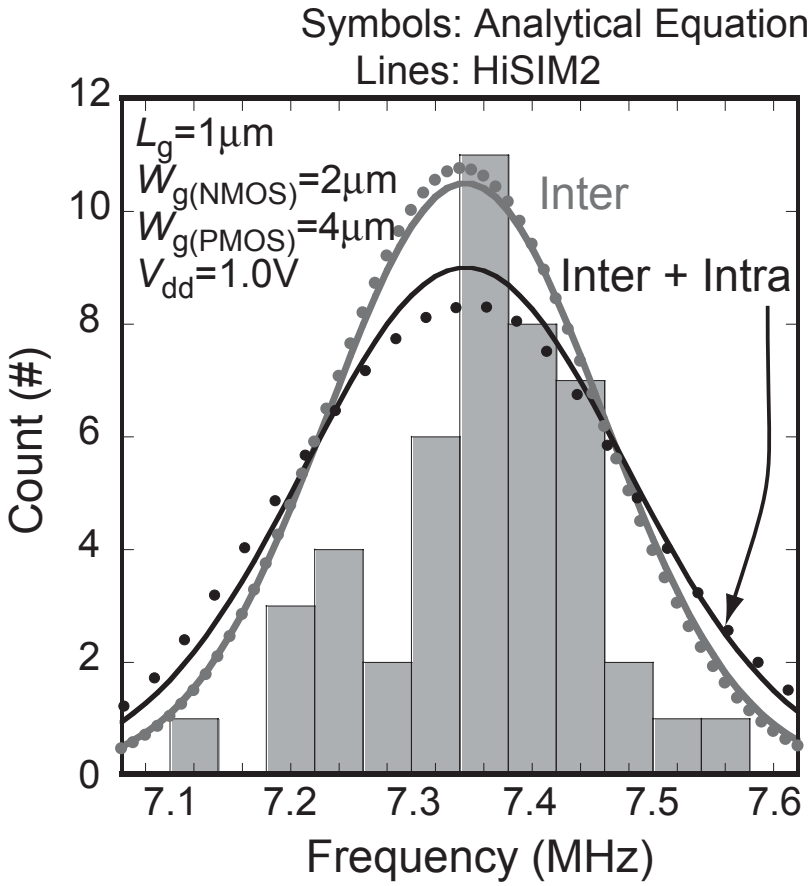
T. Mizoguchi et al., SASIMI, p. 76, 2003.

Simulated and measured variation distribution

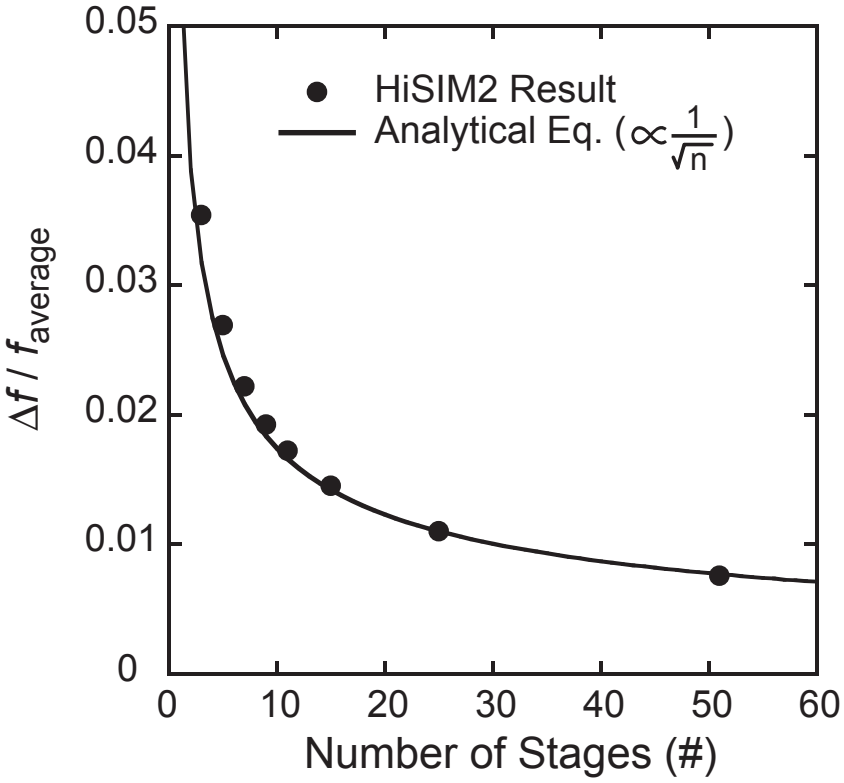


T. Mizoguchi et al., SASIMI, p. 76, 2003.

Prediction of ring oscillator variation



51 stages



stage number dependence

Conclusion

- Increase of variation effects requires a physically correct circuit-simulation model, which accurately interrelates process-parameter variations and device-performance variations.
- Separation of inter-die and intra-die variations is difficult and facilitated by using suitable circuits in the variation extraction process.
- Prediction of circuit-performance variation becomes possible under these conditions.

Presentation End

Thank you for your attention !